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Long-term Electro-Magnetic Robustness of Integrated Circuits: EMRIC research project

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Abstract

This paper presents the scientific achievements of EMRIC project that aimed at developing a new research activity which mixes EMC and IC reliability. This project contributes to improve the electromagnetic robustness (EMR) of integrated circuits over the full life-time of the electronic system, with a special emphasis on deep submicron technology. The results of this project give a unique overview about EMR in the scientific community and will contribute to develop EMR qualification procedures, EMR design techniques and EMR predictive methods.

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1. Introduction

Introducing new high performance electronic modules in automotive, aeronautic and aerospace applications forces system manufacturers to optimize system reliability and reduce time to market delivery and manufacturing costs. This trend has triggered off an increasing demand for conclusive statements about future lifetime and function of the product already at the design stage, ranging from electromagnetic compatibility (EMC) to thermal management issues and thermo-mechanical reliability forecasts. EMC has been applied to electronic systems for years, in order to ensure their insensitivity to external electromagnetic interferences (susceptibility or immunity) and their low electromagnetic radiation (emission) that could disturb neighbour equipment. Ensuring both low emission and susceptibility is required to guarantee a sufficient compatibility of the different electronic systems of an application and hence reach the functional safety level required for industrial applications.

EMC must be ensured at integrated circuit (IC) level and IC manufacturers are forced to check the EMC compliance of their products due to severe specifications [1]. The need to predict EMC of ICs after several years of operating life recently appears [2], driven by the trend towards extended warranty. Ensuring the electromagnetic robustness of nanoscale integrated circuits (extension of the EMC for the full lifetime of the product) has become a key challenge.

EMRIC (ElectroMagnetic Robustness of Integrated Circuits) project aims at developing a new research activity that mixes EMC and IC reliability to improve the electromagnetic robustness (EMR) of ICs, with a special emphasis on deep submicron technology.

During their lifetime, integrated circuits may be affected by harsh environmental conditions inducing internal degradation mechanisms that directly affect electrical performances and consequently electromagnetic behavior. The effect of natural aging of ICs on EMC is still misevaluated and has to be clarified. Highlighting the EMC drift issues induced by IC natural aging, understanding the links between the physical degradation mechanisms induced by ICs aging to the EMC drifts and predicting the extent of aging induced EMC drifts are the key challenges of this project.

Results interest both IC designers and critical system manufacturers. On the one hand, this project aims at integrating EMR concerns at different steps of an IC conception cycle. Integrating EMR models to simulation flow and developing EMR qualification procedures will help IC designer to ensure that EMC levels specified at the beginning of IC lifetime would remain within forecast margins during all the expected lifetime. On the other hand, the EMRIC project will provide EMR qualification test procedures and simulation methodologies to IC end users in order to give realistic and efficient EMR requirements to their IC manufacturers.

The first part of the paper presents the methodology set up to study the evolution of ICs electromagnetic behavior over their full lifetime. The second part, dedicated to experimental results, exhibits the drifts of a test chip electromagnetic emission and immunity levels and the link between degradation mechanisms and transistors physical parameters drifts that affect EMC. In the last section, a modeling and simulation approach is proposed.

EMRIC project described in this paper is supported by ANR (french National Research Agency), the french Midi-Pyrenees Regional Counsil and the CNES (french National Space Agency).

2. EMR experiment methodologies

2.1. Overall methodology

The EMR characterization of a circuit consists in

measuring the evolution during time of its parasitic emission and/or its susceptibility to radiofrequency interferences (RFI) before and after circuit aging.

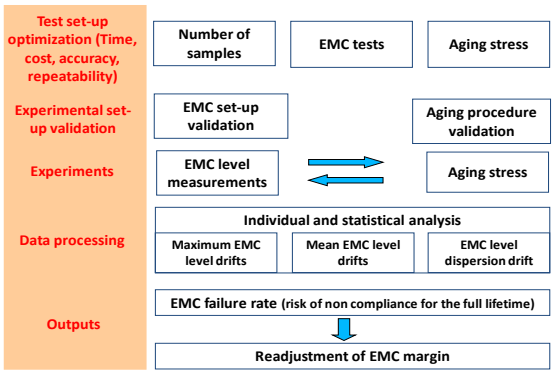


Figure 1. ICs Electromagnetic robustness experimental methodology

The first step of the proposed EMR qualification flow (Fig. 1) is linked to the choice and optimization of the experimental set-up, in order to save both time and costs, and guaranty the accuracy and repeatability of the measurements. Test set-up optimization is a critical step of the proposed methodology.

First, a compromise on the number of tested samples is found to ensure a sufficient level of confidence in measured EMC drifts and avoid too long characterization time.

In order to accurately characterize small EMC drifts, the error caused by measurement need to be limited: taking the precautions in the experimental protocol, using of equipment with long-term stability. Moreover, the design of EMC test board, the choice of passive components with low tolerance and the EMC test procedure (e.g. the susceptibility threshold extraction algorithm during immunity test) should be carefully optimized to reduce both repeatability and uncertainty issues.

To be efficient, the aging test always compresses the test duration scale by a stress that accelerates the intrinsic degradation mechanisms. The accelerated aging phase adds also uncertainties. As several samples are used to characterize the EMR of a component, the aging stress must be identical for all the samples. Moreover, the applied stress on each component must be controlled over all the stress duration. Thus, the stress conditions and the activity of circuits under test have to be accurately monitored.

ICs electromagnetic behavior is strongly linked with the electrical characteristics of semi-conductor active devices such as MOS transistor electrical parameters. The most relevant aging stresses for EMR characterization are the ones that affect transistors gate oxide inducing some electrical parameters change. Recently, some publications have shown that accelerated aging tests such as high or low temperature operating life (HTOL, LTOL), thermal cycling or electrical overstress induce a significant variation of electromagnetic behavior [3][4]. In the following experimental studies, standard (AECQ100) HTOL/ LTOL protocols and electrical stress have been selected to accelerate electrical degradation mechanisms.

As far as concerned EMC tests, IEC standards methods adapted to IC conducted and radiated emission and immunity characterization may be applied. Uncertainties of these methods are acceptable to ensure consistency of EMR results.

Conducted emission (IEC 61967-4) that consists in measuring the parasitic current produced by the IC and flowing through the ground pin, has been chosen. For immunity tests, direct power injection (DPI) method (IEC 61967-4) will be applied. It consists in superimposing RF disturbances to a low frequency signal through a decoupling network, to couple a conducted disturbance to a pin of a circuit. This is an efficient method to couple disturbances to the circuit.

Once EMC and aging procedure set-ups have been completely defined, they have to be validated experimentally. A validation step is necessary to ensure that aging procedure is the only responsible of DUT EMC drifts. The EMC validation step must ensure that the EMC measurements are repeatable enough to extract precise information concerning the EMC drifts related to aging effects. Measurement repeatability and uncertainties set a limit for the consistence of EMC level drifts.

At the end of the measurement campaign, the EMC measurement results obtained before and after aging are processed to extract statistical data concerning the EMC level drifts, such as the worst case and the mean drifts. These data are required to predict the risk that a component becomes incompliant after aging and, if necessary, readjust the EMC margins at the design level.

2.2. EMC drifts after aging: experimental results

In order to exhibit aging effect on IC EMC, the EMR methodology has been applied to a 65 nm low power CMOS technology test chip developed by ST-

Microelectronics and dedicated to the characterisation of several I/O structures.
Standard conducted emission is characterized by measuring the I/O current consumption on ground pin. As far as concerned I/O immunity, RFI are injected on I/O power supply pin . These two tests are applied on a batch of 10 components, before and after aging. Two separated batches of 5 components have been placed during 408H in a climatic chamber which regulates the temperature respectively at 150°C (HTOL) and -40°C (LTOL) (AECQ100 protocol) combined with high supply voltage (10% higher than the nominal).
Figure 2 presents the mean drift (over 5 samples) between the emission levels of fresh and aged components, for both HTOL and LTOL accelerated life tests. Immunity level mean drifts (over 5 samples) are shown in figure 3. Experimental results are reported in Table 1. Emission levels decrease clearly after both aging tests over almost all the frequency range. LTOL induces a greater emission level reduction (with a mean value about -1.48 dB) than high temperature stress (-0.3 dB on average).

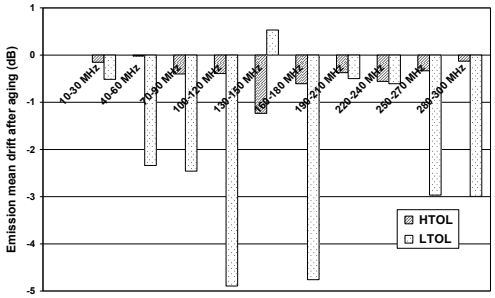


Figure 2. LTOL and HTOL aging impact on emission level (mean drift for all samples)

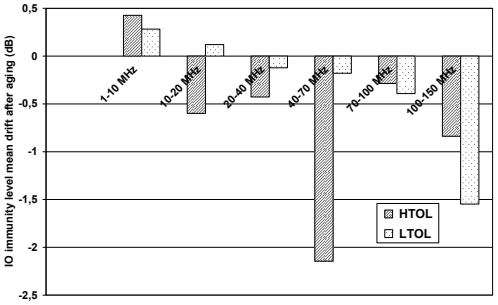


Figure 3. LTOL and HTOL aging impact on immunity level (mean drift for all samples)

Conversely, aging seems to have a negative impact on IO immunity when RF injections are performed on power supply pins. Both aging tests induce a noticeable reduction of the immunity level over a large frequency range. HTOL induces a greater immunity level reduction. Even if the average global fading of immunity level remains acceptable, the large reductions of immunity level on some samples at several frequencies (up to -8.75 dB) can seriously affect their EMC compliance.
These first experiments that exhibit some potential issues due to EMC levels evolution after aging, clearly indicate that there is a direct link between internal degradation mechanisms and EMC behavior.

EMC test	Aging Test	Max. aging drift above all frequencies (for the most affected sample)	Mean aging drift (entire batch)
Emission	HTOL	2.2 dB / -9.5 dB	-0.3 dB
	LTOL	15.3 dB / -12 dB	-1.48 dB
Immunity	HTOL	2 dB / -8.75 dB	-0.8 dB
	LTOL	1.26 dB / -8.25 dB	-0.6 dB

Table 1. Summary of LTOL and HTOL aging impact on emission and immunity levels

3. From MOS physical degradation to EMC drifts

3.1. Impact of transistor parameters drifts

During their lifetime, CMOS transistors are affected by intrinsic failure mechanisms, such as Electro Migration (EM), Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI), Time Dependent Dielectric Breakdown (TDDB), mainly activated by harsh environmental conditions such as high or low temperature and electrical overstress. The time to wear out or the lifetime of the device depends not only on the IC technology, but also on environment, as temperature, supply voltage, the operating frequency or clock duty cycle. The failure origins and modeling are studied for years and active researches are still on-going. Among them, HCI and NBTI are the major contributors to the device performance degradation in advanced CMOS technologies. The degree of degradation of a device and, hence, its lifetime depend on the stress level and duration (Table 2). Degradation mechanisms such as HCI and NBTI affect transistor parameters such as threshold voltage (VTH) and carrier mobility (μ), which could lead to circuit characteristic changes. Thus it could lead to drift of circuit electromagnetic emission or susceptibility to interferences by the

modification of the electrical behavior of internal functions such as noise margins, Jitters, current consumptions, delays…

	HCI	NBTI
Origin	High kinetic energy carrier induced interface trap and fixed oxide charge generation	Bias induced interface trap and fixed oxide charge creation.
Transistor type	NMOS	PMOS
Acceleration factors	High Vds Low temperature	High absolute Vgs High temperature
Threshold voltage (|VTH|)	Increase	Increase
Mobility (µ)	Decrease	Decrease
Drain saturation/linear current	Decrease	Decrease
Other	Substrate current (Ib) increase	Channel off current (Ioff) increase

Table 2. Impact of oxide defects based degradation mechanisms

In order to illustrate how HCI and NBTI affect the transistor characteristics [3] [4], a dedicated test chip (Freescale CMOS 90 nm) containing NMOS and PMOS devices with various geometrical and gate options has been developped. Their terminals (gate, drain, source, bulk) are accessed with DC probes in order to apply electrical stresses which accelerates NBTI or HCI and measure the evolution of the drain current. Depending on the stress voltage and duration, the drain current decreases continuously. From the measurements of the evolution of drain current vs. stress time and voltage, the evolution of the transistor V_{TH} and µ can be modeled by empirical laws, which have considerable importance for the selection of efficient aging acceleration conditions and EMR prediction.

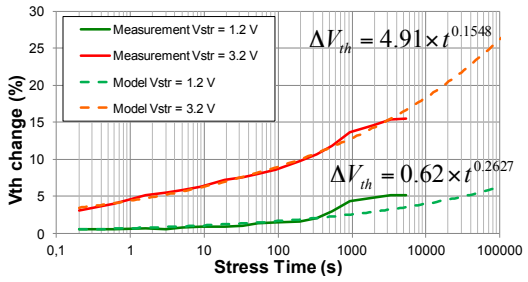


Figure 4. Measurement of VTH evolution of 90 nm low voltage PMOS device exposed to negative gate-source voltage

Fig. 4 presents the results of experimental characterization of NBTI impact on the V_{TH} of a PMOS transistor. Two negative gate-source voltages of -1.2 V and -3.2 V have been applied and the evolution of V_{TH} has been extracted from the drain current measurement. V_{TH} increases continuously with time according to a power law.

3.2. Effect of aging on IC electromagnetic emission

During the EMRIC project, numerous emission measurements combined with accelerated-aging conditions have been done on various type of ICs (small digital cores, oscillators [5], I/O buffers [6]) designed in CMOS 0.25 µm, 90 nm, 65 nm. Globally, the same conclusion has been drawn from all these experiments: applying electrical or thermal stress to ICs leads to a time dependent reduction of the electromagnetic emission (EME), whatever its technology. The technology changes only the sensitivity to stress conditions. Fig. 5 and 6 illustrate two experimental results about the effect of electrical stress applied on a CMOS 90 nm ICs, supplied at 1.2 V nominally. Fig. 5 shows that the degradations accelerated by the stress lead to a significant reduction of the power supply voltage bounce of a digital core [5]. Fig. 6 presents the evolution of the conducted emission from the switching of a digital output buffer after different stress durations [7]. The result shows a significant and gradual reduction of the high frequency spectral content of the noise created by the I/O switching.

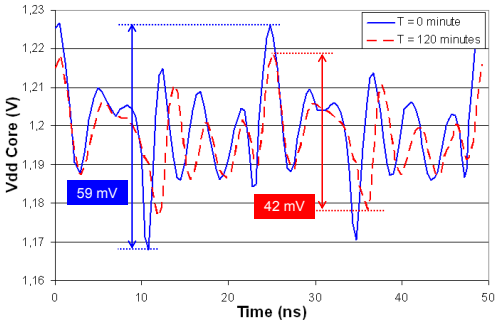


Figure 5. Evolution of the power supply voltage bounce of a digital core designed in CMOS 90 nm after 120 minutes of 3.6 V electrical stress [3]

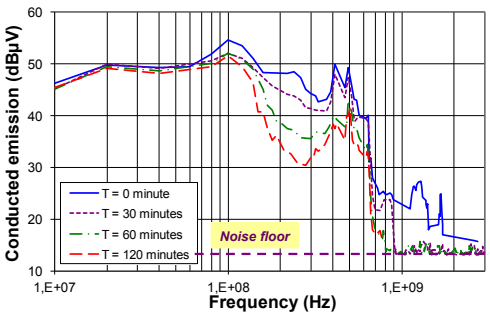


Figure 6. Evolution of the conducted emission of an I/O buffer after 120 minutes of 7 V electrical stress [5]

Experimental analysis coupled with CAD simulation helps to understand the mechanisms which lead to the reduction of the EME. IC emission depends on two parameters:

- the dynamic current consumption (in other words the "noise source") which is linked to the circuit activity and the characteristics of each gates
- the power distribution network (PDN) formed by the IC package, IC interconnects, on-chip intrinsic and added capacitance, which forms an equivalent passive filter for the noise induced by the circuit activity.

The reduction of the EME of ICs is associated to the reduction of the amplitude and the temporal spreading of the dynamic current consumption of the IC. As explained in the previous part, thermal or electrical stresses accelerate degradation mechanisms which reduce the current capability of MOS transistor. The consequences are the decrease of transistor drive current and the increase of switching time, which have a direct impact on EME from electronic functions such as digital circuits or I/O buffers. A campaign of impedances measurements confirms that the characteristics of IC PDN are not disturbed by electrical or thermal stresses. An interesting observation is that on-chip capacitors (MOS, metal-insulator-metal or polysilicon type), which are a well-known and efficient technique to reduce EME of ICs, are not affected by stresses significantly and do not contribute to an increase of EME.

Although these results are very positive for the control of EME at IC level, the impact of aging on EME should not be overlooked. Around the IC, passive devices such as capacitors, inductors or ferrites constitute efficient filtering elements of EME. However, their characteristics drift under high temperature and high voltage conditions. In applications such as switching-power mode supply, the combined degradation of filtering capacitors and inductors lead to a significant increase of both conducted and radiated EME over large frequency ranges which could compensate the reduction of EME of ICs. Predicting the evolution of EME at printed circuit board (PCB) level relies on an accurate modelling of the contribution of each part: ICs and passives.

3.3. Effect of aging on IC susceptibility

Comparing to the conclusion drawn about the impact of aging on EME, the effect of aging on EMS is less straightforward. Various types of functions have been tested during the EMRIC project, such as digital circuits [8], I/O buffers [6], voltage regulator, bandgap, operational amplifiers [9] and phase-locked loop [10], designed in CMOS 0.25 µm, 90 nm, 65 nm. Both positive and negative variations of the susceptibility levels have been measured after aging accelerated by electrical or thermal stresses, depending on the nature and the design of the tested functions. Understanding the origin of susceptibility level drift of an internal functional block requires an analysis of the physical degradation of its transistors (localization of degraded transistors, V_{TH} or mobility modifications) and then an analysis of the impact of these electrical parameters drifts on the block sensitivity to electromagnetic disturbances.

The following example is proposed to illustrate the potential effect of aging on EMS of ICs. The propose case study concerns a phase-locked-loop (PLL) designed in CMOS 0.25 µm technology [10]. The structure of the PLL is described in Fig. 7. The voltage-controlled oscillator (VCO) is based on delay-controlled ring oscillator. The VCO is made of three delay cells, where the introduced delay depends on the voltage applied on the gate of the PMOS transistors noted T_{P1}, T_{P2} and T_{P3}.

The circuit is stressed according to the accelerated-life test standard HTOL. Ten components are supplied nominally in a climatic chamber during 400 hours. Conducted susceptibility tests are performed before and after aging stress.

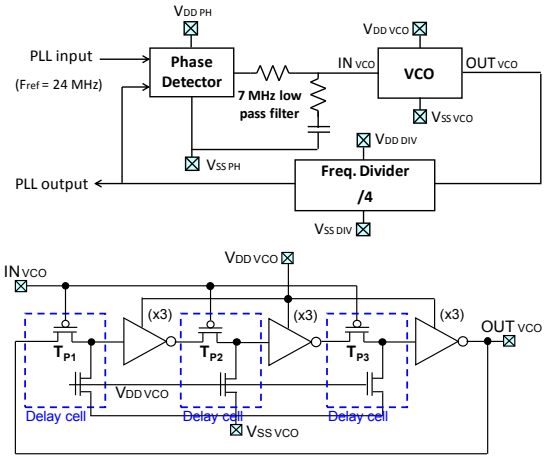


Figure 7. Internal structure of the tested PLL (top) and VCO (bottom) [8]

They consist in applying harmonic disturbances on the power supply of the PLL over the band 10 MHz to 1 GHz, and determining the minimum disturbance amplitude to produce a deviation of 5% of the nominal period of the PLL output signal.

Fig. 8 presents the comparison between the average susceptibility level of the PLL before and after the HTOL test. A significant reduction of the immunity level is observed over a large frequency range. The average reduction computed on ten components is equal to 2.6 dB while the maximum reduction exceeds 10 dB. Although the PLL remains functional in nominal conditions, power supply noise margin to prevent a functional failure is considerably reduced.

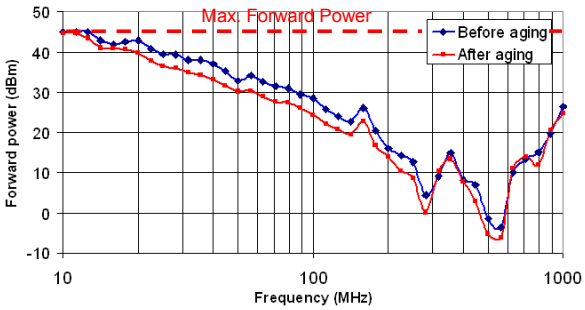


Figure 8. Evolution of the average susceptibility level of a PLL before and after an accelerated-life test [8]

Experimental measurements and CAD simulations have been performed to clarify the origin of this phenomenon. The most sensitive block of the PLL is the VCO, which converts power supply voltage fluctuations in jitter on the output signal, which can destabilize the PLL. The characterization of the VCO before and after the stress has proved that the internal degradation mechanisms have contributed to slow down the VCO and thus shifted the capture range of the PLL. Investigations based on CAD simulations have demonstrated that PMOS transistors T_{P1} to T_{P3} in the VCO are placed in conditions which accelerate NBTI during the stress and that the modification of their threshold voltage V_{TH} and mobility Uo leads to a reduction of the immunity of the PLL to power supply voltage fluctuations, as shown in Fig. 9.

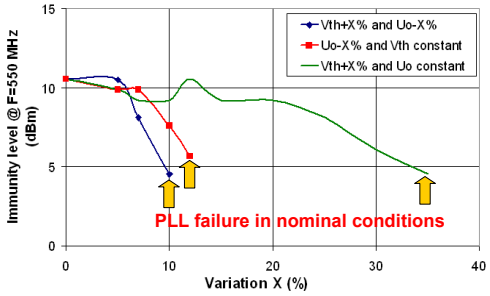


Figure 9. Simulation of the sensitivity of the PLL immunity level to variations of delay cell PMOSFET threshold voltage and mobility [8]

4. Prediction of long-term electromagnetic robustness

The evolution of EME and EMS at PCB level is dependent of the evolution of the contribution of each mounted IC and the filtering effectiveness of passive devices. An important issue to ensure the long term electromagnetic robustness of electronic applications is the prediction of the risk of non-compliance to EMC standard levels after several years of operation in harsh environments. It relies on time dependant IC EMC models. One of the objectives of EMRIC is the development of EMC models for ICs which takes into account the effect of aging. These models aim at constituting a brick to estimate the evolution of EME and EMS at PCB level.

4.1. Modeling of the evolution of IC emission

These last years, the research community which deals with EMC of ICs issues has produced a significant work about the modeling of conducted and radiated emission of ICs [11]. One of the main results was the proposal of the Integrated Circuit

Emission Model (ICEM) standard [12], which defines a methodology to build simple and non-confidential IC model dedicated to the prediction of conducted and radiated emission. Basically, ICEM proposes to model the IC in two subblocks: the internal activity (IA) block which models the transient current produced by circuit operation, and the power distribution network (PDN) which models the filtering effect of the transient current due to IC and package.

This modeling standard constitutes an interesting basis to propose an IC emission model which integrates the aging effect. As explained in part 4.2, predicting the drift of IC emission relies on an accurate modeling of the evolution of dynamic current consumption. Changing the parameters of the IA block of the ICEM model in order to spread the IC current consumption constitutes an easy method to simulate the effect of aging. Fig. 10 describes the proposed methodology to build an aging-aware ICEM model. From the IC netlist and empirical laws about transistor parameters evolution in a given stress condition, the IC current consumption changes can be simulated and the IA block of ICEM can be updated to take into account the IC aging.

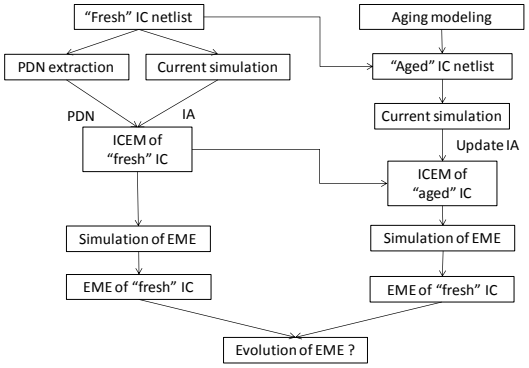


Figure 10. Aging-aware ICEM construction flow

This methodology has been used to simulate the evolution of the conducted emission of a digital core designed in CMOS 90 nm technology submitted to electrical stress [13]. Experimental characterizations of the impact of electrical stress on transistors have been performed to model the evolution of V_{TH} and μ parameters. An ICEM model has been built with a basic IA block made of two triangular waveform current sources. The integration of the aging in the ICEM model has been done with an empirical coefficient called "degradation ratio", which modifies both amplitudes and timing characteristics of the IA current sources. Fig. 11 compares the measurement and the simulation of the evolution of the conducted emission spectrum when the core is exposed to an electrical stress. The ICEM model is able to predict with a quite good accuracy the time-dependent reduction of the conducted emission spectrum up to 1 GHz. This result demonstrates that a simple and non confidential approach based on an ICEM model ensures reasonable estimation of the evolution of the EME.

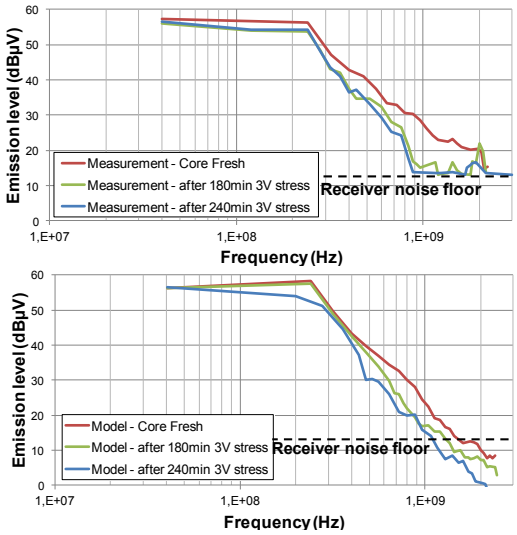


Figure 11. Measurement (top) and simulation (bottom) of the evolution of the conducted emission of a CMOS 90 nm digital core exposed to a 3 V electrical stress

4.2. Modeling of the evolution of IC susceptibility

The same type of approach has been followed to propose IC susceptibility models which integrate the aging effect. However, the research work about IC susceptibility modeling and the proposal of a modeling standard are still on-going actively. We propose to simulate IC susceptibility from a model composed of two sub-blocks: the Power Distribution Network (PDN) which describes the coupling path of the incoming disturbances and the Internal Behavior (IB) block which describes the nominal operation of the IC and detects the induced failures. As the PDN is not affected by aging, only the IB block will be modified. The IB block construction can be based on CAD simulation of the circuit netlist and modified transistor models to take into account the effect of stresses. Details about aging-aware susceptibility model can be found in [13].

This methodology has been applied to simulate the evolution of the susceptibility level of the PLL [10]. The PDN block of the circuit has been extracted by S parameter measurements, while a simple approach has been used to build the IB block. SPICE simulations of the PLL netlist have been performed to generate a "sensitivity table", which provides the minimum voltage fluctuations to apply on the PLL power supply to induce a failure. Different versions of transistor model library, with modified values for V_{TH} and µ parameters, have been used in order to take into account the aging. The IC susceptibility model is very simple as it contains only a passive network for the PDN and a simple monitoring of the PLL power supply voltage fluctuations to detect a failure condition. Fig. 12 presents the comparison between the simulated susceptibility level of fresh and aged PLL. These simulation curves have to be compared with the measured susceptibility levels presented in Fig. 8. The simulation predicts a global reduction of several dB of the immunity level over a large frequency range, as observed in measurement.

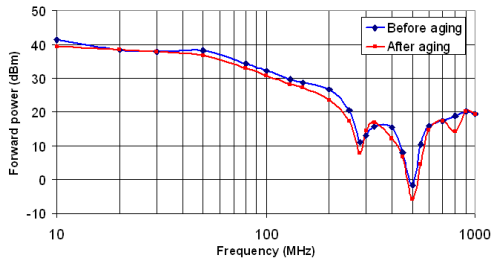


Figure 12. Simulation of the susceptibility level of the fresh and aged version of a CMOS 0.25 µm PLL [8]

7. Conclusion

This paper gives an overview of a four years project dedicated to the electromagnetic robustness concept that is an extension of the electromagnetic compatibility for the full lifetime of the device. After the presentation of the developed methodology to quantify the effect of aging on EMC of ICs by measurements, experimental results exhibited some emission and immunity level drifts on dedicated test chips after accelerated aging stresses. To study the impact of device intrinsic degradation on the circuit electromagnetic behavior, semiconductor failure mechanisms that can significantly modify electrical performances have been experimentally activated. Device degradations and induced electrical parameters changes have been evaluated. Transistor current drive and switching time are reduced after aging stresses leading to a reduction of the amplitude and the temporal spreading of the dynamic current consumption of ICs that have a direct impact on EMC. Finally a simulation methodology to predict the impact of circuit aging on conducted susceptibility and emission is presented and applied to predict a PLL immunity level reduction as well as a core emission level reduction after aging stress.

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