Prediction of Long-Term Immunity of a Phase-Locked Loop

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Abstract— **Degradation mechanisms accelerated by harsh conditions (high temperature, electrical stress) can affect circuit performances. Submitted to electromagnetic interferences, aged components can become more susceptible, which stirs up questions about the safety level of the final application. Unfortunately, the impact of circuit aging on its susceptibility level remains under evaluated and is not taken into account at circuit design level. This paper presents a first attempt of a modeling methodology aiming at predicting the impact of circuit aging on the susceptibility to electromagnetic interferences. This methodology is applied to model and explain the measured variations of the susceptibility level of phase-locked loop after an accelerated-life test.**

Keywords - Integrated circuits; susceptibiity to electromagnetic interferences; immunity modelling, circuit aging, reliability.

I. INTRODUCTION

In electronic systems, numerous electromagnetic compatibility (EMC) mitigation techniques (shielding, filtering, decoupling, grounding…) are used to ensure a sufficient robustness to electromagnetic interferences (EMI) and the compliance to susceptibility standard. However, during their lifetime, electronic systems are exposed to harsh conditions (high temperature, moisture, thermal cycling, overvoltage…) which contribute to accelerate the aging process. Several sources have reported that typical EMC mitigation techniques are affected by harsh conditions. For example, corrosion can degrade filter ground bound or shield joint [1]. The permittivity of the dielectric of ceramic capacitors widely used for decoupling is also affected by aging [2]. Therefore, depending on the amount of degradations, the aging-induced evolution of parasitic emission and susceptibility can have a serious impact on safety level of the system and should be anticipated.

Even if the aging impact on filter efficiency, shielding, decoupling capacitor have always been referenced in literature, no precise information concerning the impact of aging of integrated circuits (IC) on EMC exist to the author knowledge. It is well known that harsh environmental conditions such as high temperature or electrical overstress affect deep submicron IC by accelerating failure mechanisms such as negative bias temperature instability (NBTI) or hot carrier injection (HCI) during their lifetime [3]. Even if they trigger soft failures which do not compromise circuit operation, they can have a significant impact on performances (leakage current, noise, operating frequency…). The susceptibility of ICs to voltage fluctuations induced by EMI can be also affected if the margin to electromagnetic disturbances is shrunk. Recent publications have shown experimentally or by simulation the potential impact of IC intrinsic degradation mechanisms on susceptibility to EMI [4] [5] [6]. The reduction of margin to EMI induced voltage fluctuations can have serious consequences on the long-term immunity of circuits and thus to the long-term safety of electronic applications. Even if an aged circuit remains functional in nominal conditions, this circuit could fail with a smaller amount of EMI. Besides, typical EMC compliance tests done on “fresh devices” are not able to provide any evaluation of the evolution of susceptibility level after several years of operation. Combining EMC, environmental or accelerated-life tests could be used to evaluate the risk of reduction of robustness to EMI with time. However, combining these tests and applying them on a batch of several devices under test increase the complexity, the time and the costs of the EMC compliance procedure. Simulations which handle both device degradation mechanism models and susceptibility prediction could help designers to anticipate susceptibility level increase more efficiently.

This paper addresses the long-term immunity issue induced by circuit aging and the prediction method at design stage. This paper describes a modeling methodology aiming at simulating the potential impact of circuit aging on its susceptibility to EMI. This approach is applied to explain the variation of the susceptibility level of a phase-locked loop (PLL) measured after a standard accelerated-life test. The first part of the paper presents the experimental characterization of the conducted susceptibility of a PLL before and after accelerated aging. In the next parts, the modeling and simulation approach are presented. The construction of a susceptibility model is based on circuit design information and measurements. This model takes into account the changes of transistor parameters induced by aging. In the final part, although precise models about degradation mechanisms are not available, this model is used to simulate the sensitivity of the PLL susceptibility and reproduce qualitatively the evolution of the susceptibility level after aging.

II. CHARACTERIZATION OF AGING-INDUCED SUSCEPTIBILITY LEVEL DRIFT

A. *Presentation of the case study*

The study proposed in this paper is focused on a PLL embedded in a test chip developed in the 0.25 µm SMARTMOS technology from Freescale Semiconductor (*Toulouse - France*), dedicated to automotive applications. Figure 1a presents the PLL schematic. The PLL is based on a first order filter, and made of three sub-blocks (phase detector, voltage-controlled oscillator (VCO) and frequency divider) which have separated power supply pairs. The VCO is a delay-controlled ring oscillator, designed to operate nominally at 112 MHz (Fig. 1b), the frequency divider divides by 4 the VCO frequency. The delay introduced by the delay cell depends on the gate voltages applied on the PMOS and NMOS transistors. In the actual implementation, only the PMOS gate voltage is controlled, the NMOS gate voltage is tied to the VCO power supply. The simplification of the VCO control makes the structure more sensitive to power supply voltage fluctuations. In the following tests, the frequency of the reference signal applied on PLL input is equal to 24 MHz.

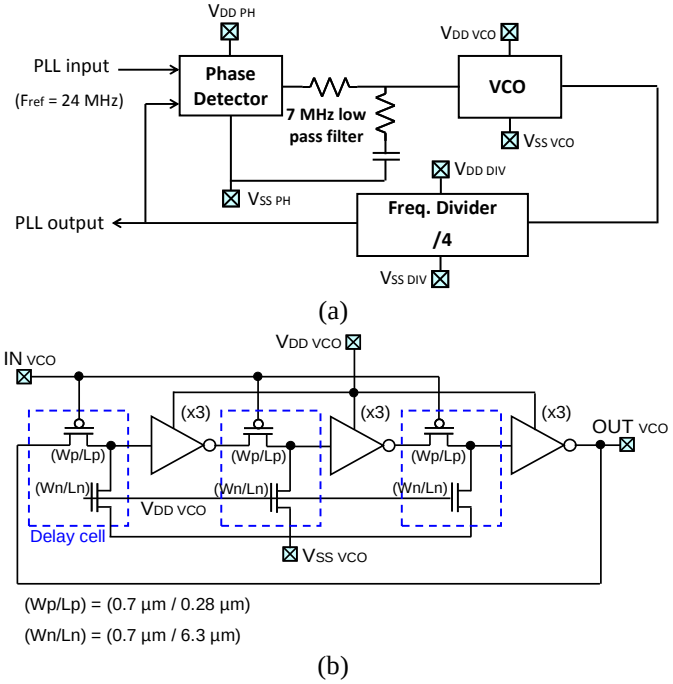

Figure 1. Schematics of (a) the PLL and (b) the delay-controlled VCO

The PLL power distribution network is unconventional but the separation of power supplies of each sub-block has been chosen to characterize internal coupling between different power supply domains and identify the role of each sub-block in the PLL susceptibility. The different power supply pairs are written V_{DD}VCO/V_{SS}VCO for the VCO, V_{DD}Ph/V_{SS}Ph for the phase detector and V_{DD}Div/V_{SS}Div for the frequency divider.

B. *Set-up description*

The methodology used to highlight susceptibility drift induced by circuit aging is described in Fig. 2. It consists in measuring the susceptibility to conducted disturbances before and after accelerated-life tests applied on a lot of 10 samples. This number of samples is certainly too small to obtain a precise evaluation of aging impact on susceptibility. However, it constitutes a good compromise to evaluate the trend induced by aging for a reasonable cost and test duration.

Accelerated-life tests are based on the acceleration of the damage rate for relevant wear-out failure mechanisms due to overstress conditions (e.g. high temperature or overvoltage) applied for a short period of time. In this test, the High Temperature Operating Life (HTOL) test has been chosen [7]. It consists in biasing a lot of several components or samples under overvoltage conditions at 150°C in a climatic chamber during 3 weeks.

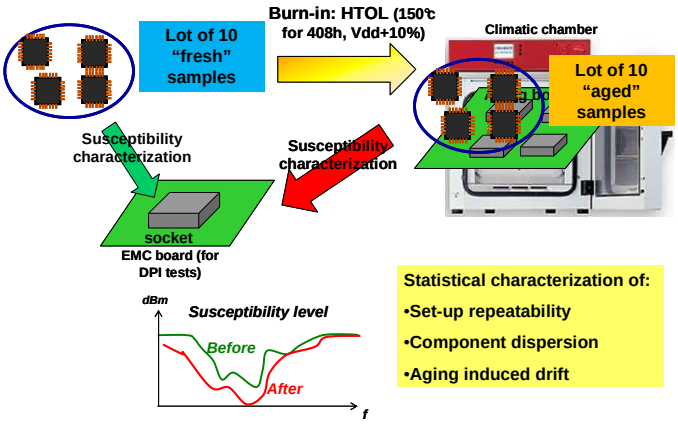

Figure 2. Experimental set-up for the characterization of the susceptibility level drift induced by accelerated aging

The PLL susceptibility is characterized according to the direct power injection (DPI) method defined by IEC 62132-3 standard [8]. This method is chosen because of its high level of repeatability. DPI test is based on conducted injection of harmonic disturbances applied on one or several pins of a circuit, which helps IC designers to evaluate the sensitivity at different frequencies of a pin or a block and locate the origin of immunity problems. The conducted disturbances represent the unwanted RF-energy coupled on cable harness and PCB tracks. The test consists in determining the magnitude of conducted RF-disturbances (i.e. RF forward power) to induce a component failure, such as an erroneous operation (e.g. bit error) or loss of nominal performances (e.g. reduction of noise margin, jitter or increase of current consumption). Figure 3 describes the DPI set-up used for the susceptibility characterization of the PLL.

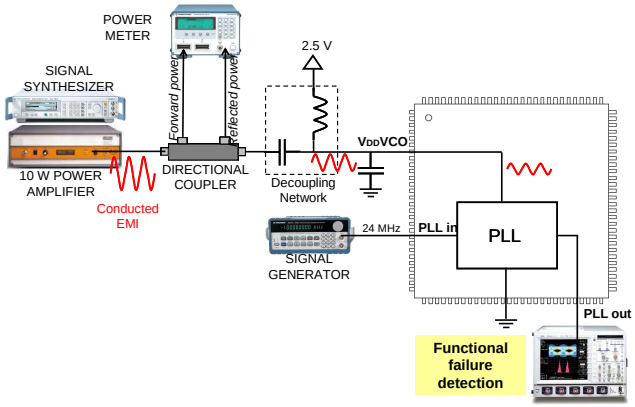

Figure 3. Conducted susceptibility test set-up based on DPI standard [8]

The PLL is very sensitive to power supply voltage fluctuations so conducted injections are performed either on VCO, phase detector, or frequency divider power supply pins. The harmonic disturbance injections are done between 10 MHz and 1 GHz. The maximum amount of disturbance is limited to 45 dBm because of power amplifier limitations. Voltage fluctuations coupled on VCO, frequency divider or phase detector power supplies are converted into timing jitter, which can affect the timing characteristics of PLL output signal or PLL stability. The PLL output period or period jitter is monitored by a digital storage oscilloscope (DSO). A maximum allowed deviation of PLL period has been set to 2 ns (i.e. 5 % of the nominal period) in order to limit the amount of power required during the susceptibility tests.

Several precautions are taken to ensure that the susceptibility level differences measured after accelerated life tests result only from circuit aging. First, all the susceptibility tests are done at ambient temperature and the power supply voltage is controlled. Secondly, the repeatability of DPI tests is measured before susceptibility tests on reference components to evaluate the uncertainties introduced by the DPI test bench. The evaluation of the repeatability is based on the repetition of the test on a reference sample and the computation of the standard deviation of the dispersion of the measurement results at each injection frequency. The repeatability of our DPI test bench is about

0.5 dB over the range 10 to 1000 MHz. Thirdly, only the circuit samples are aged since the samples are mounted either on EMC or aging test boards with specific sockets. Finally, the susceptibility tests have to be performed as soon as possible after the end of the accelerated-life test, in order to reduce the possible recovery of the samples from the aging-induced effects. As the complete susceptibility characterization of the ten samples lasts nearly one day, a partial recovery is likely but we will assume that this effect remains negligible.

C. Characterization of PLL susceptibility

First, the susceptibility of the PLL to conducted disturbances applied on VCO, phase detector or frequency divider power supply pins are compared. The susceptibility levels measured in these 3 tests performed on the same component are compared in Fig. 4.

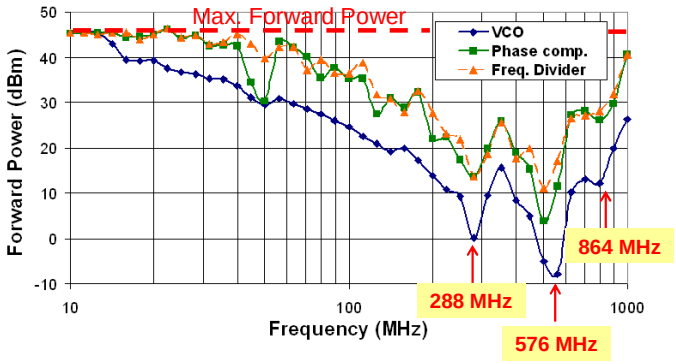

Figure 4. Conducted susceptibility of the PLL – injection on VCO, phase comparator and frequency divider power supply pins

While the susceptibility levels of the phase comparator and the frequency divider are similar, the susceptibility of the VCO is 10 to 15 dB higher. This difference demonstrates that the PLL is the most sensitive sub-block to conducted disturbances applied on the VCO power supply. The following study will be focused only on conducted injection on VCO power supply pin.

Two failure types are considered during DPI tests performed on VCO power supply: either the period jitter exceeds 2 ns or the PLL unlocks directly. The second mechanism occurs at high frequency (above 100 MHz), while the first mechanism occurs at low frequency and around particular frequencies: 288, 576 and 864 MHz. These three frequencies are respectively the third, sixth and ninth harmonics of the VCO operating frequency (96 MHz). Due to the VCO structure, synchronization between each delay cells of the VCO and the EMI happens at these frequencies and leads to a large increase of VCO jitter. The susceptibility threshold shape depends on three parameters:

- the board decoupling, which is the most efficient at 10 MHz
- the circuit power distribution network (PDN), which affects noise propagation within the circuit. The high susceptibility measured over the range 400 – 800 MHz is due the primary resonance of the VCO PDN which induces an efficient transfer of noise on VCO power supply [9].
- the VCO and PLL behaviors. The period jitter induced at the VCO and PLL outputs by a harmonic voltage fluctuation of the VCO power supply can be computed according to equations (1) and (2) [10]. The period jitter σ_T depends on the VCO frequency F_0, the pushing coefficient of the VCO K_{VCO}, the closed-loop response of the PLL G_{PLL}, the amplitude V_{EMI} and the frequency F_{EMI} of the voltage fluctuation. The analysis of equation (1) shows that the VCO converts efficiently the power supply voltage fluctuations into jitter in low frequency [10].

$$\sigma^2_{T\,VCO}(F_{EMI}) = \frac{1}{(2\pi F_0)^2}\frac{K_{VCO}.V_{EMI}}{2.(2\pi F_{EMI})^2}.\left|1-\exp(-j2\pi F_{EMI}T_0)\right|^2 \qquad (1)$$

$$\sigma_{T\,PLL} = \sigma_{T\,VCO} \times \left|G_{PLL}\right| \qquad (2)$$

D. Variation of the immunity level of the PLL induced by accelerated aging

At the end of HTOL test, the ten samples remain operational. The PLL is still locked in nominal conditions. No serious degradations or failures such as current consumption, signal integrity, I/O characteristics… can be noticed, except a variation of the free running oscillation frequency of the

VCO. The stress applied during HTOL test has accelerated degradation mechanisms which affect the properties of the VCO. The PLL does not go out of lock because the VCO is not enough degraded and the PLL is still able to compensate VCO changes.

However, the robustness of the PLL to external disturbances is affected. The comparison between DPI test results obtained before and after accelerated-aging show significant changes for conducted injection applied on VCO power supply pin. In Fig. 5, the conducted susceptibility levels of the 10 samples are superimposed before (a) and after (b) the accelerated-aging test.

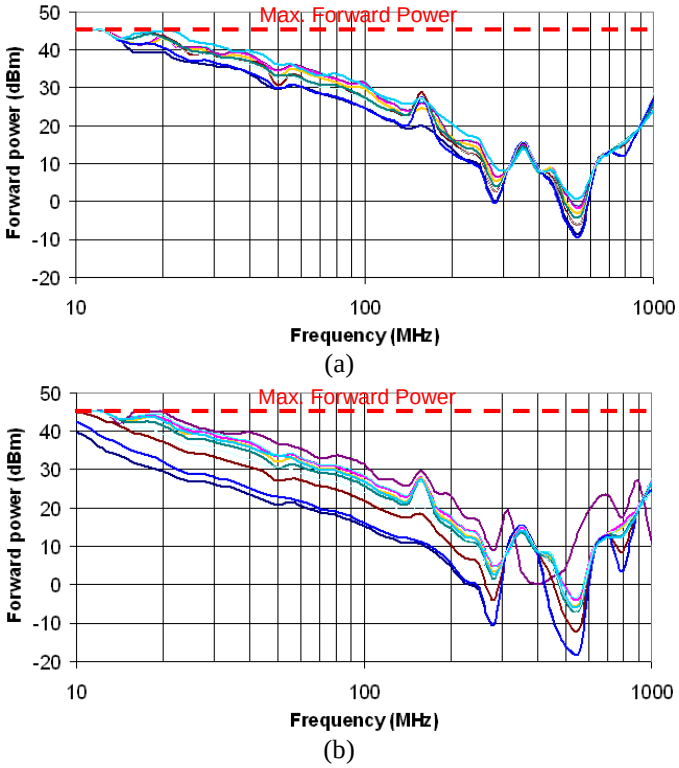

Figure 5. Superimposition of the conducted susceptibility levels of the 10 samples measured (a) before and (b) after accelerated-aging test

The susceptibility levels are randomly distributed at each injection frequency points due to circuit variability. The plot of the cumulative distribution function (CDF) of the immunity level measured at each frequency on the ten samples is similar to the CDF of a normal distribution. All the samples do not present the same immunity level before and after aging. Variations of several dB can appear between the different samples, which are larger than the DPI test bench repeatability. The comparison between results obtained before and after aging show clearly that the susceptibility level have evolved after aging. Three statistical analyses are performed to characterize these changes:

- the evolution of the average susceptibility level of the lot of 10 samples (Fig. 6)
- the evolution of the dispersion of the susceptibility level measured on 10 samples (Fig. 7)
- the average variation of the susceptibility level per sample (Fig. 8)

Fig. 6 shows that a reduction of 2.6 dB of the average immunity level occurs after aging over nearly all the frequency range. The internal degradations of the VCO induced during the accelerated aging test lead to a higher sensitivity to voltage fluctuations induced on VCO power supply. But all the samples do not follow the same evolution after aging, as shown in Fig. 8. For half of the components, a large variation is observed after aging over a large frequency range (the average reduction exceeds 2 dB for 4 samples and 1 dB for 2 samples). The worst case average reduction reaches up to 8 dB. It is interesting to notice that the components which suffer the largest reduction of susceptibility level were the most susceptible initially, and vice-versa.

Actually, it indicates that the susceptibility level dispersion has increased after aging. This trend is also confirmed by the results presented in Fig 7 which show the standard deviation of the susceptibility level distribution of the ten samples, before and after aging. A 3 dB increase of the variability of the susceptibility level is observed after aging. This effect could be linked to non uniform stress of the ten samples or a change of the DPI test bench with time. However, these hypotheses are unlikely because the temperature inside the climatic chamber is homogeneous and

the electrical stress conditions have been verified during the stress. Moreover, repeatability measurements on a golden reference sample prove that the characteristics of the DPI test bench are stable. In chapter V, the simulation results presented in Fig. 17 will provide a possible explanation about the increase of susceptibility level variability.

Contrary to all the other samples, the susceptibility level of sample 5 is slightly improved after aging. It is not likely that this opposite trend is linked to measurement errors or recovery from aging. Sample 5 is maybe a "lucky" component, in which the degradation mechanisms activated by stress conditions have made the PLL a little more robust to conducted EMI.

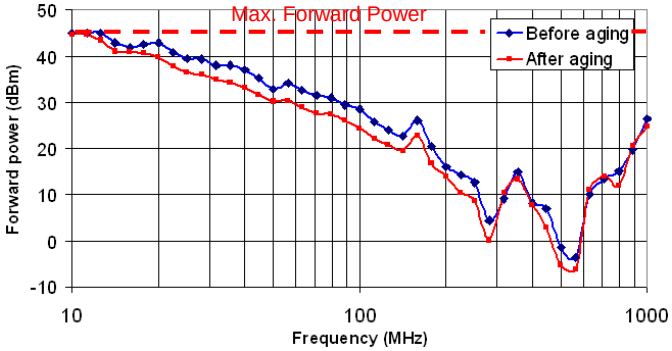

Figure 6. Evolution of the average susceptibility level measured on a lot of 10 samples before and after accelerated aging test

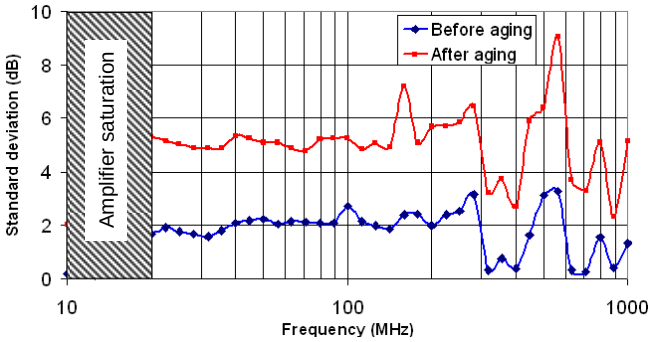

Figure 7. Evolution of the dispersion of the susceptibility level before and after accelerated aging test

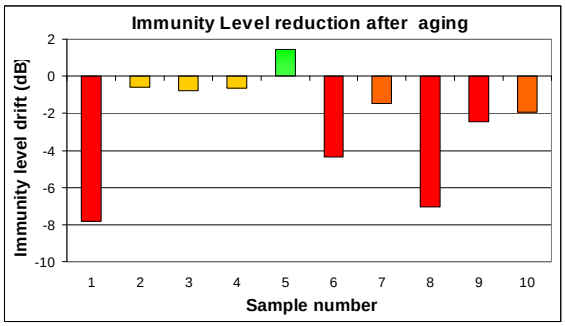

Figure 8. Average variation of the immunity level measured per sample

The reduction of the immunity level of the PLL can be correlated to the reduction of the free running oscillation frequency. This reduction is linked to the alteration of VCO characteristics induced by internal degradation mechanisms, which have been accelerated during the aging test. They have contributed to slow down the VCO and thus shift the capture range of the PLL. In nominal conditions, the degradations induced by aging are not large enough to lead to a failure of the PLL. However, they have seriously reduced the margin to voltage fluctuations and increased the susceptibility of the PLL to EMI. This trend could not be anticipated from susceptibility characterization of fresh samples. Only susceptibility measurements of aged components or CAD simulation could predict these variations. In the next part, a susceptibility model which takes into account VCO aging is proposed to explain the immunity degradation.

III. LONG-TERM IMMUNITY PREDICTION METHODOLOGY

Aging has a serious impact on VCO performances. Degradation mechanisms activated by harsh conditions of the accelerated-life test affect transistor parameters, and thus the circuit response and its susceptibility to EMI. The prediction of immunity level changes induced by aging relies on:

- a model able to simulate the susceptibility of the PLL to conducted disturbances
- a physical model of the VCO to simulate the impact of aging induced degradation mechanisms

A transistor based model will be used for the modeling of the VCO in order to integrate the effect of device aging, i.e. the degraded transistors can be identified and their characteristics can be changed according to an aging model. Figure 9 describes the proposed methodology to simulate the change of the immunity induced by aging [11]. Fresh and aged transistor models are included on device library, which can be extracted by device characterization, or by aging simulation. First, the susceptibility level of the "fresh" circuit is extracted. The circuit model only includes "fresh" transistor model. Secondly, an analysis of the circuit aging identifies which transistors are affected by degradation mechanisms and changes transistor models. Finally the susceptibility level of the "aged" circuit is extracted and compared to the level of the "fresh" circuit. In the following parts, the construction of the susceptibility model of the PLL is described.

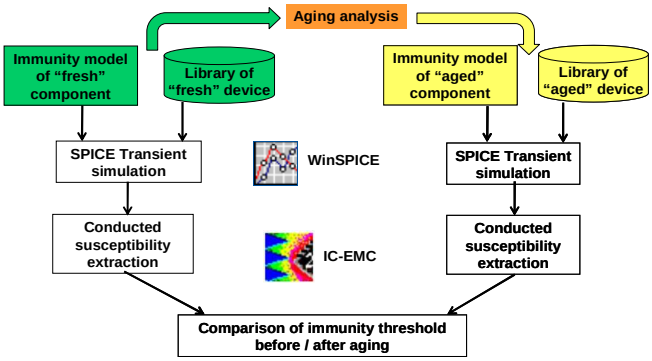

Figure 9. Long-term immunity prediction simulation flow

IV. PLL SUSCEPTIBILITY MODEL CONSTRUCTION

A. *Susceptibility model construction*

The structure of the PLL susceptibility model relies on ICIM standard proposal [12]. The model presents two parts:

- The Internal Behavior (IB) block which describes the nominal operation of the PLL and detects failures induced by coupling of EMI
- The Power Distribution Network (PDN) which describes the coupling path of the EMI to the sensitive nodes of the PLL. The PDN includes the DPI injection system, test board tracks, package and on-chip interconnects.

The IC model is finally inserted in the test bench model and the nearby environment (test board, decoupling, injection cables) is added.

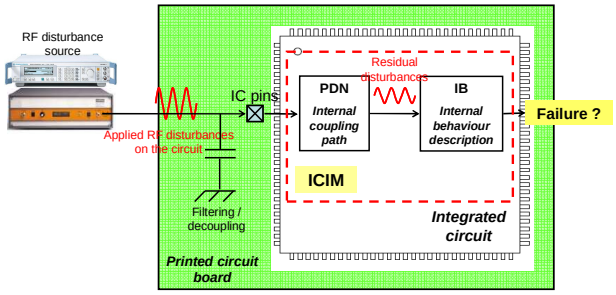

Figure 10. Structure of the susceptibility model of a circuit based on ICIM [12]

1) *Construction of the PDN block*

The PDN model of the PLL is an impedance network between the power and ground pins of the PLL sub-blocks. Each sub-block counts one power supply and two ground pins. Moreover, the PLL

input-outputs are biased by a dedicated power supply which can interact with the PLL PDN. Thus, the PLL PDN counts a total of 11 pins. A specific test board has been designed to extract the impedance network of the PLL PDN by 2-port S parameter measurements. The circuit is connected to a vector network analyzer (VNA) by high frequency GS probes (Fig. 11). Probes are connected to PCB pads placed as close as possible to the circuit under test. All the measurement configurations between each pin of the PLL PDN are possible, so package inductances, circuit equivalent capacitances, substrate coupling … can be extracted from measurements.

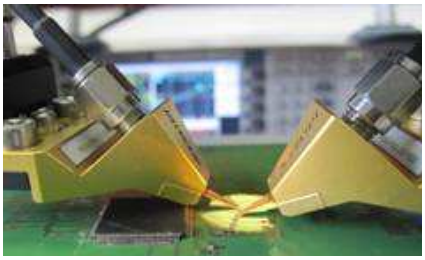

Figure 11. PLL PDN model extraction by S parameter measurements

Fig. 12 presents the PDN model extracted from S parameter measurements. Only the structure of the model and the name of the package terminals are given for legibility purpose. Fig. 13 presents comparisons between S parameter measurements and simulations obtained from the extracted model. The comparisons between measurement and simulation show a good agreement up to 1 GHz.

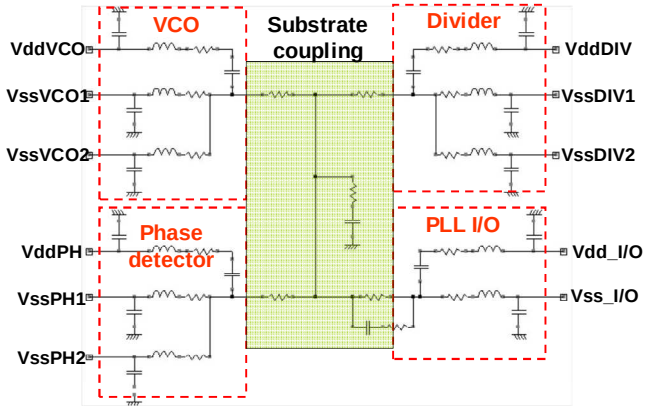

Figure 12. PLL PDN impedance model extracted from S parameter measurements

2) Construction of the IB block

The IB model construction relies on the transient simulation of the transistor level schematic of the PLL for two reasons:

- ensuring an accurate modelling of PLL failure mechanisms induced by VCO power supply voltage fluctuation
- including transistor degradation mechanisms by changing transistor model parameters

However, adding the PLL PDN and circuit nearby environment models can increase the simulation time. Parasitic inductances associated to board and package interconnects and decoupling capacitances induces a long transient state. The following methodology is used to overcome this issue. First, the voltage fluctuation amplitude applied on PLL terminals and required to induce a failure is simulated for different harmonic disturbance frequencies. As the PLL is extremely sensitive to VCO power supply voltage fluctuations, only the voltage fluctuation across this node is simulated.

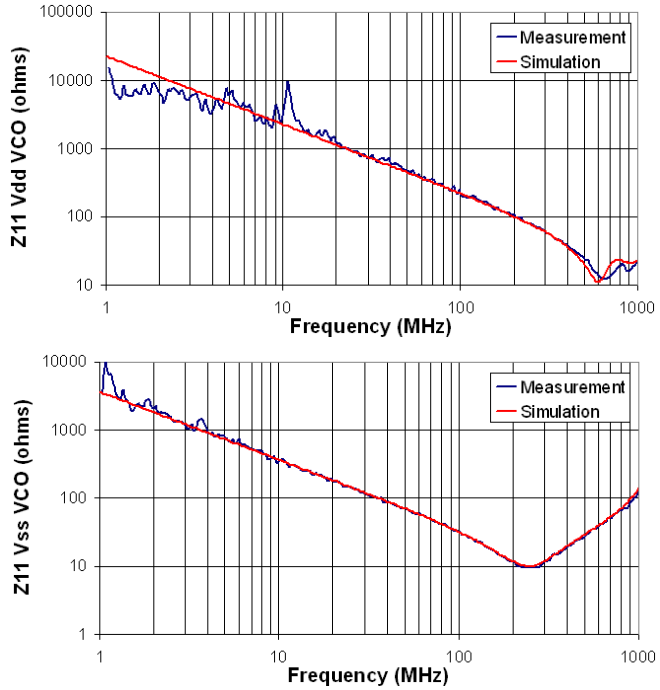

Figure 13. Examples of comparisons between S parameter measurements and simulation from the extracted model (Top: Z11 seen from V_{DD}VCO pin. Bottom : Z11between VssVCO pin)

Then, the voltage fluctuation levels are recorded in a sensitivity table (Fig. 14). In the ICIM model, the IB is replaced by a simple monitoring of the voltage fluctuation across the internal VCO power supply during the susceptibility simulation. At the end of the susceptibility simulation, if the voltage fluctuation induced by the EMI coupling is larger than the amplitude given by the sensitivity table, a failure is detected and the forward power of the disturbance is extracted.

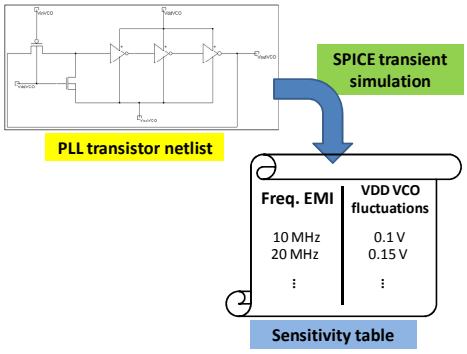

Figure 14. Generation of a sensitivity table: sensitivity of the PLL to VCO power supply fluctuations vs. EMI frequency

3) Validation of the PLL susceptibility model

The susceptibility model of the PLL includes the circuit PDN model extracted from S parameter measurements, the sensitivity level extracted from transient simulation of the PLL netlist and the model of the nearby environment (DPI test bench and test board). Fig. 15 presents the comparison between the simulation and the measurement of the susceptibility level of the PLL before aging. A good correlation is observed between 10 MHz and 1 GHz. The efficient EMI filtering around 10 MHz, the high susceptibility between 400 and 800 MHz, and the susceptibility peaks around 288, 576 and 864 MHz are simulated correctly. In spite of some discrepancies, the sensitivity of the PLL to conducted interferences is simulated correctly, so that this model can be reused for the simulation of aging impact on susceptibility.

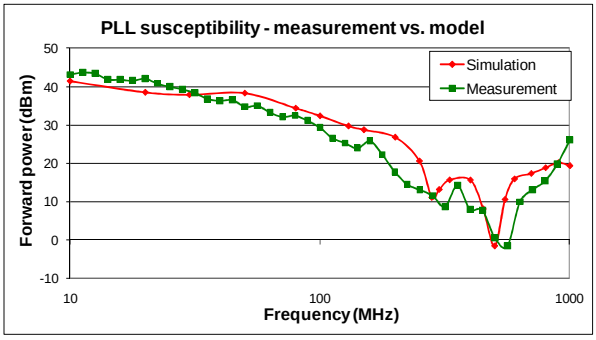

Figure 15. Comparison between measured and simulated susceptibility level of the PLL

V. SIMULATION OF THE IMPACT OF TRANSISTOR DEGRADATIONS ON PLL SUSCEPTIBILITY

A quantitative prediction of the effect of aging on susceptibility relies on the identification of critical transistors (e.g. based on electrical simulations or functional analysis) and the extraction of variation laws of transistor electrical parameters vs. stress conditions and time. In this case study, the absence of characterization of transistor degradations prevents from an accurate prediction of susceptibility level drift. In spite of the absence of experimental characterization, we can attempt to use CAD simulations to propose and consolidate assumptions about the origins of susceptibility increase. With CAD simulations, different scenarios of transistor degradation can be tested: the location of degraded transistors and device parameters affected by degradation mechanisms can be changed in order to observe the impact of the degradations of a specific transistor on the whole circuit susceptibility.

First, the most likely scenarios of transistor degradation have to be set, i.e. propose the location of degraded devices and device parameters affected by degradation mechanisms. Reliability publications report that transistor degradation mechanisms such as Negative Bias Temperature Instability (NBTI) or Hot Carrier Injection (HCI) can have a significant impact on circuit performances by increasing transistor threshold voltage Vth and altering carrier mobility U0 and drain current [3] [13] [14]. In the following analysis, we assume that threshold voltage and mobility are the only model parameters affected by aging.

Some assumptions can also be done about the location of degradations. The proposition of these assumptions can be based on experimental measurements or simulations. Experimental results have shown that the susceptibility increase is correlated with VCO slowing down so the degradation can be located on the transistors which have a major contribution on VCO oscillation frequency. The analysis of the VCO schematic presented in Fig 1.b shows that the oscillation frequency depends mainly on the delay cell characteristics. Degradation mechanisms such as NBTI or HCI can increase the channel resistance of the delay cell transistors and the delay. An electrical simulation of the voltages across each terminal of the delay cell transistors shows the PMOS gate is usually negatively biased compared to the source, which can accelerate NBTI mechanism. Moreover, as the PMOS transistor is shorter than the NMOS transistor, the delay is very sensitive to PMOS channel resistance length. Thus, we will assume that the degradation of the PMOS transistor is the origin of VCO slowing down and the increase of PLL susceptibility.

The relevance of the assumption about VCO degradation is now tested by the simulation of the VCO oscillation frequency. A degradation mechanism such as NBTI applied on the PMOS transistor of the delay cell decreases the carrier mobility and increase the threshold voltage. The variation of the VCO oscillation frequency is simulated for an arbitrary change on the carrier mobility and threshold voltage values. A change of 10 % on a transistor parameter is usually considered as a failure. Fig. 16.a presents the simulation of the VCO oscillation frequency for different power supply voltage, with nominal and degraded Vth and Uo for the PMOS transistor of the delay cell. Fig. 16.b presents the measurement of the VCO oscillation frequency measured before and after accelerated-aging test. In measurement and simulation, aging and degradation of the PMOS transistor of the delay cell lead to a reduction of the VCO frequency. The amount of frequency drift predicted in simulation depends on the variation of carrier mobility and threshold voltage.

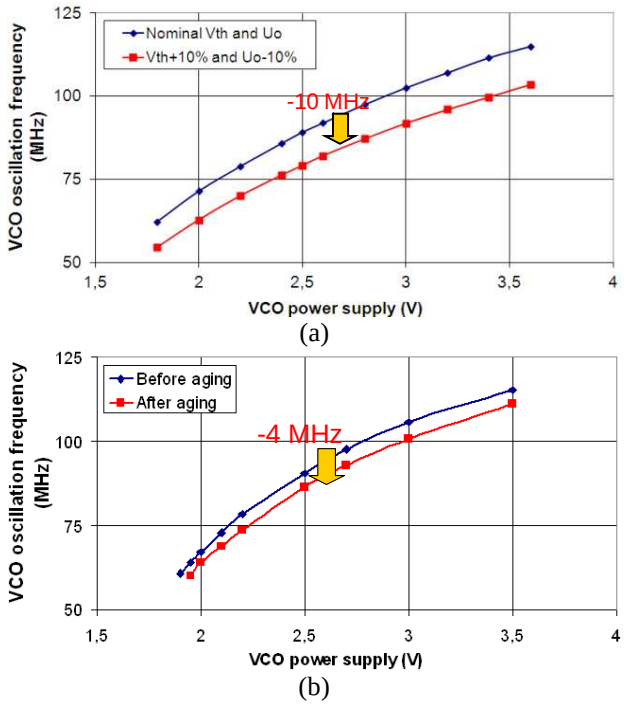

Figure 16. VCO oscillation frequency vs. VCO power supply before and after aging (a) simulation and (b) measurement

Based on the hypothesis of delay cell degradation, the effect on the PLL susceptibility is simulated. Fig. 17 presents the evolution of the immunity level at 550 MHz for different types of degradation: either the threshold voltage Vth is increased, or the carrier mobility Uo is decreased, or both parameters are changed. The amount of variation for Vth and/or Uo is marked X. In each case, transistor degradations lead to a reduction of the immunity level which reaches up to 6 dB, before a complete failure of the PLL in nominal operation (the PLL is unable to lock even without EMI). The result shows also that the delay cell is more sensitive to mobility change.

It is interesting to notice that the reduction of immunity level remains unaffected up to a certain amount of transistor degradation. Above this amount of transistor degradation, the immunity level starts falling rapidly. For example, if the variation of the threshold voltage is less than 20 % of the nominal value and the mobility remains constant, the reduction of immunity level is not significant (less than 1.5 dB). Above 20%, the immunity level reduction reaches up to 5 dB before a complete failure of the PLL. This simulation result can be compared to the experimental result presented in Fig. 8 which shows the average immunity level variation per sample. The measured susceptibility levels of the samples exhibit a large and increasing dispersion after aging. This simulation result can explain the larger dispersion of susceptibility level measured after aging. The relation between the variation of a transistor parameter (e.g. threshold voltage or mobility) and the reduction of the PLL susceptibility level is not linear. For a given dispersion of a transistor parameter, if this dispersion tends to shift and exceed a given level, the variability of susceptibility level will increase considerably.

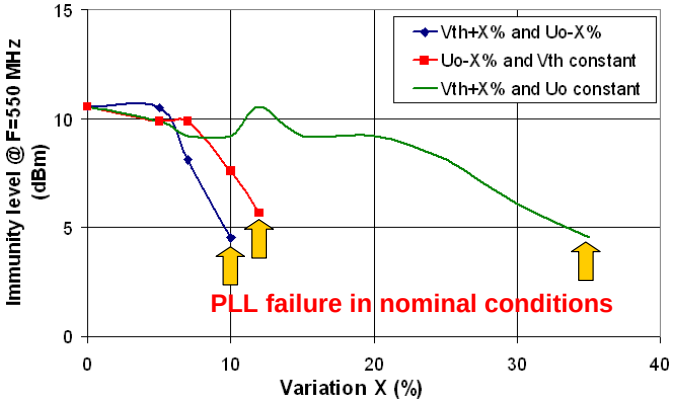

Figure 17. Analysis of the sensitivity of the PLL immunity level vs. variation of delay cell PMOSFET parameters

The worst case degradation scenario is now considered: the mobility is decreased while the threshold voltage is increased by 10% from their nominal value. The PLL susceptibility level is

simulated between 10 MHz and 1 GHz. Figure 18 presents the comparison between the simulated susceptibility level of fresh and aged PLL. The simulation predicts a global reduction of several dB of the immunity level over a large frequency range. This trend is similar to the immunity level decrease observed in measurement (Fig. 6). The degradation of the mobility and threshold voltage of the PMOS transistor of the delay cell is responsible for a large part of the reduction of the PLL robustness to conducted interferences. However, the immunity level decrease predicted in the worst case scenario is less than the measured variation: the simulation predicts an average reduction of the immunity level about 1.6 dB while the measured average reduction is about 3 dB. The maximum reduction reaches up to 6 dB in simulation and 10 dB in measurement. This difference can be explained by the insufficiency of the susceptibility model to simulate the impact of mobility and threshold voltage variations on the PLL performances. A better transistor model would certainly improve our immunity model.

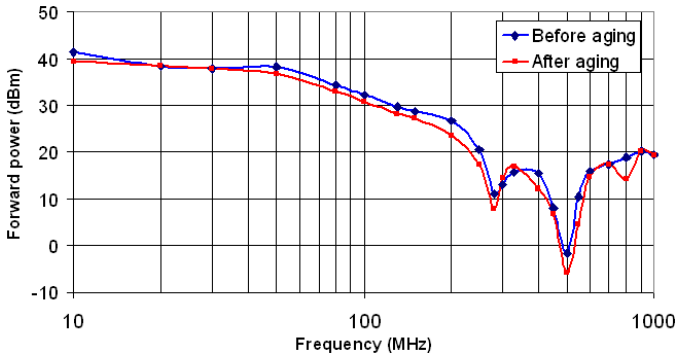

Figure 18. Comparison between the simulated susceptibility level of fresh and aged PLL

Even if the absence of internal reliability analysis and transistor degradation model prevents a complete validation of this degradation scenario and an accurate prediction of the variation of susceptibility level, the proposed model reproduces qualitatively the measured evolution of the susceptibility level of the PLL to conducted disturbances. The CAD analysis confirms that a degradation of threshold voltage and mobility of PMOS transistor of delay cell induced by a degradation mechanism such as NBTI can reduce the margin to power supply voltage fluctuations. An accurate quantitative prediction of the evolution of the susceptibility would rely on a characterization of degradation mechanisms which affects the transistors designed in this technology and the extraction of equivalent models to insert in the circuit schematic [15]. Moreover, failure analysis methods such as laser stimulation can help to locate precisely the root cause of susceptibility increase [16].

In addition to the aging effect, measurements have shown that the variability of the susceptibility level tends to increase after aging. The simulation results suggest that the variability of device parameters such as mobility and threshold voltage induces a dispersion of the susceptibility level according to a non linear relationship. Taking into account device variability issues, e.g. with Monte-Carlo simulations, is important to predict accurately the distribution of the susceptibility level variation and thus in which extent the robustness to EMI can be modified.

VI. CONCLUSION

This article has been focused on the issue of long-term susceptibility of integrated circuits, which relates to the changes of susceptibility to electromagnetic interferences induced by circuit aging. The long-term immunity has to be ensured at circuit design level to guarantee a high level of safety of the final electronic applications. This paper has presented a simulation methodology to predict the impact of circuit aging on conducted susceptibility. This method has been applied to model and explain the variation of susceptibility level of a phase-locked loop measured after an accelerated-life test. An electrical model of the PLL has been developed to predict the susceptibility level of the PLL to conducted disturbances coupled on the VCO power supply pin. A hypothesis has been proposed about the origin of the susceptibility level drift. The degradation of carrier mobility and threshold voltage of the PMOS transistor of the VCO delay cell slow down the VCO, modify the capture range of the PLL and thus increase the susceptibility. Including the change of transistor parameters in the susceptibility model has induced a similar reduction of immunity level as the measured one. The simulation predicts that the susceptibility of the PLL increases when the degraded transistor exceeds a given level. This effect can explain the large dispersion of susceptibility level drift measured after aging. Although the presented simulation results remain qualitative, the characterization and the accurate modeling of transistor degradation mechanisms will allow a quantitative prediction of susceptibility level drifts.

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