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Transport property study of MgO–GaAs(001) contacts for spin injection devices

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The electrical properties of Au/MgO/*n*-GaAs(001) tunnel structures have been investigated with capacitance-voltage and current-voltage measurements at room temperature with various MgO thicknesses between 0.5 and 6.0 nm. For an oxide thickness higher than 2 nm and for low bias voltages, the voltage essentially drops across the oxide and the structure progressively enters the high-current mode of operation with increasing reverse bias voltage, the property sought in spin injection devices. In this mode, we demonstrate that a large amount of charge accumulates at the MgO/GaAs interface in interface traps located in the semiconductor band gap. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2802727]

Electrical spin injection from a ferromagnetic metal into semiconductor structures is essential to realize functional devices based on spins in semiconductors.[1] In conventional ferromagnetic metal/semiconductor contacts, the large conductivity mismatch between the two materials prevents efficient spin injection.[2–4] However, spin injection can be achieved by a tunnel effect through a thin insulating barrier inserted between the ferromagnetic metal spin source and the semiconductor, as soon as the condition for efficient spin injection established by Fert and Jaffrès[4] is fulfilled. Although it was shown in recent studies that a CoFe/MgO tunnel spin injector can provide a high polarization of electrons in a GaAs based structure,[5] the fundamental mechanisms governing the current injection in this structure are not clearly understood so far. The purpose of this paper is to investigate the mode of operation and the electrical properties of Au/MgO/*n*-GaAs(001) tunnel structures. In particular, we show that these structures can enter the high-current mode of operation under applied reverse bias voltage (the spin injection condition) because it is possible to modify the charge accumulated in the trap states at the MgO/GaAs interface with the reverse bias.

Au/MgO/GaAs(001) structures were grown by molecular beam epitaxy (MBE). Some details about the preparation of the MgO/GaAs(001) samples can be found elsewhere.[6] In brief, 1.5 μm thick Si *n*-doped (4×10^{16} cm^{-3}) GaAs buffer layers were first grown on n^+-GaAs(001) substrate using standard MBE conditions. The MgO layers between 0.5 and 6 nm were then deposited at room temperature (RT) by the evaporation of high purity MgO powder at approximately 0.06 nm/min under an O_2 atmosphere of 5×10^{-7} Torr on an As-rich GaAs(001)-(2×4) surface. Finally, the 30 nm thick Au metal contacts of 250, 350, or 500 μm in diameter were deposited *in situ* at RT from an effusion cell using a shadow mask. The capacitance-voltage (*C-V*) measurements were carried out using a HP4284 *LCR* meter with a sinusoidal voltage amplitude of 30 mV and a frequency between 20 and 1 MHz, and the current-voltage (*I-V*) measurements were obtained using a Keithley K617 electrometer. All *C-V* and *I-V* characterizations were made in the dark and at RT.

Figure 1 shows measured current density–voltage (*J-V*) characteristics for various MgO thicknesses. As can be seen in Fig. 1, for an oxide thickness of 1.5 nm, the structure shows a rectifying behavior. This indicates that the voltage drop takes place mainly across the semiconductor depletion layer, as in intimate metal/semiconductor contacts, and that the barrier height under bias Φ_B (Φ_B is defined as the energy difference between the GaAs conduction band minimum at the MgO/GaAs interface and the Fermi level in the metal under bias) weakly evolves with the applied voltage (V_a). From an analysis of the *J-V* characteristic in the forward direction using thermionic model, we obtain a zero-bias barrier height of 0.65 eV and an ideality factor of 1.12. The ideal factor near unity indicates that thermionic emission is the dominant mechanism in this structure.[7] Upon increasing the oxide thickness, we observe that the rectifying characteristic progressively disappears. For instance, for an oxide thickness of 3.9 nm, the structure progressively enters a high-current mode of operation with increasing reverse bias voltage (under −1 V, a high reverse current density of about

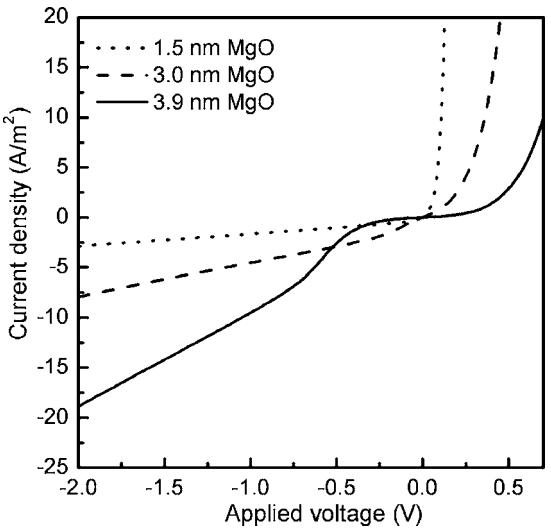

FIG. 1. *J-V* curves measured at RT for MgO thicknesses of 1.5, 3.0, and 3.9 nm.

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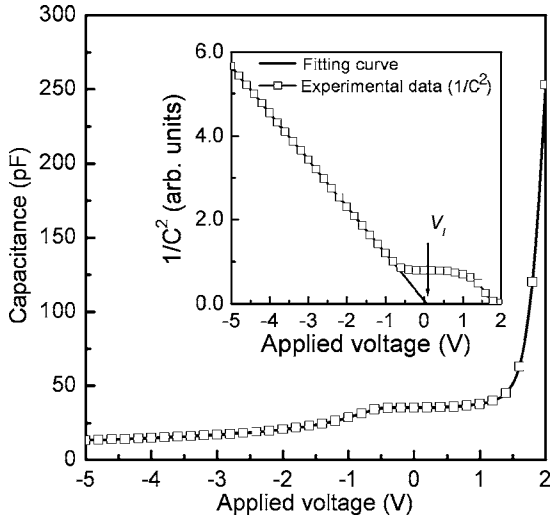

FIG. 2. High-frequency (1 MHz) *C-V* curve measured at RT with a voltage sweep rate of ~0.1 V/s for an MgO thickness of 3.9 nm and a Au contact of 250 μm in diameter. The inset shows the corresponding $1/C^2$ curve compared to the linear fitting curve in the deep depletion regime ($V_a < -0.7$ *V*). V_I is the voltage intercept of the extrapolated $1/C^2$ curve with the voltage axis.

10 A/m^2 is obtained). This result suggests that the presence of the MgO layer causes a reduction in barrier height Φ_B with the increasing reverse bias voltage. It is interesting to note that due to the reduction of Φ_B, the reverse current density of the structure with 3.9 nm MgO thickness may actually be greater than that of the structure with 1.5 nm MgO thickness. For reverse bias voltages higher than 0.7 V, the *J-V* curve is linear indicating that the structure operates in the Ohmic mode with a differential resistance of 0.1 Ω/m^2. Although the reverse current density strongly increases in reverse bias due to the reduction of the barrier height, the condition for efficient spin injection as calculated by Fert and Jaffrès for a metal/semiconductor/metal structure is still not fulfilled.[4] The interface contact resistance is indeed too large by five orders of magnitude.

To obtain further information on the mode of operation of the metal/oxide/semiconductor (MOS) structure, we have performed capacitance measurements. Figure 2 shows the *C-V* characteristic at 1 MHz for MgO thickness of 3.9 nm. No detectable hysteresis effects were observed in the *C-V* loops taken with voltage sweep rate going up to 2 V/s, which means that the structure operates in the steady-state mode.[8] Considering that the interface traps do not respond to the alternative excitation at 1 MHz, the total capacitance is a series combination of the oxide capacitance (C_{OX}) and the semiconductor capacitance (C_{SC}). As long as the structure does not enter the accumulation mode, the C_{OX} value is much larger than the C_{SC} value and, consequently, the measured capacitance is essentially that of the depletion layer in GaAs. To calculate the C_{OX} value, we have considered the geometric capacitance of the MgO layer with a relative dielectric constant of 8.0.[9]

The *C-V* curve in Fig. 2 exhibits an almost flat step between −0.7 and 1.0 V, which indicates that the depletion width is only weakly changed in this voltage range. At $V_a = 0$ V, the estimated band bending, using depletion approximation, is 0.7 eV. In fact, the large plateau in the *C-V* curve can be interpreted as being caused by trap states located at the MgO/GaAs interface in the band gap of GaAs. This interpretation was proposed to explain the presence of similar plateau in *C-V* curves of MOS capacitors.[10] Let us assume that the interface trapped charges are in equilibrium with the semiconductor, where the quasi-Fermi level is flat and are located in the semiconductor band gap at the interface. As the bias voltage decreases, the quasi-Fermi level at the MgO/GaAs interface moves toward the valence band maximum. When interface states cross the quasi-Fermi level, they become empty (by emission and/or recombination processes), and, consequently, the interface charge is changed. Thus, if the interface trap distribution is continuous in the band gap of the semiconductor and presents a high density, a slight change in semiconductor band bending causes a large modification of the charge density at the interface. Such a plateau region can also be observed for MOS structures operating under strong-inversion conditions. However, in this case, we expect a capacitance value (at high frequency) per unit area of 5.3×10^{-4} F/m^2. The measured value (per unit area) at zero-bias voltage is larger (7.1×10^{-4} F/m^2), excluding the formation of an inversion layer at the interface, in our case in the voltage range of the plateau.

Since the current density injected in the semiconductor through the MgO barrier is high in the forward direction and as the oxide capacitance is only known with a large error, it is then difficult to obtain an accurate estimate of the distribution of the interface traps density (D_{it}) using the conductance or capacitance methods.[11] However, using the conductance method we have obtained between 0.1 and 0.3 eV above the GaAs midgap a D_{it} value of about 4×10^{13} states/cm^2/eV, which is a rather large value.

Let us now discuss the *C-V* characteristic for the large negative bias voltages ($V_a < -0.7$ V). The capacitance increases with the applied voltage and the corresponding $1/C^2$ vs V_a curve (inset of Fig. 2) is a straight line. The value of the doping concentration deduced from the slope of the curve agrees well with that of the GaAs buffer layer, and the intercept of the straight line with the voltage axis gives a Φ_B value of 0.1 eV.[12] From these observations, it is clear that for large negative bias voltages, a nonequilibrium deep depletion mode occurs. Indeed, at thermal equilibrium, in the strong-inversion mode, the capacitance should be constant. The absence of the inversion charge in the valence band of the GaAs can be related here to the long response time of the minority carriers in GaAs and the high reverse current density in the structure.[13] These results also show that in this regime, the barrier Φ_B does not evolve significantly with the applied voltage, and the voltage drop across the MgO layer remains mainly constant: the further decrease of the bias voltage falls entirely over the GaAs depletion layer.

The fact that Φ_B remains constant for applied voltage below −0.7 V can be explained as follows:[14] for $V_a < -0.7$ V, the tunnel current becomes high enough so that the electron injection from the metal to the interface trap states compensates any increase of positive charge in these states. As a result, it is not possible to accumulate more positive charge in the interface states for higher reverse bias voltages.

Under (sufficiently large) reverse bias voltages, the linear dependence of the $1/C^2$ vs V_a curves has been observed for the whole range of oxide thicknesses, showing that the MOS structures operate under depletion or deep depletion mode. In Fig. 3(a), we show the evolution of the Φ_B value extracted from these curves[12] as a function of the MgO thick-

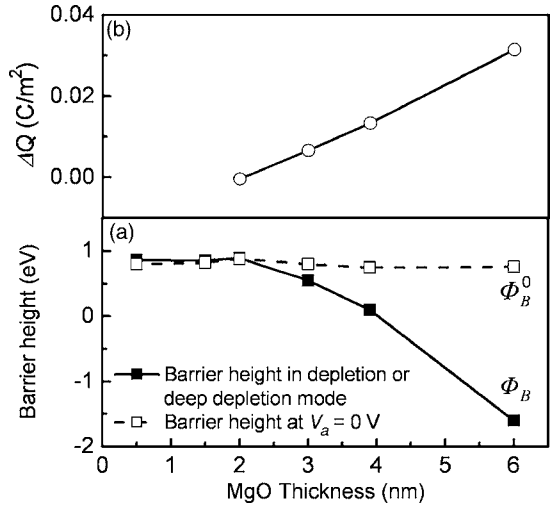

FIG. 3. (a) Evolution of Φ_B and Φ_B^0 as a function of the MgO thickness. Φ_B (Φ_B^0) corresponds to the barrier height under depletion or deep depletion mode (for the nonpolarized structure). (b) Evolution of the additional positive charge per unit area ΔQ accumulated in the interface traps [$\Delta Q = C_{OX,A}(\Phi_B^0 - \Phi_B)/e$, where $C_{OX,A}$ is the oxide capacitance per unit area and e is the elementary charge].

ness. The barrier height value for the nonpolarized structure Φ_B^0 is also presented in Fig. 3(a). As can be seen, no significant difference between Φ_B and Φ_B^0 for MgO thicknesses lower than 2 nm appears. This means that the voltage drops almost entirely across the semiconductor, as already deduced from the analysis of the *J-V* characteristics. Here, the interface states are probably in equilibrium with the metal and no significant charge can be accumulated at the MgO/GaAs interface under reverse bias voltage. For oxide thicknesses higher than 2 nm, the difference between Φ_B^0 and Φ_B increases with the oxide thickness, which demonstrates that the maximum voltage drop across the MgO layer also increases. Figure 3(b) shows the corresponding evolution of the additional positive charge per unit area ΔQ accumulated in the interface traps. In fact, as observed in Fig. 3(b), the probability of charge exchange between the metal and interface traps diminishes with increasing MgO thickness and, consequently, the ΔQ quantity increases.

In summary, we have studied the electrical properties of the Au/MgO/GaAs(001) (*n* type) structure using *C-V* and *I-V* measurements at RT. For oxide thickness higher than 2 nm, our results show a clear evidence of the presence of a large density of trap states at the MgO/GaAs interface ($\sim 4.10^{13}$ states/cm^2/eV). Although the structure does not operate under strong-inversion or accumulation conditions, we observe a large voltage drop across the MgO layer with the change of the applied voltage. We demonstrate that this behavior is caused by the charge accumulation in the interface traps. As a result of this voltage drop across the MgO layer, a strong increase of the current injection into the semiconductor structure can be observed with increasing reverse bias.

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