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Architecture Level TSV Count Minimization Methodology for 3D Tree-based FPGA

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***Abstract*—The CMOS technology scaling has greatly improved the overall performance and density of Field Programmable Gate Array (FPGA), nonetheless the performance gap between FPGA and ASIC has remain very wide mainly due the programming overhead of FPGA. Three-Dimensional (3D) integration is a promising technology to reduce wire lengths. Through Silicon Vias (TSV) provide electrical connectivity between multiple active device planes in 3D integrated Circuits (ICs). TSVs require a significant silicon area compared to planar interconnects and also bring critical challenges to design of 3D ICs. In this paper we propose an architectural level TSV count optimization solution to minimize the TSV count without compromising the chip performance. The experimental results shows we are able to minimize 40% of TSV count in 3D Tree-based FPGA.**

I. Introduction

The 3D integrated circuit (IC) technology has emerged as one of the most promising solutions for overcoming the challenges in interconnection and integration complexity in modern circuit designs [2]. TSV is the key enabling technology element for 3D integration, which is currently being actively evaluated as a potential solution to reduce the interconnect delay and increase the logic density in FPGA. In some recent studies shows that in Mesh-based FPGAs, 40%-80% of overall design delay and 90% of the chip area are attributed to programmable routing resources [1]. It has also reported that in Mesh-based FPGA, as much as 80% of the total power consumption is associated with routing resources. Considering the area, delay and power consumption overhead, the programmable routing resources is the key design element in FPGA design. In this paper we discus an innovative design methodology to minimize the TSV count of 3D Tree-based FPGA architecture.

II. 3D Tree-based FPGA Architecture

In a Tree-based FPGA architecture [4], The Logic Blocks (LBs) are grouped into clusters located at different levels. Each cluster contains a switch block to connect local LBs. The switch blocks are divided into Mini switch Blocks (MSB). As illustrated in Figure 1, the Tree-based FPGA architecture unifies two unidirectional upward and downward interconnection networks using a Butterfly Fat-Tree topology to connect Downward MSBs (DMSB) and Upward MSBs (UMSB) to LBs inputs and outputs. A 3D interconnection network architecture for Tree-based FPGA presented in [4]. As illustrated in Figure 1, in a Tree-based FPGA architecture, the programmable interconnects are arranged in a multilevel network with the switch blocks placed at different tree levels. In the 3D interconnect network organization, a horizontal *break point* introduced between tree level 3 and 4 based on the interconnect delay optimization. In the 3D design process, the logic blocks along with local programmable interconnects belong to tree levels 0 to 3 are placed in layer 1 and programmable interconnects belong to tree levels above the break point are placed in active layer 2 and interconnected using TSVs. A symbolic horizontal break point shown in Figure 1.

The inter-layer vias (TSVs) are to be limited because they are large in size compared to the minimum feature size on the die. While the finest vias currently available are about 4μm diameter with a pitch of about 8μm [5]. Although the design engineers are trying to reduce the TSV dimensions, the minimum feature size on the die is also shrinking. Therefor the TSVs are expected to remain larger than the wire dimensions in metal layers within the die. Thus TSV count has to be minimized. In [7] a 3D place and route (TPR) was presented, to investigate the wire length and delay associated 3D Mesh-based FPGA. TPR [7] is flexible on deciding the number of TSVs compared the horizontal channels, however all switch blocks are assumed to be 3D may lead to large number of unused TSV resources, which increase manufacturing cost.

III. TSV Count Optimization

Considering the programmable interconnect overhead, FPGA is an ideal device that can benefit significantly by 3D integration, in which the circuits are integrated vertically by stacking multiple dies together and interconnected using TSVs [2]. Since FPGA is an interconnect dominated device, it is essential to minimize the TSV count because the TSVs consume more silicon area than horizontal interconnects. The TSV count optimization is performed using Rent's parameter [6] p defined for a Tree-based architecture shown in equation 1. The Tree level is represented as ℓ and k is the cluster arity, c is the number of in/out pins of an LB and IO is the number of in/out pins of a cluster located at level ℓ. A *2 level* Tree-based FPGA with rent value p=0.73 is illustrated in Figure IV. For upward and downward network, reduction in the number of inputs at level ℓ impacts level $\ell+1$, since the number of inputs at level $\ell+1$ is equal to the number of inputs at level ℓ. The optimization of upward and downward networks based on Rent's parameter [6] is done as follows

$$IO = c.k^{\ell.p} \tag{1}$$

A. The Downward Network Model

A cluster situated at level ℓ contains $N_{in}(\ell-1)$ DMSB, where $N_{in}(\ell)$ is the number of inputs of cluster located at

level ℓ with k outputs and $\frac{N_{in}(\ell)+kN_{out}(\ell-1)}{N_{in}(\ell-1)}$ inputs, whereas k is also the cluster arity size. Since DMSBs are full crossbar devices, the total number of switches at level ℓ cluster is $k(N_{in}(\ell)+kN_{out}(\ell-1))$. At each level ℓ, $\frac{N}{k^{\ell}}$ clusters, whereas N is total number Logic Blocks and the total number of switches or interconnects in the downward network is

$$\sum_{\ell=1}^{\log_k(N)} k \times N \times \frac{N_{in}(\ell) + kN_{out}(\ell-1)}{k^{\ell}} \quad (2)$$

Following equation 1, we can simplify the number of outputs of a Logic Block is $N_{out}(0) = c_{out}$ and the number of inputs equal $N_{in}(\ell) = c_{in}.k^{\ell.p}$ and $N_{in}(\ell-1) = c_{out}.k^{(\ell-1)p}$ and so on. The total interconnects used at each level ℓ can be calculated by equation 3.

$$N_{switch}(down) = N \times (k^p c_{in} + kc_{out}) \times \sum_{\ell=1}^{\log_k(N)} k^{(p-1)(\ell-1)} \quad (3)$$

B. The Upward Network Model

Similar to the downward interconnect network. The upward interconnect network also built using a *Butterfly-Fat-Tree* network topology. In level ℓ every cluster contains $N_{out}(\ell-1)$ UMSBs with k inputs and outputs. UMBSs are also full crossbar devices with $k^2 \times N_{out}(\ell-1)$ switches at a level ℓ cluster. There are $\frac{N}{k^{\ell}}$ clusters at each level ℓ, and the total number of upward interconnection block is

$$\sum_{\ell=1}^{\log_k(N)} \frac{k^2 \times N}{k^{\ell}} \times N_{out}(\ell-1) \quad (4)$$

$N_{out}(0) = c_{out}$ is the outputs of Logic Block and using equation 1, $N_{out}(\ell-1) = c_{out}.k^{(\ell-1)p}$. The total number of interconnect required for the upward interconnect network is calculated using equation 5

$$N_{switch}(up) = N \times k \times c_{out} \times \sum_{\ell=1}^{\log_k(N)} k^{(p-1)(\ell-1)} \quad (5)$$

The total number interconnects in Tree-based FPGA architecture is

$$N_{switch}(Tree) = N \times (k^p c_{in} + 2kc_{out}) \times \sum_{\ell=1}^{\log_k(N)} k^{(p-1)(\ell-1)} \quad (6)$$

The TSV count minimization methodology is developed using Rent's parameter based iterative negotiation based on 3D Tree-based FPGA router [4] program. The aim is to find the best tradeoff between device routability and interconnect requirement of each MCNC application. TSV optimizer considers the same architecture with different rent parameter "p" values to find the minimum number of TSVs required to implement each application netlist. The 3D TSV optimizer router program as illustrated in Figure IV select the horizontal break point level of tree interconnect and optimize the number of TSVs required between layer 1 and 2 of the 3D stacked Tree-based FPGA illustrated in Figure IV. Once it finish the break point level, the TSV optimizer choose the other level above or below the break point level of the tree-based FPGA architecture, which could be either in active layer 1 or 2 to optimize the required interconnect in the upward and downward interconnection network. The 2 layer 3D stacked Tree-based FPGA architecture used for 3D TSV optimization illustrated in Figure IV. The Logic Blocks and local interconnects upto tree level 0 to 3 were placed in layer 1 of the stacked 3D chip.

Table I presents The TSV count optimization and performance analysis results of 3D Tree-based FPGA. An average reduction of 40.1% TSVs and an average speed degradation of 4.7% recorded in these experiments. A similar experiment on 3D Mesh-based FPGA for reduction of 30% TSV resulted in 6.47% degradation in performance as illustrated in Figure IV. Table II present the Tree-based FPGA architecture level interconnect optimization results and area estimation. The results reported in Table II represent the average of 21 large MCNC benchmark circuits. Compared to 3D Mesh-based FPGA, the 3D Tree-based with TSV interconnections save $\approx$ 30% interconnect area and 53% performance improvement. Using our Rent based optimization methodology, the programmable interconnect overhead is reduced 63.4%. These experimental results confirm that 3D is a consistent architecture to build high density and high performance FPGA, which is unlikely to be attained in Mesh-based FPGA architecture.

IV. Conclusion

A systematic TSV count optimization methodology for 3D Tree-based FPGA presented. The issues associated with TSV size and count and its impact on design and manufacturing of 3D integrated circuits studied and presented. The study reveals the management of TSVs in a 3D stacked chip is essentials for guaranteed performance and yield. The architecture level methodology adopted based Rent parameter shows a performance degradation of 4.7% for a corresponding reduction of 40.1% TSVs. This result places 3D Tree-based FPGA as a viable alternative to build 3D re-configurable systems compared to 3D Meash-based FPGA.

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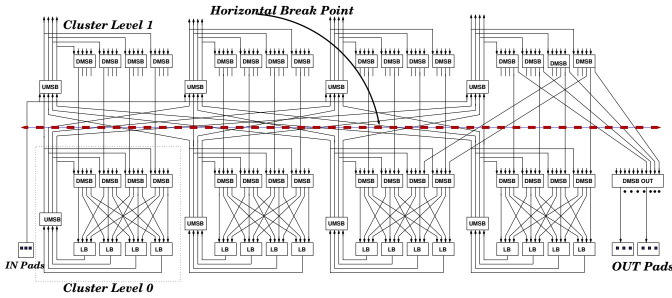

Fig. 1. A 2 level Tree-based Multilevel FPGA interconnect: Upward and Downward Interconnection network

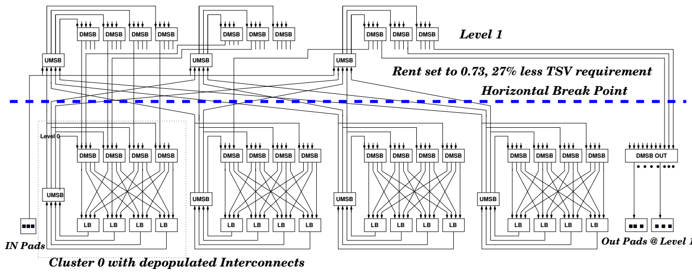

Fig. 2. Vertical interconnect (TSV) depopulation using Rent's rule(*level 1* with p=0.73)

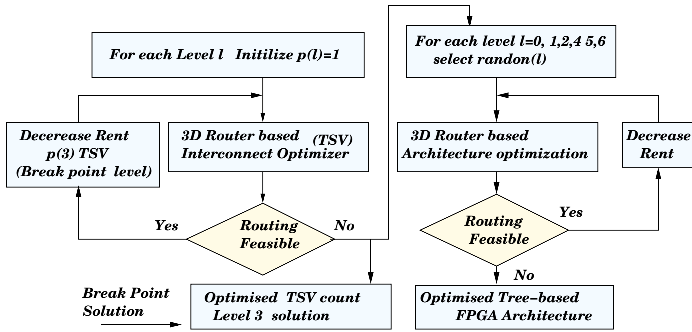

Fig. 3. 3D Router based TSV count optimization methodology

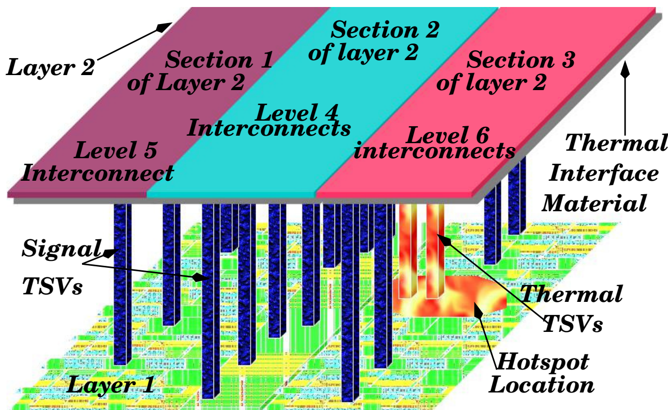

Fig. 4. 2 layer 3D Tree-based FPGA experimental structure used for TSV count Optimization

TABLE I. 3D TREE-BASED FPGA TSV COUNT OPTIMIZATION RESULTS AND PERFORMANCE DEGRADATION ANALYSIS

	Tree Levels=7, Arity=4, Arch=4x4x4x4x4x4x4				
		Speed Performance			Rent=p
Circuits MCNC[a]	Optimized Rent=p	Rent=1 2D (nS)	Rent=1 3D (nS)	Rent=p 3D (nS)	Speed degrade(%)
alu4	0.47	59.9	25.81	26.97	4.5
apex2	0.51	80.4	30.92	32.84	6.2
apex4	0.61	76.4	31.83	32.18	1.1
bigkey	0.60	79.1	20.19	20.90	3.5
clma	0.58	198.0	59.48	62.45	5.1
des	0.56	90.8	28.83	30.01	4.1
diffeq	0.66	62.6	26.66	27.86	4.5
dsip	0.65	61.9	19.78	20.59	4.1
elliptic	0.66	107.0	42.78	44.23	3.4
ex1010	0.55	143.1	45.42	47.01	3.5
ex5p	0.58	168.2	41.42	43.53	5.1
frisc	0.62	118.6	42.82	45.13	5.4
misex3	0.64	67.4	24.94	26.39	5.8
pdc	0.59	143.9	45.86	47.60	3.8
s298	0.55	130.8	45.81	48.93	6.8
s38417	0.65	75.46	30.69	32.38	5.5
s38584	0.62	118.0	40.51	42.33	4.5
seq	0.61	64.6	24.59	25.94	5.5
spla	0.58	109.6	38.29	40.28	5.2
tseng	0.65	131.1	45.79	48.31	5.5
ava	0.63	206.2	111.21	117.10	5.3
average	0.59	109.18	31.22	41.09	4.7

[a]http://er.cs.ucla.edu/benchmarks/ibm-place.

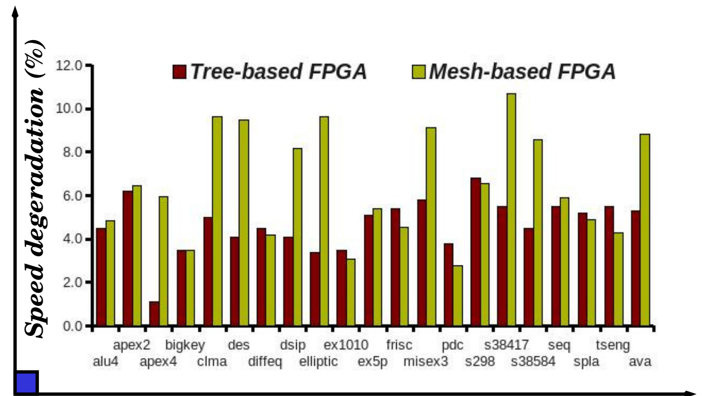

Fig. 5. Speed degradation comparison of 3D Tree-based FPGA and 3D Mesh-based FPGA

TABLE II. ARCHITECTURE OPTIMIZATION RESULTS

Tree Levels=7	Arity=4, Arch=4x4x4x4x4x4x4		
Architecture Levels	3D Chip Layer	Optimized Rent 'p'	Optimized Area μm^2
Logic Blocks	Layer 1	–	93635273
Switch Level 0	Layer 1	0.67	2412
Switch Level 1	Layer 1	0.54	10800
Switch Level 2	Layer 1	0.66	37496
Switch Level 3	Layer 1	0.59	232128
$BreakPoint_{Hori}$	Horizontal Break Point		
Level 3 to 4	TSV Area=40192μm^2		
Switch Level 4	Layer 2	0.67	814440
Switch Level 5	Layer 2	0.66	45553499
Switch Level 6	Layer 2	0.65	38145463