SiC Vertical JFET Pure Diode-Less Inverter Leg

Rémy Ouaida, Xavier Fonteneau, Fabien Dubois, Dominique Bergogne, Florent Morel, Hervé Morel, Sébastien Oge

SiC Vertical JFET Pure Diode-Less Inverter Leg

Rémy Ouaida[1,2], Xavier Fonteneau[1], Fabien Dubois[1], Dominique Bergogne[1], Florent Morel[1]
Hervé Morel[1], Sebastien Oge[2]

[1] Laboratoire Ampère UMR CNRS 5005
Université de Lyon - INSA de Lyon
21 avenue Jean Capelle
69621 Villeurbanne CEDEX, France
remy.ouaida@etu.univ-lyon1.fr

[2] THALES Microelectronics
CAP BRETAGNE - Z.A. Le Piquet
35370 ETRELLES
sebastien.oge@fr.thalesgroup.com

***Abstract*—The aim of this paper is to investigate the ability of a vertical structure JFET to operate in an inverter leg without any internal or external diode. The JFET is characterized to show the reverse conduction capability while the gate-to-source voltage is lower than the threshold voltage. An inverter leg is tested at 540 V /5 A and 50 kHz. A specific test board is implemented to assess a safe operation over a period of time.**

***Index Terms*—Silicon Carbide, Vertical JFET, Diode Less, Inverter Leg**

I. Introduction

Power SiC JFETs have been available for some time now and have gained extreme popularity. This paper deals with a specific aspect of using JFETs in inverter legs: in [1] the authors propose to operate the JFETs without using any diode, –hence the DiodeLess expression– by utilizing a specific control sequence and resonance during switching. Very recently, in [2], the contributors propose to use a Vertical JFET (VJFET) without any diode or peculiar gate control timing. The possibility to reduce component count at no expense on the control circuit is very attractive indeed. This paper describes an experimental power converter implementing such a technology.

A. Inverter legs, freewheeling diodes

Power electronics is often introduced by the concept of the inverter leg, a basic circuit that is used to build more complex structures. It is a circuit made of the association of switches, which connects an electrical power source to another circuit, for example an induction motor. Figure 1 presents the structure of an inverter leg. The switches can be seen as ideal switches: either closed or open. The switching process takes place between a voltage source and a current source linked together [3]. To control the power flow, the converter structure has to be able to open that link. One major consequence is that the current flow must be routed instantaneously to a closed circuit, the phenomenon is called freewheeling. Freewheeling is mandatory and is solely achieved by using a self-controlled switch: the diode. This electronic component, whatever the temperature, the rate of variation of the current or the parasitic elements of the circuit, automatically turns on in order to switch the current source. This is why inverter legs implement

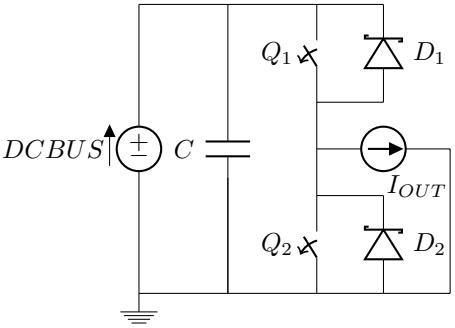


Fig. 1. Structure of an inverter-leg

diodes for freewheeling and controlled switches to set the output voltage.

Sometimes the controlled switches are build in such a way that an internal diode is naturally present within the device and can be used as a freewheeling diode. When it is not the case, the designer has to add an external diode to ensure the freewheeling action as in [4], or to integrate it on the same die as proposed in [5].

B. SiC Vertical JFET

For the SiC JFET devices, there are two different structures [6]: the vertical channel structure JFET [7] and the two channels structure JFET [8], [9]. The two channels structure [10] has an internal body diode that can be used as a freewheeling diode in an inverter leg. For the vertical channel structure from Semisouth, a simplified cross section the VJFET structure, inspired by [2], is shown in figure 2. In this figure, it can be observed the absence of a source-drain body diode. A more detailed fabrication process and electrical characteristics can be found in [11]. Here, a brief description is presented.

Operating principle of the power JFET is modulation of the channel depletion region through the applied gate-to-source voltage. If the gate-to-source voltage (V_{GS}) is higher than the gate threshold voltage, the JFET begins to conduct and a current can be established in the channel. The gate threshold voltage is the boundary between the conduction and the blocking area. Currently two vertical JFET structures have been developed. The one used the principle of the depletion mode mainly known as the normally-on JFET and the second

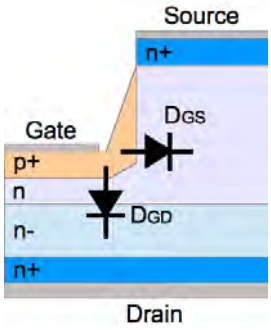


Fig. 2. Cross section of a half-cell of a VJFET showing the internal diodes, P-N junctions, as described in [2]. The channel between drain and source is composed by one semiconducting material. Thus, there is no body diode

one, the JFET normally-off, is using the enhancement mode. In this paper the inverter leg is composed of normally-on SiC JFETs. In a normally-on device, a 0V gate-to-source voltage allows current to flows in the channel and a gate-to-source voltage below the threshold voltage turn off the JFET.

In this paper the authors explore a specific property of the VJFET that makes possible an inverter leg operation without diodes, even a body diode, hence the name: Pure Diode Less (PDL).

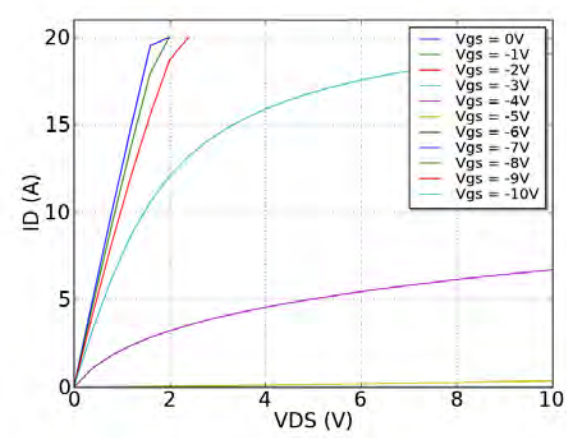
C. Dead-time

In an inverter leg, two switches in series are connected to a voltage source. This implies to prevent any conduction of both devices at the same time. Because switching is not instantaneous and its duration is subject to variations, a break before make operation has to be implemented; it is called dead time [12]. In a classic configuration, during dead times, both controlled power switches are turned off and the current flow takes place through the freewheeling diodes. It is shown in this paper that, in a PDL inverter leg, a current may flows through the VJFETs from Source to Drain even during the dead-time when both gate to source voltages are negative. It is then mandatory to focus on the electric characteristics of the VJFET in direct and reverse conduction.

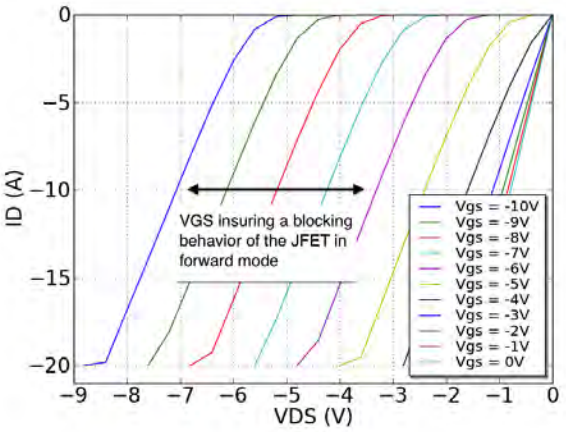
This paper presents the possibility of a converter to operate without internal or external diode (Pure Diode Less). Section II, presents the static characteristics of a SiC normally-on VJFET in a direct and reverse conduction. Section III explains the principle of an diodeless inverter-leg operation. A demo board has been developed and tested to validate the PDL operation. Section IV presents the result of this demo board. Moreover, the power losses are discussed in section V. Section VI concludes this paper and opens perspectives to the future works.

II. Static Characterizations

Direct and reverse static characterizations of the vertical JFET from Semisouth, SJDP120R085 [13], were performed at room temperature using the Curve Tracer Agilent B1505A.



(a)



(b)

Fig. 3. Static characterizations of JFET (a) in forward mode and (b) reverse mode at room temperature for different gate to source voltages.

For positive values of the drain current, $I_D(V_{DS})$ characterization results for various gate-to-source voltages are plotted in figure 3a. In this mode, the drain current I_D is modulated by the gate-to-source voltage. For positive values of the drain-to-source voltage V_{DS} it can be observed that the VJFET is fully turned-off when the gate-to-source voltage is lower than -6 V (threshold voltage).

In figure 3b, the reverse static characterizations for various gate-to-source voltages are plotted. Gate voltage is referenced to the source, while the drain-to-source voltage is driven in negative. The figure shows that a reverse current could pass through the channel if a negative voltage between drain and source is sufficiently high even though the gate-to-source voltage is lower than the threshold voltage. It can be seen that different values of V_{GS} allow a blocking of the VJFET in forward mode. The device behaves like a diode with a threshold voltage, which depends on the value of the gate-to-source voltage.

The next section shows that this behavior can be used to obtain a freewheeling path without diode.

III. Diodeless inverter leg principle

This section introduces the principle of the Pure Diode Less (PDL) mode in an inverter leg.

A simplified schematic of the inverter leg consisting of two JFETs and the load (inductor and resistor) is illustrated in figure 4. It is possible to divide the PDL operation into four distinct steps. For each step, the path of the load current is plotted in red. This study is done for a positive output current. When the current becomes negative the observed phenomenon are the same on the other switch.

A. Step 1: Q1 with $V_{GS1} = 0V$ & Q2 with $V_{GS2} < V_{TH}$

The high switch (Q1) is in the on state while the low switch (Q2) is in the off state. So, a current flows through the high VJFET in direct conduction. This current depends of the nature of the load. The voltage across the load is considered equals to the bus voltage (since the one state resistance is low) such as the drain-to-source voltage across the low switch (Eq. 1).

$$V_{DS2} \approx V_{DCBUS} \approx V_{LOAD} \tag{1}$$

B. Step 2: Q1 with $V_{GS1} < V_{TH}$ & Q2 with $V_{GS2} < V_{TH}$

Switch Q1 is turned-off while Q2 is still driven at the off state in order to protect the inverter leg from a short circuit (dead time). During this state, a path for the load current is necessary. The drain potential in the low device is floating, therefore the potential decrease due to the inductance. The decrease of the drain-to-source voltage (V_{DS2}) allows current to flow in the channel even if the gate-to-source voltage (V_{GS2}) is lower than the threshold voltage. As show the characteristics in figure 3, the drain-to-source voltage in the low device is set by the current flowing in the load and the value of the gate-to-source voltage applied when the JFET is turned-off. V_{PDL} is the value of the voltage across the low device during the dead time.

C. Step 3: Q1 with $V_{GS1} < V_{TH}$ & Q2 with $V_{GS2} = 0V$

The gate-to-source voltage in the low side device equal to 0 V, drives the JFET in conduction. The load current continues to flow through the channel. But the channel does not behave as presented in step 2 (diode) because the gate-to-source voltage has been changed. For a $V_{GS2} = 0\,V$, it can be observed on the characteristics in figure 3 that the power channel is similar to a resistance.

The drain-to-source voltage in the device Q2 is equal to the on state resistance multiplied by the value of the load current. However this voltage is closed to 0V due to the small value of the one state resistance. This negative voltage is called V_{COND}.

D. Step 4: Q1 with $V_{GS1} < V_{TH}$ & Q2 with $V_{GS2} < V_{TH}$

This step is necessary to turned-on the high side JFET (Q1). This step is similar to the step 2 corresponding to the second dead time.

The PDL mode has been described and the four steps show that PDL mode in an inverter leg is possible.

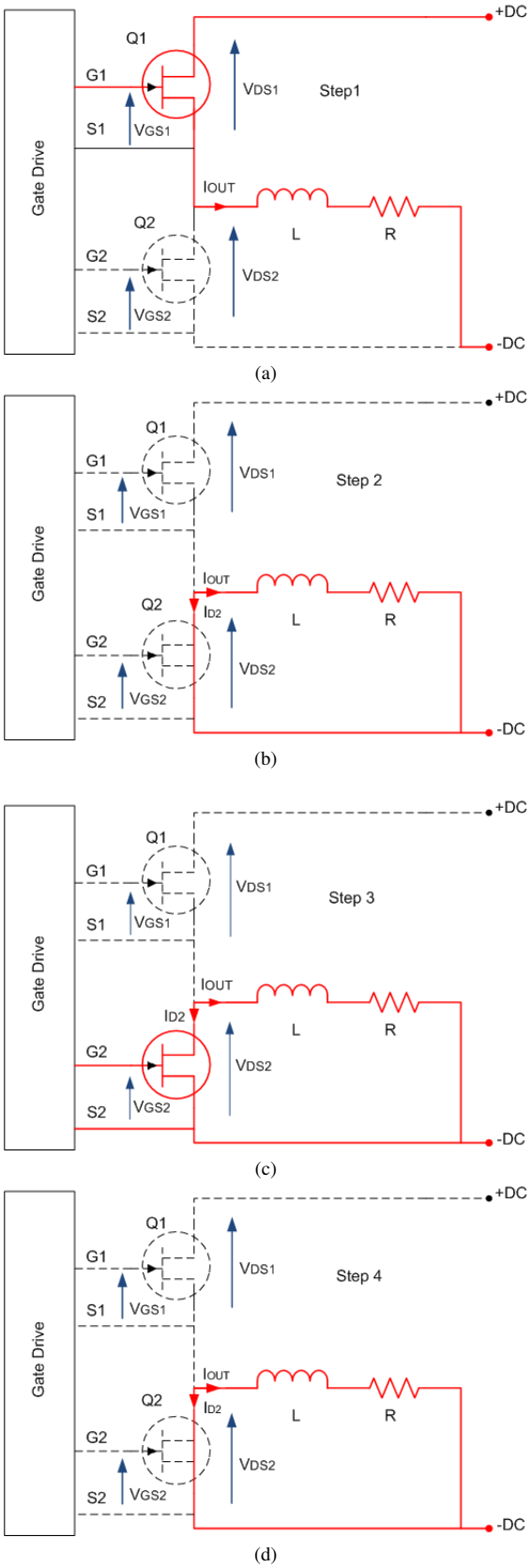


Fig. 4. Circuits schematics of an inverter leg for each steps which divides the PDL mode

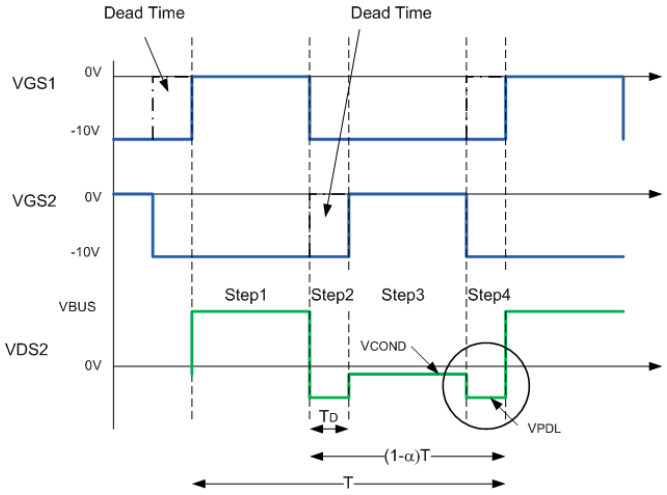


Fig. 5. The four steps of a pure diode less inverter leg

Table I. Most significant values of the demo board

Parameters	Values
Gate bias (V_{GS}) [V]	-10 / 0
Gate resistor [Ω]	22
Dead Time [us]	1.5
DC bus [V]	540
Switched current [A]	5

Figure 5 resumes the four steps by plotting different voltages signals on a switching period. This figure shows the gate-to-source voltage in the two devices and the drain-to-source voltage in the low side VJFET.

IV. Experimental validation

To demonstrate the PDL operation, an inverter leg has been built. The test is performed at 50 kHz switching frequency, 540 V bus voltage (i.e corresponding to airborne applications [14]) for several loads up to 2 kW, for many hours, in DC static operation. Table I resumes electrical parameters of the tested PDL inverter leg. The dead time is set to 1.5 μs in order to have a large PDL time for the sake of the experiment. Practical values for the dead time of a SiC JFET inverter leg is in the 100 ns to 500 ns range. Devices are turned off with a gate-to-source voltage equal to -10 V. This characterization is plotted in figure 6.

The picture 7 shows the experimental PDL inverter leg. VPSU is a variable power supply to set the correct voltage on the gates drivers. GtDr H and GtDrV L are the high side and low side gate drivers. The current in the low side VJFET is sensed by a T&M Research precision shunt. A high frequency resistive probe was implemented, Rprobe, to sense the gate voltage. The voltage source of the PDL inverter leg is supported by the association of MKP film and electro-chemical capacitors, DCBcaps. The load is connected placed at a remote place. The PWM signal comes from an external generator while the dead time is made by an on-board delay circuit. The VJFETs are not visible as they are directly connected across

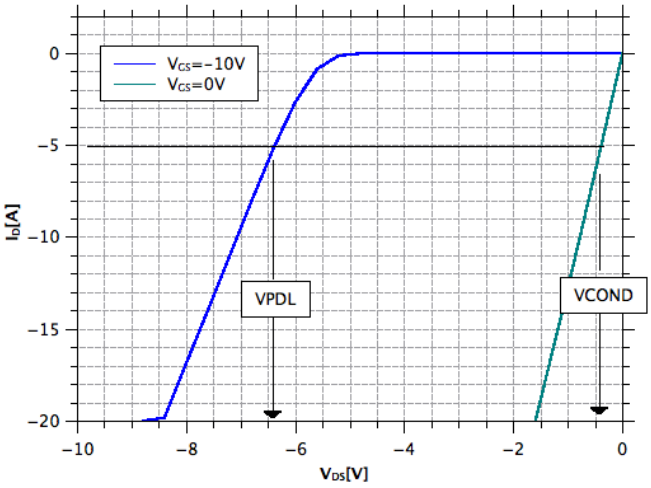


Fig. 6. Reverse static characterizations of a VJFET. For $I_D = -5\,A$ and $V_{GS} = -10\,V$, $V_{PDL} \approx -6.5\,V$. For $I_D = -5\,A$ and $V_{GS} = 0\,V$, $V_{COND} \approx -400\,mV$.

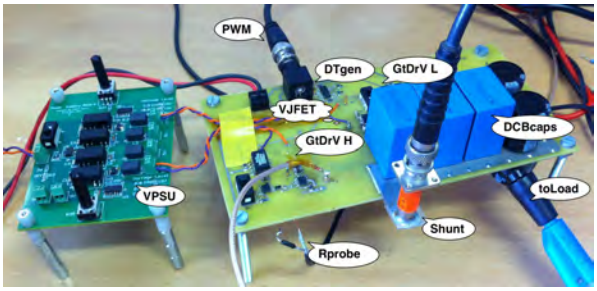


Fig. 7. Picture of the test board using two JFETs beneath the printed circuit board ($P_{OUT} = 2\,kW$ in continuous operation test at 50 kHz)

the voltage source, beneath the capacitors, on the copper side of the printed circuit board.

The first results on the inverter leg without external or internal freewheeling diode are presented in the figure 8. The low device drain-to-source voltage and the gate-to-source voltage are plotted. It can be seen that the V_{DS} in the low device is equal to the bus voltage (540 V). On this figure, the drain current in the low side VJFET is plotted. It can be observed that this drain current is null when the high side VJFET is turned-on (step 1). When the high device is turned-off and the low device is turned-on (step 3), a negative current flows in the channel ($I_{OUT} = 5\,A$).

In order to show the different steps described in PDL inverter leg principle, the figure 9 is an enlargement of the drain-to-source voltage in the low device during dead time. In addition to the V_{DS2}, the gate-to-source voltage are plotted to understand when the low JFET is turned-off. The steps 3, 4 and 1 are presented on the graph. In this paper, during step 3 the voltage drop when the low device is turned-on is called V_{COND} and it corresponding to the low device conduction. The data sheet of the JFET gives an on-state resistance of 85 mΩ at room temperature. With a reverse load current of

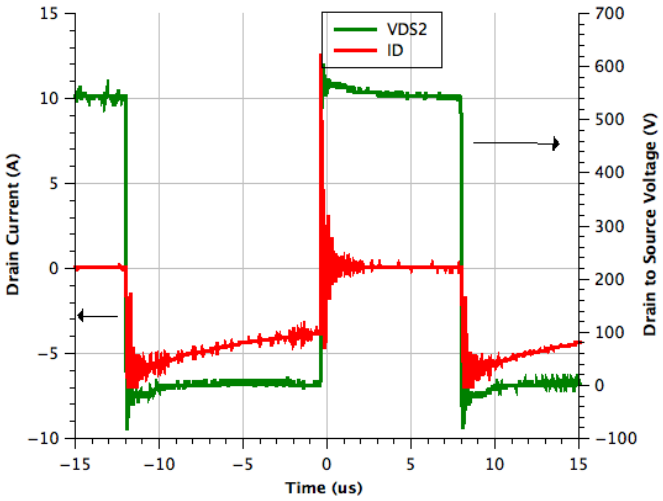


Fig. 8. Drain-to-source voltage and drain current in the low side device for a input voltage of 540 V at 50 kHz with a load current of 5 A

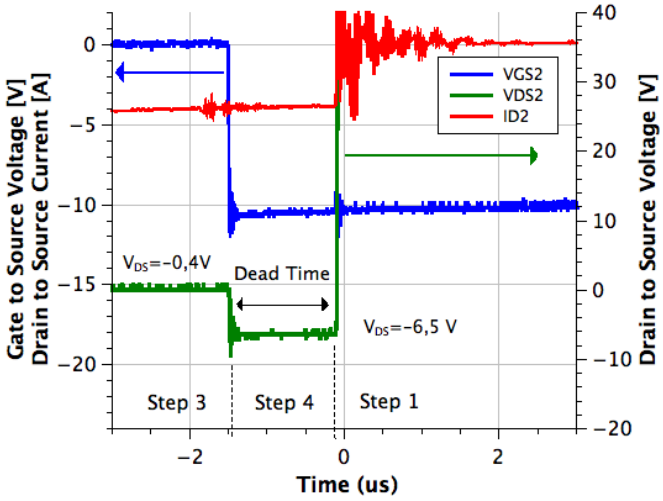


Fig. 9. Waveforms for dead time of 1.5 μs at 50 kHz, 540 V and 25 °C

5 A, the voltage drop is 425 mV. As previously described, the drain-to-source voltage is null.

During the step 4, both devices are turned-off, this is the dead time. The gate-to-source voltage (-10 V in this experiment) shows a bias lower than the threshold voltage (≈-6 V for the considered VJFET). It can be observed that V_{DS} is equal to -6.5 V during dead time. The drain current is fixed by the load and it flows in reverse. It has been measured that the drain current during this phase is equal to -5 A. On figure 6, a current of -5 A forces a drain-to-source voltage of -6.5 V. This value is similar to the experiment. It can be seen that the gate-to-source voltage remains constant during dead time. In step 1, the low device still is turned-off while the high device becomes turned-on. The drain-to-source voltage in the low device is equal to the bus voltage (540 V). The previous theoretical study is validated by the experiment that proves the PDL mode is possible.

V. Discussion

The PDL operation leads to decrease of the number of components. This is an interesting feature for industrial converters, cost is reduced and reliability is increased.

However during the dead time in the PDL mode, the reverse conduction in the vertical JFET introduces a voltage drop higher than the voltage drop produced by an external freewheeling diode in a classic inverter leg mode. This increase of voltage drop produces more power losses for a given current. Finally power losses have to be taken into account to validate the benefit of the PDL inverter leg mode. As a first evaluation, the power losses in Q_2 when Q_1 is blocked can be estimated by equation 2. This equation is defined according to the drain-to-source voltage in the low device during the dead time (V_{PDL}), the drain-to-source voltage during the conduction (V_{COND}), the duty cycle (α), the period (T), the frequency (f) and the dead time (T_D).

$$P_{PDL} = P_{DT} + P_{SWITCH} \tag{2}$$

With:

$$P_{DT} = f.(2.V_{PDL}.T_D.I_{OUT})$$
$$P_{SWITCH} = f.(V_{COND}.I_{OUT}.((1-\alpha)T - 2.T_D))$$

On equation 2, it can be seen that the PDL mode associated losses depend on the duration of the dead time. However the absence of freewheeling diodes reduces the parasitic capacitance of the power switch. This should contribute to the reduction of the switching losses. PDL mode should be advantageous when the increase of the conduction losses is balanced-out by the reduction of the switching losses. Estimation and measurement of power losses, including switching losses, is a very complex task where the component properties and the circuit parasitics have a major impact. So, a specific study on losses has to be carried out in order to discuss the relevance of the PDL mode in inverters applications.

The elimination of the diode impacts voltage rise times, high speed current variations… then conducted and radiated noises will change. Rise times, fall times and oscillations during the switching process are known to create perturbations in the MHz frequency range [15]. Filtering is not easy at these frequencies and a higher level of perturbations would lead to a more expensive and bulky filter. Therefore, switching waveforms, with and without diode, should be studied in-depth from the EMI point of view.

VI. Conclusion

It has been demonstrated that a vertical JFET can be used in an inverter leg without external freewheeling diodes thanks to the reverse conduction propriety. Experimental work validates the preliminary study of the Pure Diode Less Inverter Leg. Removing the freewheeling diode leads to a reduction of the cost of converters. However the power losses during the dead time increase. This extra losses depend principally on the value of the gate-to-source voltage. Also the EMI impacts has still to be quantified.

Future works would be dedicated to the physical understanding of the reverse properties of the vertical JFET.

REFERENCES

[1] B. Ållebrand and H.-P. Nee, "On the choice of blanking times at turn-on and turn-off for the diode-less SiC JFET inverter bridge," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Graz, Austria, Aug. 2001.

[2] D. Sheridan, K. Chatty, V. Bondarenko, and J. Casady, "Reverse conduction properties of vertical SiC trench JFETs," in *Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium on*, june 2012, pp. 385 –388.

[3] N. Mohan, T. Undeland, and W. Robbins, *Power electronics: converters, applications, and design*, ser. Power Electronics: Converters, Applications, and Design. John Wiley & Sons, 2003, no. vol. 1. [Online]. Available: http://books.google.fr/books?id=ToYoAQAAMAAJ

[4] H. Zhang, L. Tolbert, J. H. Han, M. Chinthavali, and F. Barlow, "18 kW three phase inverter system using hermetically sealed SiC phase-leg power modules," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, feb. 2010, pp. 1108 –1112.

[5] R. Radhakrishnan and J. Zhao, "Monolithic integration of a 4H-silicon carbide vertical JFET and a JBS Diode," *Electron Device Letters, IEEE*, vol. 32, no. 6, pp. 785 –787, june 2011.

[6] A. Lemmon, M. Mazzola, J. Gafford, and K. Speer, "Comparative analysis of commercially available silicon carbide transistors," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, feb. 2012, pp. 2509 –2515.

[7] M. Mazzola, J. Casady, N. Merret, I. Sankin, W. Draper, D. Seale, V. Bondarenko, Y. Koshka, J. Gafford, and R. Kelley, "Assessment of normally on and quasi on SiC VJFET's in half-bridge circuits," *Material Science Forum*, vol. 457-460, pp. 1153–1156, 2004.

[8] H. Morel, Y. Amieh, D. Tournier, R. Robutel, F. Dubois, D. Risaletto, C. Martin, D. Bergogne, C. Buttay, and R. Meuret, "A multi-physics model of the VJFET with a lateral channel," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 30 2011-sept. 1 2011, pp. 1 –10.

[9] I. Abuishmais, S. Basu, and T. Undeland, "On understanding and driving SiC power JFETs," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, march 2011, pp. 1071 –1075.

[10] P. Friedrichs, "Silicon carbide power devices - status and upcoming challenges," in *Power Electronics and Applications, 2007 European Conference on*, sept. 2007, pp. 1 –11.

[11] B. Bose, "Power electronics and motor drives recent progress and perspective," *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 2, pp. 581 –588, feb. 2009.

[12] R. Lai, F. Wang, R. Burgos, D. Boroyevich, D. Zhang, and P. Ning, "A shoot-through protection scheme for converters built with SiC JFETs," *Industry Applications, IEEE Transactions on*, vol. 46, no. 6, pp. 2495 –2500, nov.-dec. 2010.

[13] Semisouth, "Normally-on Trench Silicon Carbide Power JFET," Semisouth, Tech. Rep., 2011.

[14] F. Dubois, D. Risaletto, D. Bergogne, H. Morel, C. Buttay, and R. Meuret, "Active protections for normally-on SiC JFETs," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 30 2011-sept. 1 2011, pp. 1 –10.

[15] E. Rondon, F. Morel, C. Vollaire, and J.-L. Schanen, "Impact of SiC Components on the EMC Behaviour of a Power Electronics Converter," in *Proceedings of the 4th Annual IEEE Energy Conversion Conference and Exposition*, Raleigh, États-Unis, Sep. 2012, p. 4411.