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A solid-mounted resonator-oscillator-based 4.596 GHz frequency synthesis

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This paper describes a 4.596 GHz frequency synthesis based on a 2.1 GHz solid mounted resonator (SMR) voltage-controlled oscillator (VCO). The SMR oscillator presents a chip size lower than 2 mm^2, a power consumption of 18.2 mW, and exhibits a phase noise of −89 dBc/Hz and −131 dBc/Hz at 2 kHz and 100 kHz offset frequencies, respectively. The VCO temperature–frequency dependence is measured to be −14 ppm/°C over a range of −20 °C to 60 °C. From this source, a low noise frequency synthesizer is developed to generate a 4.596 GHz signal (half of the Cs atom hyperfine transition frequency) with a phase noise of −81 dBc/Hz and −120 dBc/Hz at 2 kHz and 100 kHz from the carrier. The frequency synthesis output is used as a local oscillator in a Cs vapor microcell-based compact atomic clock. Preliminary results are reported and discussed. To the authors knowledge, this is the first development of a SMR-oscillator-based frequency synthesizer for miniature atomic clocks applications. © *2011 American Institute of Physics*. [doi:10.1063/1.3567010]

I. INTRODUCTION

Atomic frequency references provide the most stable signals over long integration times because their frequency is determined by an atomic transition. Recently, huge efforts have led to the development of low power consumption chip scale atomic clocks (CSAC) exhibiting typical fractional frequency stability of 2×10^{-10} and 1×10^{-11} at 1 s and 1 h integration time, respectively.[1,2] They consist of a microfabricated alkali vapor cell, a photodiode, and a vertical-cavity surface-emitting laser (VCSEL) whose injection current is modulated by a microwave signal (3.4 GHz for Rb and 4.6 GHz for Cs) coming from a local oscillator (LO). These miniaturized atomic frequency references combining coherent population trapping (CPT) spectroscopy[3,4] and microelectromechanical systems (MEMS) fabrication techniques are of great interest to bring improvements in global positioning systems receivers, synchronization of telecommunication systems, or embedded military applications.

LOs developed for CSAC applications need to combine and satisfy stringent requirements not only in terms of volume (footprint below 1 cm^2) and dc power consumption (∼10–30 mW) but also in terms of phase noise performances, output power, tuning range, and thermal frequency sensitivity.

Phase noise is critical because the short term frequency stability of a passive atomic frequency standard can be degraded by the LO phase noise. Indeed, it has been demonstrated that the LO frequency noise components at even multiple harmonics of the modulation frequency f_m are transferred into the atomic resonator loop bandwidth through an aliasing effect.[5] The frequency stability limitation $\sigma_{y\,\mathrm{alias}}(\tau)$ due to this aliasing effect is given by

$$\sigma_{y\,\mathrm{alias}}(\tau) \simeq \sqrt{S_y(2fm)}\tau^{-1/2} \simeq \frac{f_m}{\nu_0}\sqrt{S_\varphi(2fm)}\tau^{-1/2}, \qquad (1)$$

where ν_0 is the LO frequency, S_y is the power spectral density of the relative frequency fluctuations, and S_φ is the power spectral density of the relative phase fluctuations. Assuming a LO modulation frequency f_m of 1 kHz, it is then found that the LO single-sideband phase noise power spectral density needs to be lower than −60 dBc/Hz at $f = 2f_m = 2$ kHz Fourier frequency to reach a clock fractional frequency stability of 6×10^{-10} at 1 s integration time.

The exact needed LO output power is mainly conditioned by the diode impedance of the VCSEL used in the CPT clock as well as the matching impedance network placed in front of the VCSEL. It has been shown in Rb CPT CSACs that a power lower than −6 dBm is sufficient to transfer 60% of the light power in both first-order lateral sidebands,[6] whereas a power of 0 dBm is well adapted in Cs CSACs.[7]

The LO temperature–frequency dependence needs to be minimized to prevent its resonance frequency to drift out of the tuning range provided by the servo. Simultaneously, the LO tuning range specifications result from a trade-off between frequency deviation capabilities and frequency resolution. It needs to be large enough (a few MHz) in order to be able to adjust accurately the LO frequency but also sufficiently small to improve the frequency resolution and stability.

Different LO technologies have been proposed for CSACs but only a few of them have been concretely tested together with CSAC physics package because of the difficulty to tune the LO frequency to the exact atomic transition frequency. In most cases, the LO microwave signal is generated by frequency multiplying and synthesizing the RF frequency signal (typically 10 MHz) of a few mW power consumption temperature-controlled or microprocessor-controlled

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crystal oscillator. However, this frequency multiplication degrades the phase noise and may require additional power consumption. In an another way, Brannon *et al.* developed for CSAC applications microwave oscillators based on quarter-wavelength ceramic-filled coaxial resonators with phase noise performances of −35 dBc/Hz and −94 dBc/Hz at 100 Hz and 10 kHz from the carrier, respectively.[6] Nevertheless, the opportunity to develop fully integrated MEMS oscillators is of great interest for CSACs to simplify the fabrication process and to reduce the production cost.

In that sense, a promising solution is the development of sources based on bulk acoustic wave (BAW) resonators due to their small size and relatively high Q-factor.[8] Usually, there are three different kinds of BAW resonators: film bulk acoustic resonators (FBARs), high-overtone bulk acoustic resonators (HBARs), and solid mounted resonators (SMRs). FBAR was applied by Romisch and Lutwak in a low power 4.596 GHz Colpitts oscillator for Cs CSAC applications.[7] HBARs are also a really promising technology because they presently exhibit the highest Q-factors[9,10] with dimensions compatible for CSACs. Recently, Yu *et al.* demonstrated a HBAR-based 3.6 GHz Pierce oscillator with a phase noise of −67 dBc/Hz at 300 Hz fourier frequency, a power consumption of 3.2 mW, and a free-running frequency stability of 1.5×10^{-9} at 1 s.[11] The HBAR source was successfully frequency locked to a CPT resonance in a cm-scale Rb vapor cell CPT clock.

A major problem of BAW resonators is their high thermal frequency sensitivity. To overcome this issue, Pang *et al.*[12] reduced the frequency–temperature dependence of a 2.8 GHz FBAR to 40 ppm/K using an integrated air-gap capacitor. Yu *et al.* developed ultratemperature stable BAW resonators (less than 1 ppm/K; Ref. 13) using a SiO_2 compensation support layer. Recently, Baron *et al.* even demonstrated radio frequency HBARs with a second-order temperature compensation.[14] Another difficulty with BAW resonators is the difficulty to operate on the desired mode due to the presence of a high density of closely spaced series and parallel resonances.

This paper is devoted to present an original SMR-oscillator-based 4.596 GHz frequency synthesis. Low power and low phase noise SMR BAW oscillators have been proposed recently.[15] To our knowledge, no scientific reference reports the concrete use of such sources in CPT atomic frequency standards. The packaging and miniaturization of the ensemble is not reported but remains fully feasible. Section II describes the 2.1 GHz SMR voltage-controlled oscillator (VCO). Section III presents the frequency synthesis to generate the 4.596 GHz signal as well as other useful signals. Eventually, in Sec. IV, the detection of CPT resonances using the 4.596 GHz synthesized signal is demonstrated in a mm-scale Cs vapor cell CPT clock. A preliminary clock frequency stability measurement is realized and discussed.

II. THE SMR-BASED VOLTAGE-CONTROLLED OSCILLATOR

Figure 1 shows the schematic structure of the SMR. The SMR mainly consists of a metal-piezo (Mo–AlN)-metal

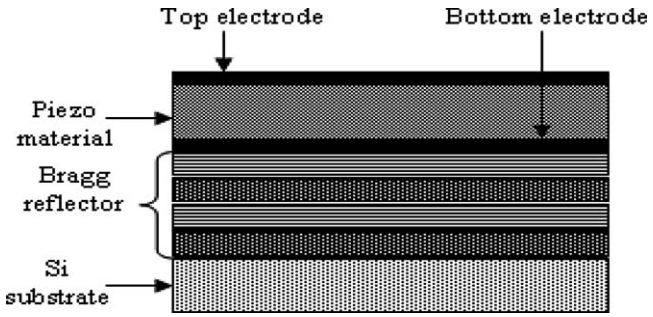


FIG. 1. Cross section of the solid mounted resonator.

layered sandwich. The resonator is constructed over a Bragg reflector acoustic mirror structure using alternating layers of low and high acoustic velocity. The Bragg reflector is made of Tungsten (W) and silicon oxide (SiO_2). Using acoustic wavelength mismatch of the Bragg reflector ensures a *1b-type* acoustic mode, essentially meaning that thickness and shear modes are able to propagate. Acoustic boundary conditions in the resonator perimeter need to be controlled to confine the acoustic energy in the useful thickness mode within such a resonator. This is obtained by the so-called "frame" technique[16] consisting to insert an additional ringlike acoustic loading modification on the top of the stack. When successively employed, this process leads to resonators with high quality factors.

The SMR is measured on the wafer with a probe station. Figure 2 shows the impedance magnitude of the SMR measured with a vectorial network analyzer. A quality factor value of 1176 at the series resonance frequency f_s of 2.083 GHz is obtained. This Q-factor value decreases to 502 at the parallel resonance frequency f_p of 2.125 GHz. One can see a spurious phenomenon around 2.05 GHz caused by a lack of optimization on "frame" producing a parasitic resonator and jails acoustic energy. Then, the series resonance is chosen to operate the oscillator with improved phase noise performances. For this purpose, the SMR must be connected to a low impedance part of the active circuit, so that the surrounding impedances would be low enough not to degrade the series resonance of the Q-factor.

A good candidate for the VCO architecture is the common-base configuration shown in Fig. 3. The oscillator was designed and optimized to achieve low phase noise

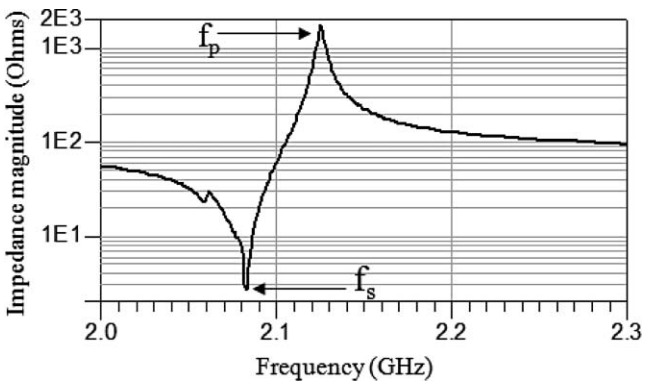


FIG. 2. Measured impedance magnitude of the solid mounted resonator.

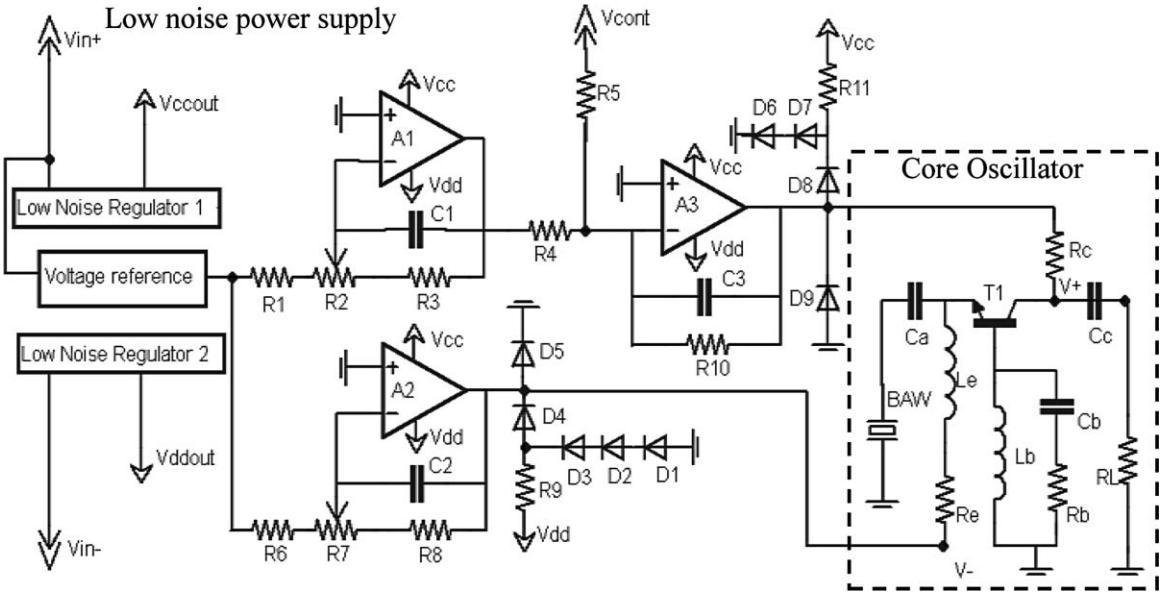


FIG. 3. Simplified schematic of the SMR VCO.

using ADS software and according to Kurokawa criterion,[17,18] while the layout is realized by CADENCE. The SMR VCO consists of two main parts: the solid-mounted resonator used to fix the frequency and the active circuit that compensates the resonator losses. The active circuit is a SiGe:C heterojunction bipolar transistor using BiCMOS7RF 0.25 μm technology processes from ST Microelectronics. This transistor exhibits a theoretical 1/*f* noise cutoff frequency of about 2 kHz and was chosen to reduce the flicker phase noise up-conversion.

Both the transistor T1 and the inductor Lb are connected together to create a negative differential resistance. Cb and Rb are connected in series to the base of T1 in order to minimize the value of Lb. In this way, the chip size is reduced and the phase noise performances of the oscillator are improved. A low noise power supply is designed and realized to optimize the phase noise of the SMR VCO. As shown in Fig. 3, positive and negative bias voltages (*Vcc* and *Vdd*) are supplied by low noise regulators. The power supply noise at the input of the three operational amplifiers A1, A2, and A3 is then reduced to less than 30 μVRMS (10 Hz to 100 kHz frequency range) according to the data sheet of the low noise regulators. The main role of these operational amplifiers is to modify the voltage reference which exhibits a thermal stability of 3 ppm/°C and to provide the optimum bias voltage to the core oscillator in order to minimize its phase noise ($V+ = 0.9$ V and $V- = -1.7$ V). The varactors (D1 to D9) are used for voltage safety of the core oscillator. To frequency lock the oscillator on the atomic cell resonance, only a narrow tuning bandwidth is required. This explains why we did not use varactor diodes to prevent the LO phase noise degradation. The fine frequency tuning of the oscillator is achieved by the adjustable voltage control supply V_{cont} added to the bias voltage $V+$. The coarse frequency tuning necessary to compensate for the SMR resonance frequency offset from the ideal correct value (4.6 GHz or 2.3 GHz if a frequency doubler is used) is achieved by a direct digital synthesis (DDS) circuit.

Figure 4 shows a photograph of the SMR oscillator. The implemented core oscillator uses a hybrid method by wire-bonding the BiCMOS chip (1 mm × 1 mm) and the solid mounted resonator (0.35 mm × 0.3 mm). For optimal phase noise performances, the oscillator is biased at 7 mA with $V+ = 0.9$ V and $V- = -1.7$ V producing a 2.09 GHz oscillation frequency with a −1.2 dBm output power.

Figure 5 shows the measured oscillation frequency and output power of the SMR VCO as a function of the voltage control V_{cont}. The oscillation frequency variation is about

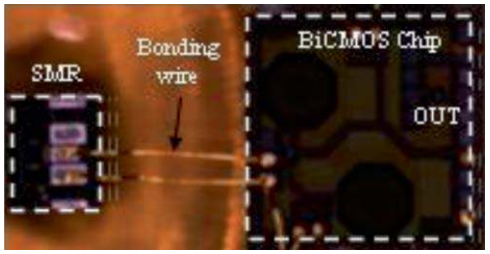


FIG. 4. (Color online) Microphotograph of the SMR oscillator (SMR size: 0.35 mm × 0.3 mm and BiCMOS chip size: 1 mm × 1 mm).

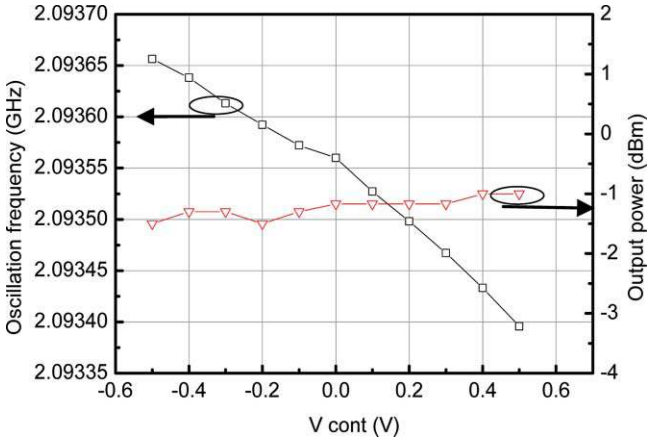


FIG. 5. (Color online) Measured oscillation frequency and output power of the SMR VCO as a function of V_{cont} (from −0.5 to 0.5 V).

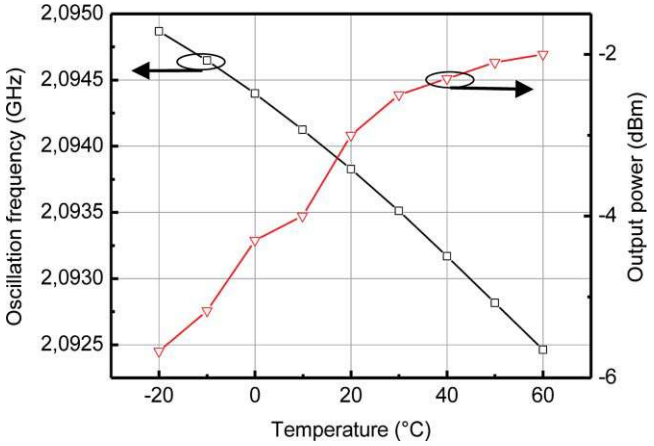


FIG. 6. (Color online) Measured oscillation frequency and output power of the SMR VCO as a function of the temperature.

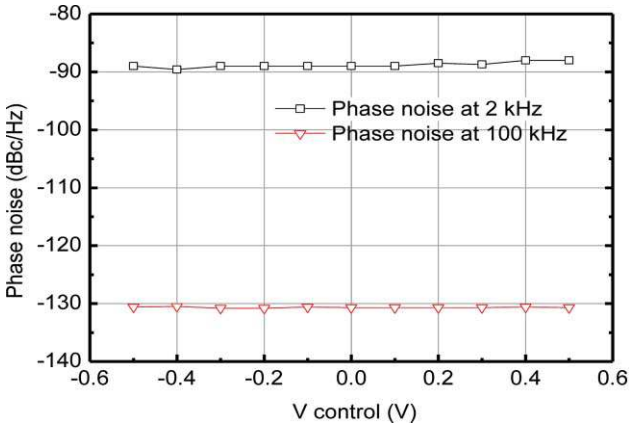


FIG. 8. (Color online) Measured phase noise at 2 kHz and 100 kHz offset of the SMR VCO as a function of V_{cont} (from −0.1 to 0.1 V).

linear and measured to be 260 kHz for a 1 V total voltage tuning (260 kHz/V). The measured output power variation is 0.5 dBm for V_{cont} varying from −0.5 to 0.5 V. Figure 6 reports the variation of the VCO output frequency and power versus the resonator temperature from −20 °C to +60 °C with 10 °C steps. In this range, the total frequency shift due to temperature is 2.4 MHz leading to a relative frequency–temperature dependence of −14 ppm/°C. Assuming a control of the VCO temperature at the mK level, the relative frequency variation of the VCO is then limited to 1.4×10^{-8}. The variation of the VCO output power versus the temperature is about 3.6 dBm in the same temperature range. It leads to a sensitivity of 0.045 $dBm/°C$.

The VCO phase noise was measured with Agilent E5052B equipment at room temperature. Figure 7 shows that the phase noise curve presents a −30 dB/decade slope between 100 and 3 kHz frequency offset and a −20 dB/decade slope between 3 and 3.5 MHz offset frequency. This result agrees well with the Leeson effect[19,20] stipulating that the amplifier phase noise is converted into frequency noise in the oscillator loop for Fourier frequencies lower than the Leeson frequency $f_L = \nu_0/2Q_L$. The VCO phase noise is −160 dBc/Hz for $f > 3.5$ MHz and is −82 dBc/Hz at 1 kHz offset frequency. We also note that the level of spurious peaks is very low. Figure 8 shows the measured phase noise at 2 and 100 kHz offset of the SMR VCO as a function of the voltage control V_{cont} (from −0.5 to 0.5 V). A very slight degradation of the VCO phase noise, lower than 1.5 dB, is obtained at $f = 2$ kHz when the voltage control is increased, while no significant variation is observed at $f = 100$ kHz.

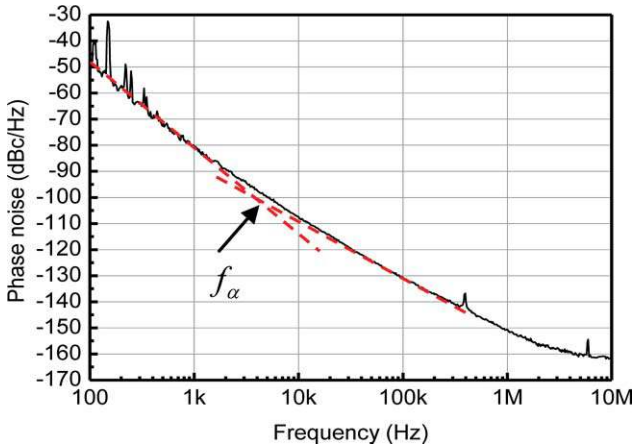


FIG. 7. (Color online) Measured phase noise of the SMR VCO ($V+ = 0.9$ V, $V- = -1.7$ V, and $I_{\text{bias}} = 7$ mA).

III. THE 4.596 GHZ FREQUENCY SYNTHESIS

Figure 9 shows the configuration of the 4.596 GHz frequency synthesis based on the 2.1 GHz SMR VCO. Except for the latter, all the components are commercially available components in order to validate fully the synthesis architecture. The generation of the 4.596 GHz signal is realized by first frequency-doubling the VCO frequency at 4.2 GHz. Simultaneously, a signal of 396 MHz frequency is generated by mixing (mixer M1) the 384 and 12 MHz signals from two direct digital synthesis DDS2 and DDS1, respectively. Eventually, the 4.596 GHz signal is obtained by mixing the 4.2 GHz and the 396 MHz signals using the mixer M2. Up-converter mixers (M1 and M2) with image rejection are applied to this frequency synthesis for their clean output frequency spectrum. Additional attenuators and low noise amplifiers are added before these mixers in order to adjust properly the power of the mixers inputs. This allows us to optimize image rejection and conversion losses of the mixer and consequently to improve phase noise performances. An amplifier LNA 3 and an attenuator are used to adjust the output power of the 4.596 GHz signal to be sent to couple microwave power in the VCSEL diode.

A synchronization clock signal (77 MHz) for DDS1, DDS2, and a field-programmable gate array circuit (FPGA) is delivered by tracking and frequency dividing the SMR oscillator signal. This topology allows us not only to take advantage of the good phase noise of the SMR VCO but also to avoid possible synchronization problems when we demodulate the CPT resonance signal. Except for the DDS2 that is controlled by a computer to generate the additional frequency, all other digital circuits are controlled by a FPGA. A frequency shift keying (FSK) modulation at a bit rate of 1 kHz and frequency

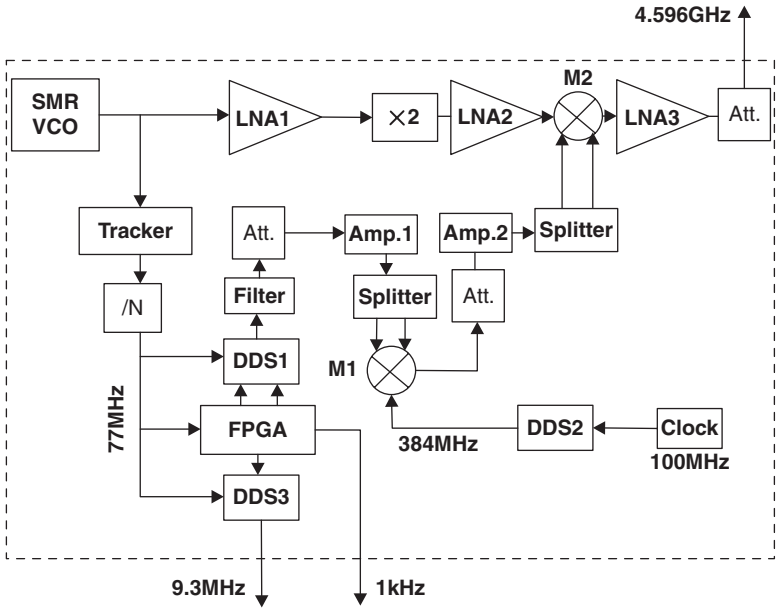


FIG. 9. Architecture of the SMR-VCO-based frequency synthesizer.

deviation of 3 kHz is generated by the DDS1. This modulation is used to lock the final VCO output frequency on the atomic transition frequency. The DDS3 generates the useful 9.3 MHz RF signal to characterize easily the atomic clock frequency stability when the CPT clock is locked.

Figure 10 shows the frequency spectrum of the 4.596 GHz signal from the synthesis output without any modulation. The output power is measured to be about 0 dBm. Figure 11 reports on the same plot phase noise performances of the free-running 2.1 GHz SMR VCO, the DDS2 (384 MHz), and the 4.596 GHz frequency synthesis output. The phase noise was measured with Agilent E5052B equipment at room temperature. For $f > 150$ kHz, the frequency synthesis phase noise is clearly limited by the DDS2 phase noise at a level of -120 and -132dBc/Hz at 1 MHz and 10 MHz offset frequencies, respectively. For $f < 100$ kHz, the phase noise of the 4.596 GHz frequency synthesis signal is imposed by the phase noise of the VCO with a degradation of about 6–7 dB according to the low noise frequency doubling process. Consequently, the phase noise of the 4.596 GHz signal is -76 and -100 dBc/Hz at $f = 1$ and 10 kHz, respectively.

IV. APPLICATIONS TO A MINIATURE CPT ATOMIC CLOCK

Sections IV A shows preliminary tests in which the SMR-VCO-based frequency synthesis is used as a local oscillator in a compact CPT atomic clock.

A. Experimental setup

The CPT clock experimental setup, depicted in Fig. 12, mainly consists of the SMR-VCO-based frequency synthesis, a VCSEL resonant with the Cs D_2 line at 852 nm, a

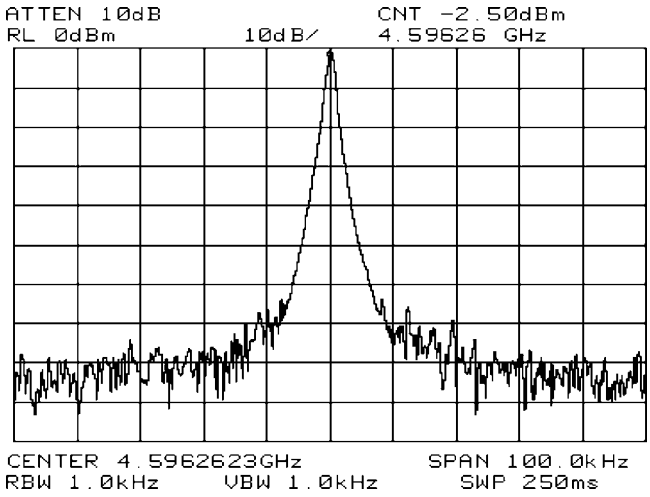


FIG. 10. Frequency spectrum of the 4.596 GHz signal from the synthesis output without modulation.

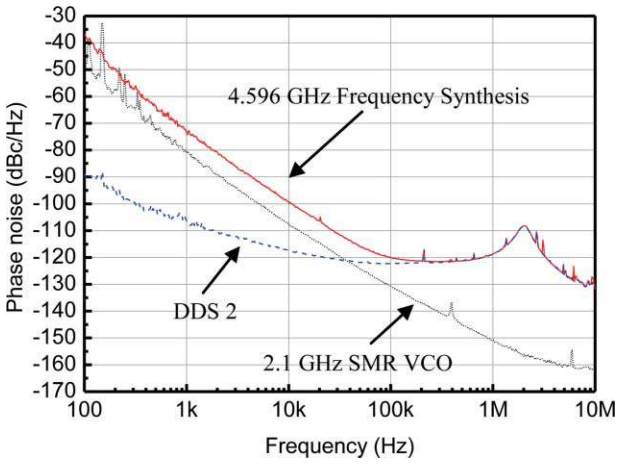


FIG. 11. (Color online) Phase noise performances of the 2.1 GHz SMR VCO, of the DDS2 and of the 4.596 GHz output signal of the frequency synthesizer.

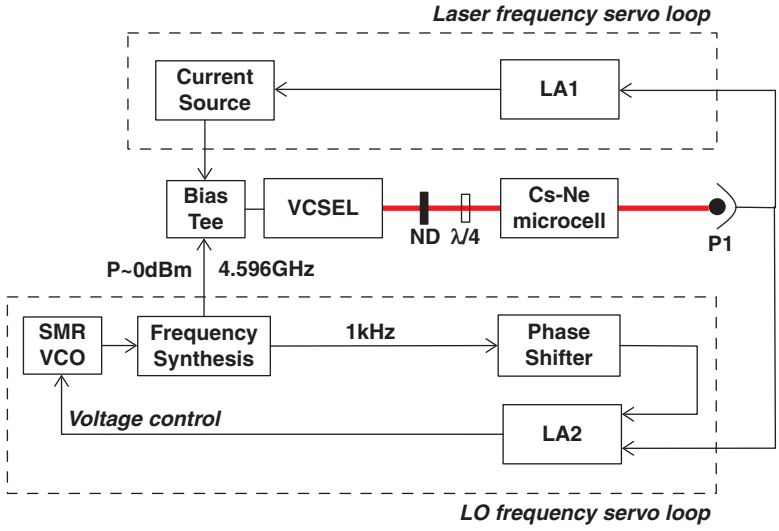


FIG. 12. (Color online) The CPT clock experimental setup consists of a VCSEL, a Cs vapor microcell filled with a Ne buffer gas pressure, and a photodetector. The injection current of the VCSEL is modulated with the 4.596 GHz signal from the SMR-oscillator-based frequency synthesizer output. The CPT resonance is measured by scanning the synthesizer output frequency and by detecting the change in the laser power transmitted through the cell. The CPT signal is then extracted to produce a voltage error and correction signal used to lock the synthesizer output frequency to the atomic transition.

microfabricated Cs vapor cell[21–23] filled with a Ne buffer gas pressure in order to operate in the Dicke regime,[24] and a photodetector.

The injection current of the VCSEL is directly modulated by the 4.596 GHz signal with a power of 0–2 dBm coming from the frequency synthesizer driven by the 2.1 GHz SMR VCO. Two phase-coherent optical sidebands separated by the atomic ground state transition frequency (i.e. the clock frequency at 9.192 GHz) are then generated, allowing us to pump the atoms in the CPT state. In this so-called dark state, the optical media becomes transparent and a maximum of optical power is detected at the output of the cell by the photodiode P1. In our experimental setup, the presence of Ne buffer gas in the cell causes a slight shift of the clock frequency of about +45 kHz (Refs. 25 and 26) because of alkali-buffer gas collisions.[27]

The microcell temperature is stabilized to within 1 mK around 62°C where the CPT signal height is maximized. The atomic resonator is surrounded by a solenoid applying a static magnetic field of 15 μT in order to raise the Zeeman degeneracy and isolate the hyperfine clock transition $|F = 3, m_F = 0\rangle \rightarrow |F = 4, m_F = 0\rangle$. The ensemble is inserted into a cylindrical mu-metal magnetic shield in order to reduce spurious environmental magnetic fields.

The linearly polarized output beam from the VCSEL is collimated and converted into circular polarization using a quarter-wave plate. A neutral-density filter is used in order to obtain a laser intensity of about 315 μW/cm^2, which optimizes the slope of the CPT resonance error signal.

The VCSEL frequency is locked on the position of maximum optical absorption by modulating the laser dc current at 65 kHz and demodulating the absorption signal on the photodiode with the lock-in amplifier LA1. An error signal is then fed back to the VCSEL current driver to correct the laser injection bias current. The CPT resonance is measured by scanning the synthesizer output frequency and by detecting the change in the laser power transmitted through the cell. A commercial lock-in amplifier (LA2) driven by the 1kHz FSK modulation signal from the described synthesis is used to increase the signal-to-noise ratio of the detected CPT resonance. A voltage error signal is then amplified in a PI controller and sent to the electric tuning port of the SMR VCO in order to lock the synthesizer output frequency to the atomic transition.

B. Experimental results

The CPT resonance was successfully detected. Figure 13 shows the typical shape of the CPT resonance (direct output of the lock-in amplifier LA2) obtained when the VCSEL injection current is modulated with the 4.596 GHz signal from the SMR-VCO-based frequency synthesizer. The linewidth of the clock transition, extracted by fitting the CPT resonance error signal with the FM lineshape of a Lorentzian function,[28] is measured to be 6.5 kHz.

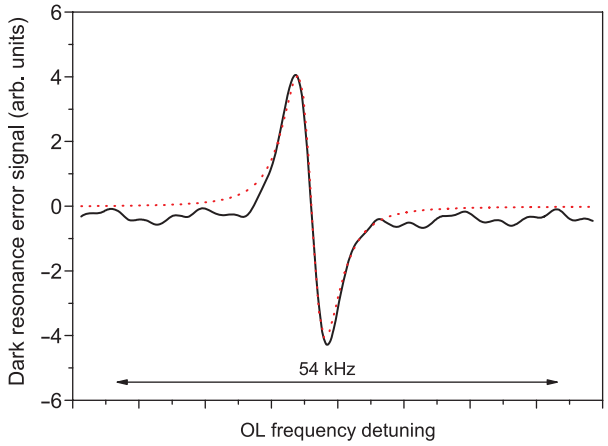


FIG. 13. (Color online) Typical CPT resonance error signal at the output of the lock-in amplifier LA2 (solid line: experimental data, dotted line: data fit). The CPT resonance linewidth, extracted by fitting this signal by a FM Lorentzian lineshape, is measured to be 6.5 kHz.

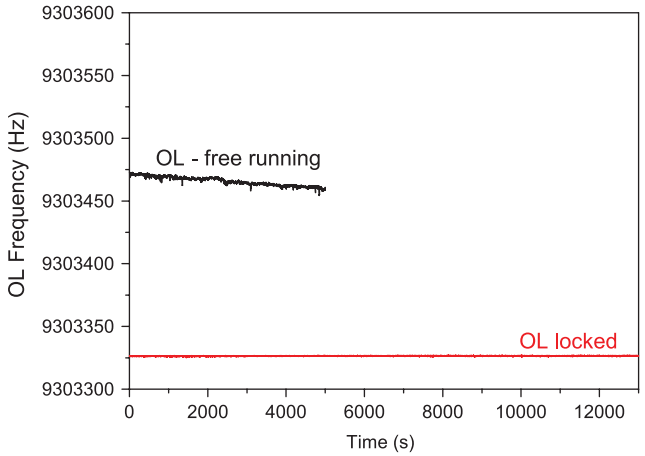


FIG. 14. (Color online) Output frequency of the SMR VCO vs time: free-running or locked.

Once the CPT resonance is detected, the synthesizer output frequency is locked to the atomic transition frequency. The clock frequency is measured by extracting a 9.3 MHz signal from the SMR-oscillator (see Fig. 9) and counting it with a digital high resolution frequency counter. The clock frequency stability is determined using a 5120A Allan deviation test set[29] referenced by a hydrogen maser.

Figure 14 plots the 9.3 MHz signal frequency versus time in respective cases where the SMR oscillator is free-running or locked to the atomic transition. Figure 15 shows that the Allan deviation of the free-running oscillator is measured to be 9.5×10^{-8} at 1 s integration time and increases after 10 s averaging time. This means that the SMR oscillator needs to be locked to the atomic CPT resonance with a minimum loop bandwidth of 1 kHz to reach a frequency stability of 1×10^{-10} at 1 s in the locked regime. In a preliminary measurement, the BAW oscillator signal fractional frequency instability was measured to be $2.5 \times 10^{-9}\ \tau^{-1/2}$ for integration times up to 20 s when locked to the atomic transition frequency. This represents an improvement by a factor of 38 and 83 compared to the unlocked regime at 1 and 10 s, respectively. The clock short-term frequency stability could be improved by an order of magnitude by increasing the LO

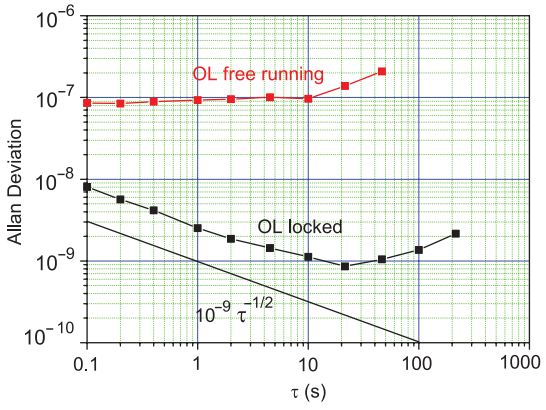


FIG. 15. (Color online) Allan deviation of the SMR VCO in free-running or locked configurations.

frequency servo loop bandwidth at about 1 kHz (less than 100 Hz in the current case). Unfortunately, this result could not be optimized because of time constraints. For longer integration times, the clock frequency drifts because of temperature variations in the laboratory room as well as laser intensity fluctuations.

V. CONCLUSIONS

We presented a 2.1 GHz SMR voltage-controlled oscillator with a phase noise of −89 dBc/Hz at $f = 2$ kHz and −131 dBc/Hz at $f = 100$ kHz. The chip size of the core oscillator is lower than 2 mm^2. The frequency–temperature dependence is −14 ppm/°C over a range from −20°C to 60°C, while its power consumption is 18 mW. An original analog–digital 4.596 GHz frequency synthesizer based on the designed SMR VCO was realized and tested. The SMR-VCO-based frequency synthesizer was preliminary successfully locked to the CPT resonance of Cs atoms in a mm-scale vapor cell.

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