An Accelerated Stress Test Method for Electrostatically Driven MEMS Devices

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Abstract

This paper addresses an innovative solution to develop a circuit to perform accelerated stress tests of capacitive MEMS switches and shows the use of instruments and equipment to monitor physical aging phenomena. A dedicated test circuit was designed and fabricated in order to meet the need for accelerated techniques for those structures. It integrated an in-house miniaturized circuit connected to additional test equipment (e.g. oscilloscope and capacitance meter) that enabled reliability characterization of capacitive switches. The Accelerated Stress Test (AST) circuit generated an ElectroStatic Discharge (ESD) like impulse that stressed the device. This setup allowed simultaneous measurement of the current and voltage waveforms, and the capacitance variation of the device under test after each stress. The results obtained using the miniature AST circuit are discussed and were correlated with results obtained using a commercial Human Body Model (HBM) tester as well as data from cycling benchmark. The scope of this paper encompasses; theory, methodology, and practice of measurement; the

development of an testing miniaturized board; analysis, representation of the information obtained from a set of measurements. As a result, it may contribute to the scientific and technical standards in the field of instrumentation and measurement of electrostactically actuated devices having insulating layers.

Keywords

Microelectromechanical devices, Reliability testing, Electrostatic discharges (ESD), Charging, Accelerated testing, Dielectric breakdown

I. Introduction

In the RF-MEMS switch market, despite the lack of significant revenue since 2003, RF-MEMS switches continue to fascinate the industry [1]. New designs and structures have been evolving rapidly. Nowadays, RF-MEMS devices are produced in appreciable volumes and in the coming years the market may increase significantly. This market expansion will pressure manufacturers to lower unit costs since 80% of the total production cost is devoted to device packaging [2]. Therefore significant savings can be obtained by detecting defective components at the wafer-scale, prior to packaging [3]. However characterizing the electromechanical properties of RF-MEMS structures at a very early stage of manufacturing is a challenging task for quality assurance in on-wafer testing field. Furthermore, standardized testing procedures are not yet available.

In the last decade, the reliability of RF-MEMS switches has been intensively investigated [4]–[10]. One of the main issues in electro-statically driven MEMS switches is dielectric charging [11], [12]. Charge is deposited on the surface or trapped in the bulk of the dielectric material. This failure mechanism occurs over time and over a repeated number of cycles.

Up to now the basic lifetime test method is based on the pull-out and pull-in cycling. In this procedure arbitrary voltage waveform profiles, such as simple square wave or two step one, have been used. The results of these investigations using the cycling method led to the conclusions that the device lifetime:

- decreases exponentially with magnitude of the pull-in voltage [11] and
- depends only on the cumulative pull-in time and not on the cycling frequency or duty cycle [13]

In spite of these basic conclusions, the only alternative method for RF-MEMS lifetime prediction is the use of continuous DC stress [11], [14], [15]. Unfortunately those tests are still time consuming, since typical RF-MEMS switches should have lifetimes on the order of years, a demonstrator with a lifetime of 10 years cannot be easily obtained with such tests.

In this scope and based on expertise gathered from modeling [16] and Pulse Induced Charging experiments [17], there exists a need to develop a methodology for accelerated testing of electro-statically driven RF-MEMS switches.

The proposed methodology deals with the use of ESD-like pulses in order to perform an Accelerated Stress Test (AST). For this work, a dedicated circuit has been fabricated and integrated into a complete test bench. The circuit can be easily mounted on RF probes. It allows the monitoring of the current waveform across the device during the discharge and includes a direct output for capacitance or DC

leakage measurements. The data obtained are discussed and correlated with results obtained using a commercial Human Body Model (HBM) tester as well as with data from the conventional cycling benchmark.

In our previous work [17], [18], we have shown that voltage and temperature acceleration is conceivable in reliability testing of RF MEMS switches, using a Pulse Induced Charging (PIC) setup (Fig.1) and the correlation between AST results and conventional cycling data has been shown.

However, signals provided by the conventional pulse generator used in the PIC setup leads to an Electrical Over Stress (EOS) type breakdown as shown in Fig.2(a). ESD stress failures lead to small degradations that can easily be located and analysed, giving additional information on the failure mechanism (Fig.2(b) and 2(c)). EOS breakdown on the other hand, will completely destroy the component. Therefore, there's no way to determine the cause of failure. This is one of the first reasons the AST circuit and methodology, proposed in this paper, has been developed. The wiring diagram of the AST circuit is shown in Fig.3. It also integrates other interesting functionalities such as:

- The circuit is directly mounted on a RF probe in order to drastically reduce the parasitic capacitance of the cables and connectors.
- Using a conventional ESD generator, the setup does not allow the use of a voltage probe, because the capacitance of the probe ($\sim$10pF) is close to the down-state capacitance of the RF MEMS switch and it will then dissipate the discharge before it stress the device. Hence a 1 - 49Ω bridge is used in order to capture in real-time the current waveform during a discharge , allowing us to determine the voltage across the device after discharging if no breakdown occurs. This voltage is given by:

$$V_{DUT} = V_{generator} - \frac{1}{C}\int Idt. \tag{1}$$

- The circuit integrates a direct OUTPUT connection (SW4 on the diagram) for external capacitance or DC leakage measurements.
- Finally the circuit is small, portable, easily mounted with other measurement instruments and can be easily placed in a vacuum chamber for instance.

II. Fabrication and integration within a complete test bench

The AST circuit diagram is represented in Fig.3. The corresponding printed circuit board (PCB) was miniaturized as small as possible. The final PCB dimensions were 35×45 mm. The circuit board and the layout are both represented in Fig.4(a). The printed circuit was made on a 0.8 mm-thick PCB FR4 substrate. The line width was chosen to have an 50 Ω of resistance for impedance matching. SMA connectors were used to connect the AST board to external instruments. Reed relays were used for fast commutations in order to control the charging and discharging time of the 100 pF capacitor. All the other electronic components of the board (capacitor, inductor, resistance, diodes) were Surface Mounted Devices (SMD). The fabricated circuit was mounted on a RF probe as shown in Fig.4(b).

The complete AST test bench schematic is shown in Fig.5. The programmable High Voltage (HV) source was connected to the board in order to charge the 100 pF capacitor (SW1 on). The Tektronix AFG320 signal generator was used to controlled SW2 and SW4 relays (SW2 was on to apply the

discharge and SW4 was on for the capacitance measurement). In order to be sure that no residual signal remains in the DUT, SW3 was used to short-cut the DUT. During the discharging, the waveforms were monitored through the Tektronix DPO 4034 oscilloscope. A BOONTON 7200 capacitance meter (1 fF to 2000 pF range) was used to measure the CV characteristics. Automation of the setup was performed using LabVIEW.

III. MEASUREMENT RESULTS

Time	SW1	SW2	SW3	SW4	Action
t_0	ON	OFF	OFF	OFF	Charge the 100 pF capacitor
t_1	ON	ON	OFF	OFF	Discharge the ESD-like pulse to the device which will remains until SW4 was switched ON
t_2	ON	OFF	OFF	ON	Measure the capacitance (or the leakage current)
t_3	ON	OFF	ON	OFF	Short-cut the 100 pF capacitor

TABLE I
SEQUENCE FLOW OF THE AST METHODOLOGY

Beyond the development and fabrication of this circuit board, it is important to consider this experiment as a complete methodology. The validation of the board was done following an established sequence, which is shown in Table I.

The output "SCOPE" of the board was connected to channel 1 of the oscilloscope. Using"T" connectors, channels 2 and 3 were used to monitor the control signals of the two relays SW2 and SW4 (powered by the signal generator). The Trigger was set to the front-edge of channel 2, i.e. the moment the discharge was applied to the device. The precise measurement of the stress duration was crucial to the overall method described in this paper. According to the sequence flow shown in Table I, the duration of the stress applied to the component was the difference between t_2 and t_1. In fact, at $t = t_1$, the discharge was applied to the device, but the energy out from the discharge remained on the device until $t = t_2$ when SW4 was turned ON and the energy that remained in the device could dissipate. The time-charts of this measurement are presented in Fig.6(a). Hence the stress time was controlled using SW2 and SW4. In this work the stress time was arbitrary chosen to be 20 ± 5 ms. The resulting discharge waveform of the capacitor to an short-circuit is shown in Fig.6(b). As expected, it corresponded to an Human Body Model (HBM)-like waveform of ~ 550 ns. It was equivalent to the discharge of the capacitor through the 1500 Ω resistor and the 5 μH inductor.

Thorough analysis of the circuit was performed using VHDL simulations (SystemVision software) and was reported in our previous work [19]. In this work the stress was applied to the same test structure than reported in [17], however in principle it could be applied to any MEMS structure with an insulating layer in its active area (e.g. electrostatically driven capacitive structures). The test structure consisted of a doubled-clamped beam structure with an active area of of 96×77 μm^2. The insulating film above the signal was ~ 250 nm of high-frequency-processed silicon nitride ($HF - Si_3N_4$). The gap between the signal line and the upper membrane was $1.5\mu m$. The actuation voltage was $20 - 25V$. The test procedure was as follow:

1) An initial CV curve was measured (the principle of this methodology partial CV curve is described in [17]),
2) The stress was applied to the signal line of the device. Following the procedure described in Table I.
3) Another partial CV curve was measured after the stress.

The superposition of the two CV graphs from step (1) and step (3) showed a shift in voltage ΔV. This shift was proportional to the amount of charge collected or trapped by the dielectric material, which is an indicator of its reliability, and therefore its lifetime [11].
It has been shown that a correlation exists between HBM test results and data from conventional cycling test [18]. In fact, the relation between the charging and the time the switch remains in the downstate during cycling is:

$$\Delta V_c(t_c, N_c) = \Delta V_{0,c} \cdot \left(\frac{t_{down,c}}{\tau_c}\right)^{n_c} \cdot N_c^{n_c}, \tag{2}$$

where $\Delta V_{0,c}^*$ is the cycling amplitude factor that depends on the material, $t_{down,c}$ is the total down-state time of the cycling calculated from the frequency and the duty cycle, τ_c the charging process time constant (also material dependent), N_c is the number of cycles, and n_c is power law exponent/index.

An analogous expression is proposed for the pulse-stressing data obtained herein:

$$\Delta V_s(t_s, N_s, E_s) = \Delta V_{0,s} \cdot \left(\frac{t_{down,s}}{\tau_s}\right)^{n_s} \cdot N_s^{n_s} \cdot \left(\frac{E_s}{E_0}\right)^{m_s}, \tag{3}$$

where $\Delta V_{0,s}$ is the stress amplitude factor that depends on the material, $t_{down,s}$ is the total down-state time of the stress, τ_s the charging time constant, N_s is the number of pulses, E_s is the electric field of the stress, E_0 is an equivalent factor and m_s, n_s are power law exponents.

In order to make the correlation between the pulse stress method and cycling, it is necessary to examine the common relation between the resulting voltage shifts ΔV_c and ΔV_s. Taking into account the electric field intensity during cycling was $E_c = 0.8$ MV/cm, and assuming that we apply only a single cycle/pulse under this electric field, we obtain: $\Delta V_c = 18mV$ and $\Delta V_s = 26mV$.
It allows us, within a given and tolerable error, to assume that high voltage impulse ageing can be done and the acceleration factor has been determined to be:

$$N = \left(\frac{E_s}{E_c}\right)^{\alpha},$$

where $\alpha > 1$ (in this case $\alpha \sim 1.5$).

In Fig.7, we plotted results from conventional cycling tests, HBM stress testing [18] and data obtained using the AST circuit. The cycling results showed a shift ΔV as a function of number of cycles whereas HBM and AST stress results show a shift ΔV as a function of the electric field. The higher the electric field was the shorter the lifetime of the device (here it is assumed that the lifetime is related to the parameter ΔV). The results of HBM and AST testing were obtained using one single, virgin device for each data point in order to avoid any residual stresses.
Finally the results show that high voltage impulse testing can be used for voltage accelerated tests in electrostatically driven MEMS switches and the AST circuit developed here is an original demonstration.

IV. Conclusion

This paper proposed an accelerated testing methodology for RF MEMS switches lifetime qualification. Correlation between conventional cycling measurements and the results obtained using the AST circuit was presented. It constituted an effective on-wafer accelerated stress test and the authors believe that it can contribute to the standardization of reliability test procedures for RF-MEMS switches. Since the AST circuit board was small, it could easily be placed in a vacuum chamber for controlled environment condition tests. Simultaneous measurement of mechanical displacement using a laser interferometer is also conceivable. This methodology was not devices-limited and it could be used as general testing technique.

Acknowledgment

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Figures

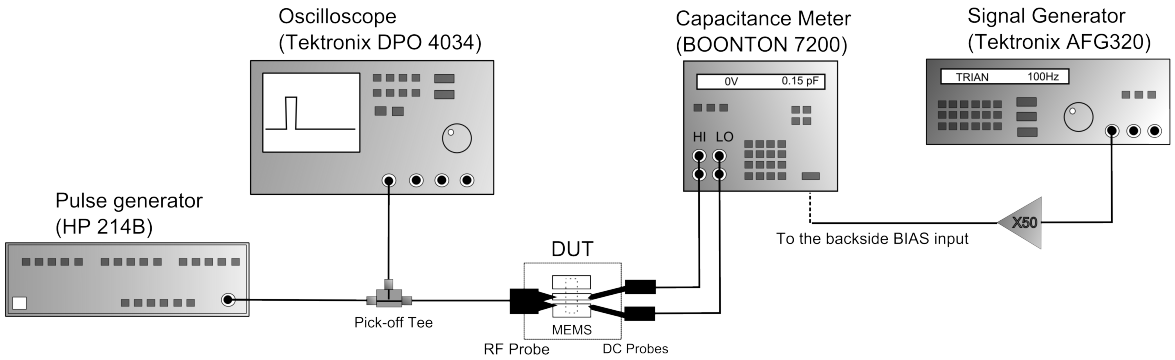
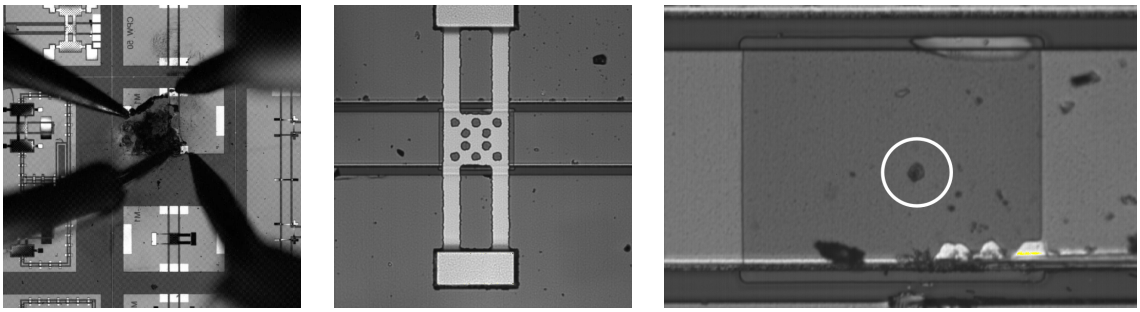


Fig. 1. Pulse Induced Charging setup.



(a) (b) (c)

Fig. 2. Consequence of (a) an Electrical Over Stress (EOS) breakdown and (b) an ESD-like pulse breakdown, (c) the assessment of the real failure by removing the upper membrane manually.

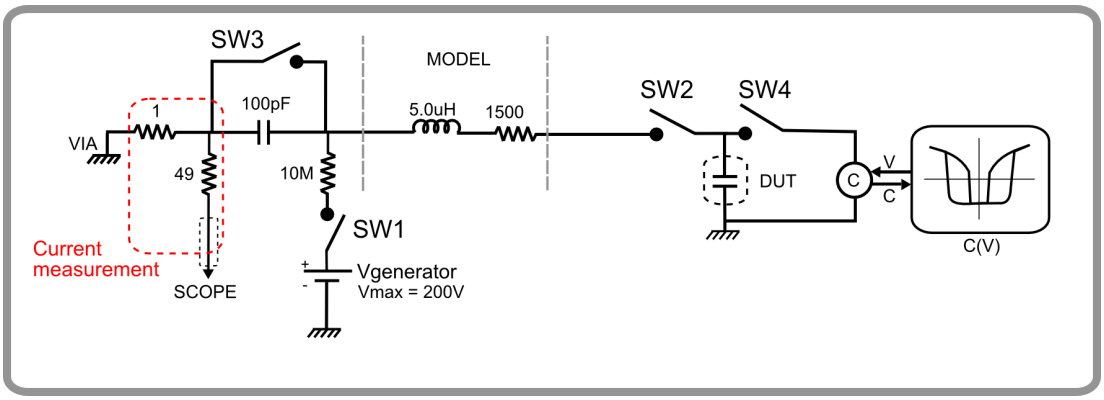
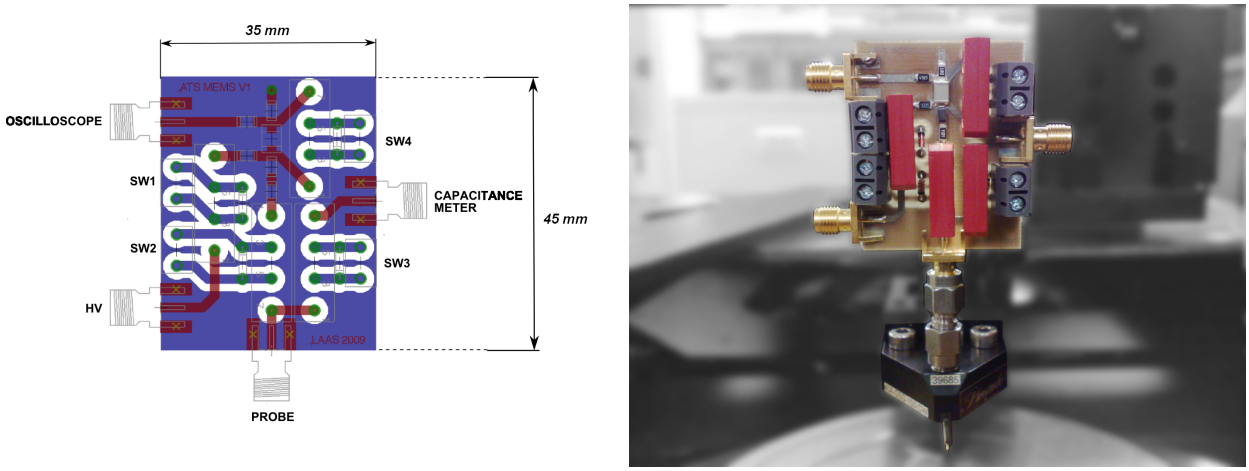


Fig. 3. Accelerated Stress Test Circuit diagram.



(a) Circuit layout

(b) Fabricated circuit

Fig. 4. Fabrication and mounting of the AST circuit.

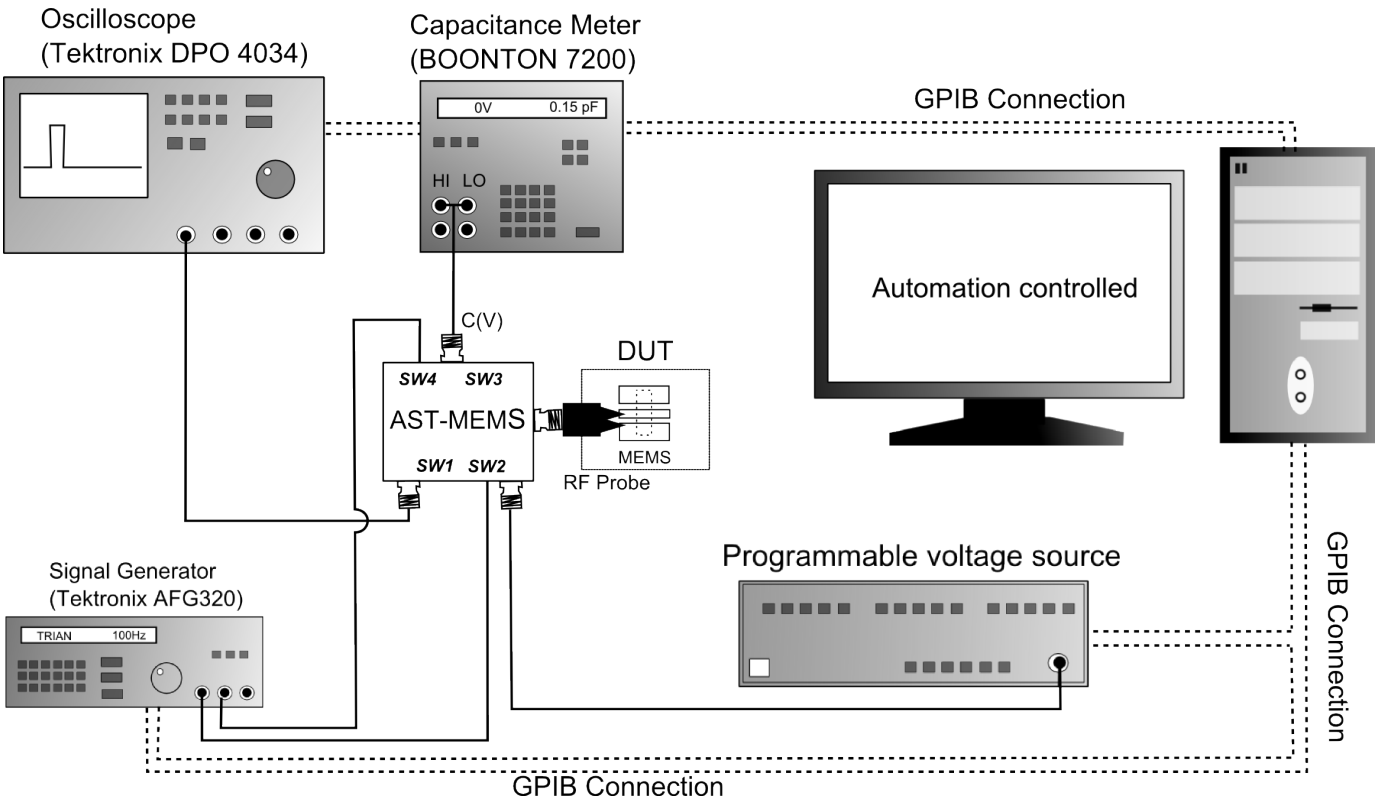
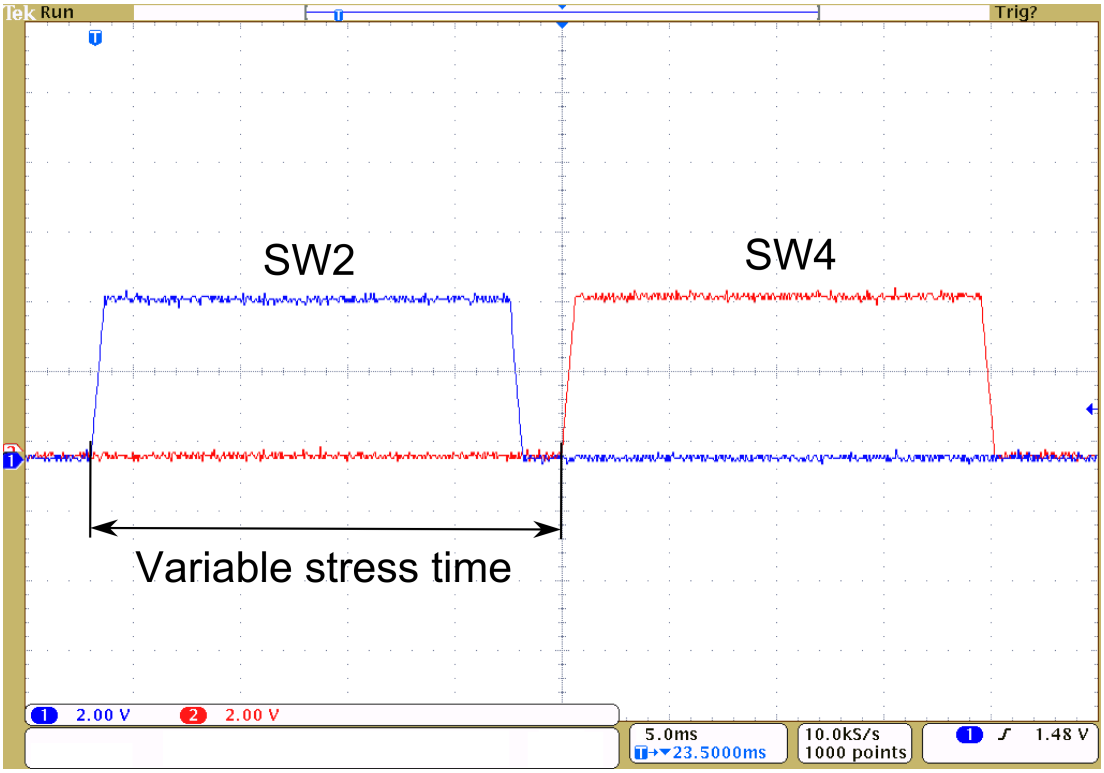
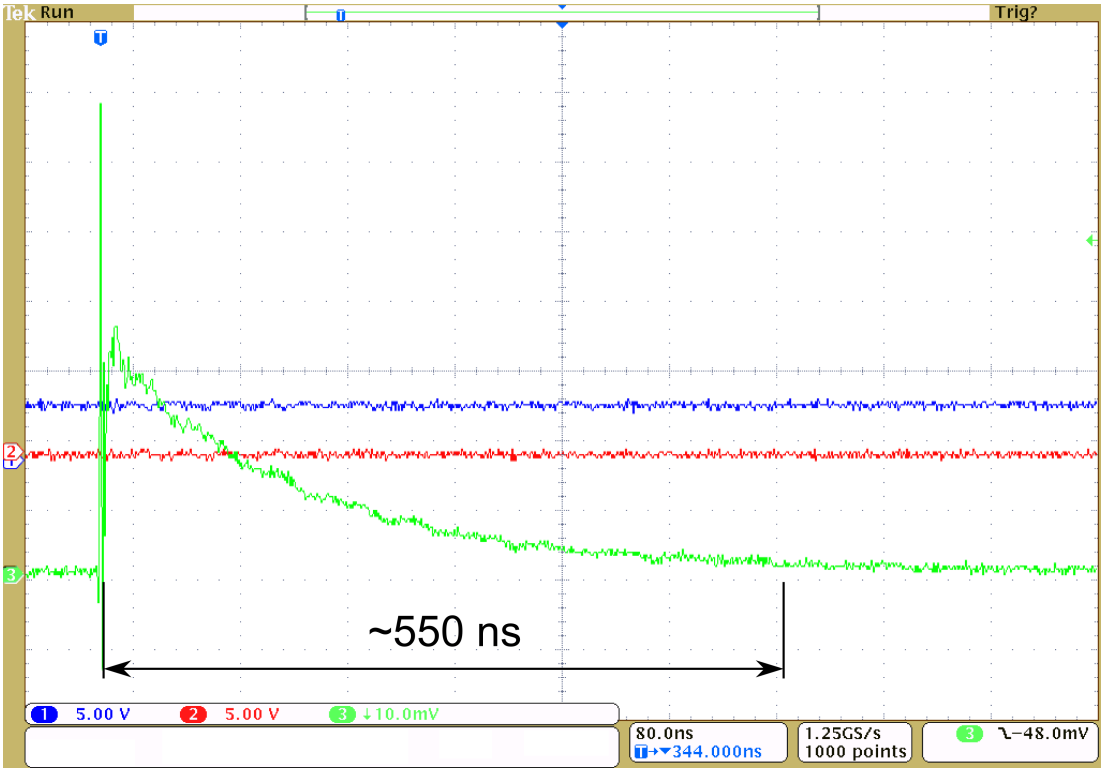


Fig. 5. The complete AST test bench schematic.



(a) The control signal time-charts of SW2 and SW4 relays



(b) The discharge waveform

Fig. 6. Measured time-sharts of the AST circuit response.

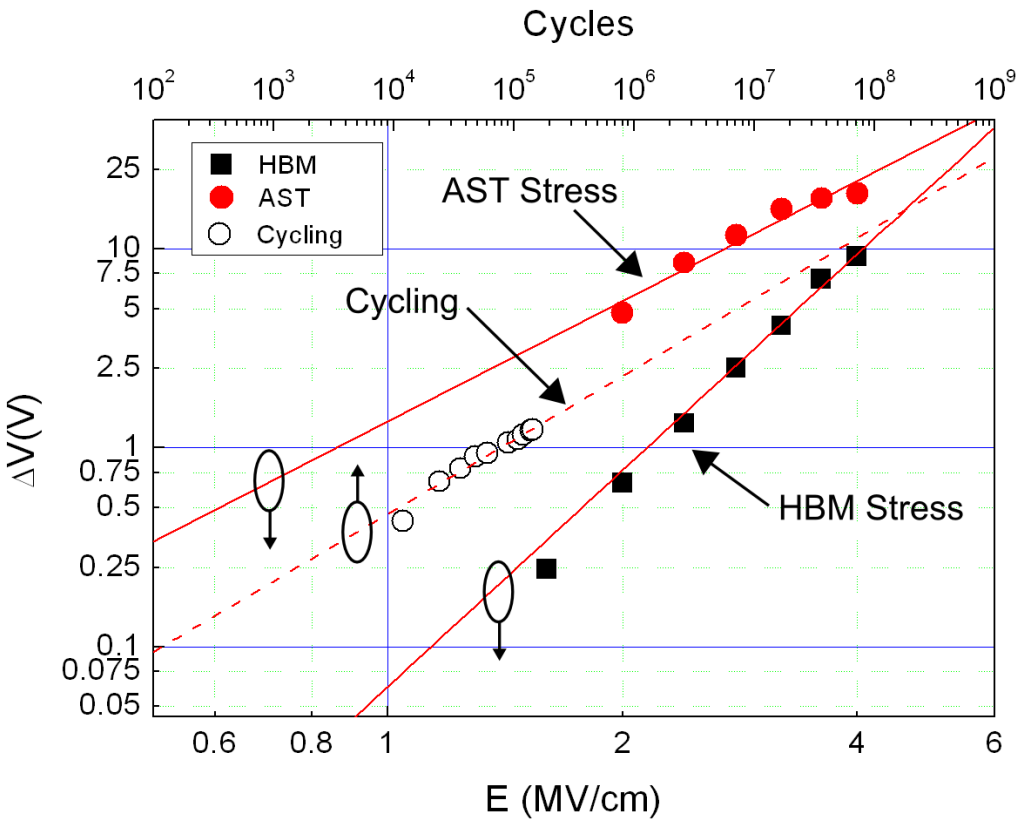


Fig. 7. Measurement results, the voltage shift due to charge accumulation vs. the electric field of the stress in accelerated condition and vs. the number of cycles in normal condition.