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# Reducing The Convergence Loss of 3-Dimensional Turbo Codes

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**Abstract**— This paper deals with the convergence loss reduction of a 3-dimensional turbo code combining both parallel and serial concatenation. This code is derived from the classical turbo code by concatenating a rate-1 post-encoder at its output. In order to reduce the observable loss of convergence at high error rates, we propose first a time varying construction of the post-encoded parity. Then, we analyse the association of the 3-dimensional turbo code with high order modulations, where both the systematic bits and the post-encoded parity bits are more protected than the other parity bits. Performance comparisons are made between the 3GPP2 standardized turbo code and the 3-dimensional 3GPP2 turbo code. The different stages are illustrated with simulation results, asymptotical bounds and EXIT charts.

**Keywords**—turbo code; iterative decoding; 3-dimensional turbo code; 3GPP2; convergence threshold; time varying trellis; turbo coded modulation.

## I. INTRODUCTION

The first application of the turbo principle concerned the error correcting codes and resulted in the invention of turbo codes (TCs) in the early nineties [1]. However, in spite of their performance in compliance with the theory developed by Claude Shannon in the middle of the twentieth century, TCs suffer from a flattening at medium-to-high signal to noise ratios. In order to improve the performance at very low error rates by raising the Minimum Hamming Distance (MHD), a hybrid concatenated code, called 3-dimensional turbo code (3D TC) was introduced in [2, 3]. It is based on the partial concatenation of a classical turbo code with a rate-1 post-encoder, which encodes only a fraction  $\lambda$  of the parity bits from the upper and lower constituent encoders. The fraction  $1 - \lambda$  of parity bits which is not re-encoded is directly sent to the channel or punctured to achieve the desired code rate. The value of  $\lambda$  can be used to trade-off performance in the waterfall region with performance in the error floor region. As shown in [2, 3], the 3D TC improves performance in the error floor compared to the TC, at the expense of an increase in complexity and a certain loss in convergence.

This paper is organized as follows. In Section II, we present the 3D TC. The code optimization issues are discussed in the same section, followed by a detailed study of the complexity increase of the 3D TC in Section III. Then, in Section IV, we discuss convergence issues and we propose time varying 3-

dimensional turbo codes as an alternative to reduce the observable loss of convergence. Furthermore, we analyze the association of 3D TCs with specific high order modulations to improve the performance of the 3D TC in the waterfall region. Finally, section V draws some conclusions.

## II. CODING SCHEME

### A. Encoding Structure

A block diagram of the 3D turbo encoder is depicted in Fig. 1. In our work, we focused on the 3GPP2 code, an 8-state binary turbo code, used in the third generation (3G) mobile phone communication systems [4]. The 3GPP2 turbo code is built from the parallel concatenation of two Recursive Systematic Convolutional (RSC) codes, with generator polynomials 13 (recursivity) and 15 (redundancy). The overall code rate before puncturing is  $1/3$ . A fraction  $\lambda$  of the parity bits from the upper and lower constituent encoders are grouped by a P/S multiplexer, permuted by a permutation  $\Pi'$ , and encoded by an encoder of unity rate. In [2, 3],  $\lambda$  is referred to as the permeability rate. Usually, very simple regular permeability patterns are applied. For instance, if  $\lambda = 1/8$  the bits to be post-encoded are chosen in the regular basis  $\{10000000\}$  for both the upper and the lower encoders.

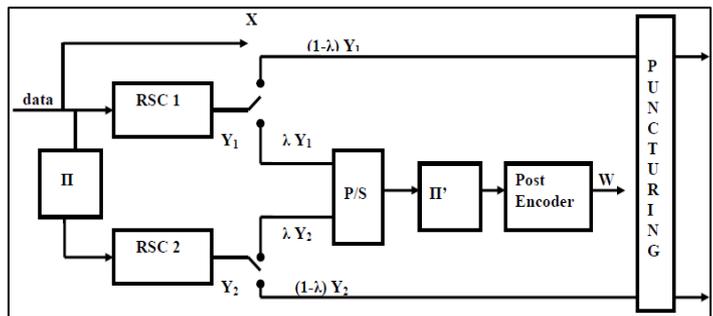


Figure 1. 3D turbo encoder structure. A fraction  $\lambda$  of the parity bits from both component encoders are grouped by a P/S multiplexer, permuted by the permutation  $\Pi'$ , and encoded by a rate-1 post-encoder.

### B. Choice of the Post-Encoder

The choice of the post-encoder influences the performance in both the waterfall and error floor regions. In general, the post-encoder must be simple to limit the complexity increase of the corresponding decoder. Low memory RSC codes satisfy

this requirement. Three linear RSC codes having memory 2 are given in Fig. 2. Besides, the convolutional code is made tail-biting [5] to prevent from any side effects as the initial state and the final state of the post-encoder are always the same. This requirement is important for real-time and demanding applications, such as TV broadcasting or videoconferencing, where very low error rates are sought for. Last but not least, the post-encoder must not exhibit too much error amplification, to prevent from a high loss in convergence (see [2, 3] for details). To complete the analysis in [2, 3], the choice of the post-encoder is justified by means of EXtrinsic Information Transfer (EXIT) [6] analysis.

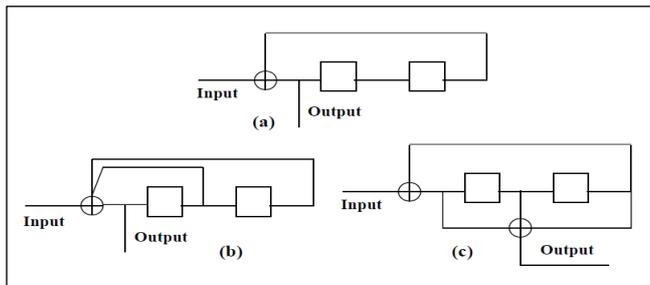


Figure 2. Possible linear post-encoder candidates with memory 2.

In Fig. 3 we report the EXIT curves for the three linear post-encoders of Fig. 2. When no a-priori information is available at the input of the pre-decoder (*i.e.* first iteration) the Mutual Information (MI) at its output is higher for post-encoder (a). In fact, code (a) has a corresponding decoder which only doubles the number of errors of its input at the first step of the iterative process, while code (b) will (roughly) triple the number of errors at the first step. The worst case occurs with code (c) because its decoder will make a mistake once every two bits in its entry.

Let us assume that a post-encoder, where the MI at its output is zero when there is no MI at its input (such as code (c)), has been selected. The worst case occurs when all the parity bits are post-encoded, which corresponds to high coding rates such as  $R = 2/3$  for  $\lambda = 1/4$  or  $R = 4/5$  for  $\lambda = 1/8$ . In this case, the error rate at the output of the corresponding pre-decoder at the first iteration will be 0.5. And the turbo decoder will have no parity to decode with at the first step of the iterative process. It will just be something catastrophic! Therefore, the EXIT analysis is a very important tool to select a post-encoder convenient at low but also at high coding rates.

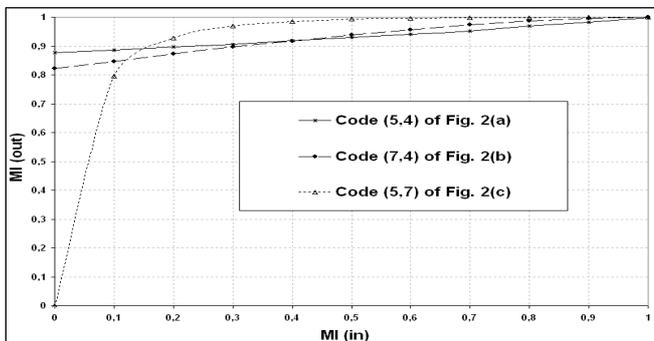


Figure 3. EXIT curves for different linear post-encoders.

In Fig. 4, we report the Frame Error Rate (FER) performance of the 3D 3GPP2 TC to compare it with that of the 3GPP2 TC for the block size 570 bits, at coding rate  $R = 1/3$  and  $\lambda = 1/4$ . We observe a loss of convergence in the waterfall region when the post-encoder of Fig. 2(a) is used. But, as expected, this loss of convergence increases when the post-encoder of Fig. 2(b) is used (see Fig. 4). The largest loss of convergence was observed when the code of Fig. 2(c) is used. Other simulations at high coding rates, such as for  $R = 2/3$  and  $\lambda = 1/4$ , show that the 3D TC does not converge when the code of Fig. 2(c) is selected to be the post-encoder. Therefore, from a convergence point of view, code (a) has been selected to be the post-encoder in different simulations of the 3D TC.

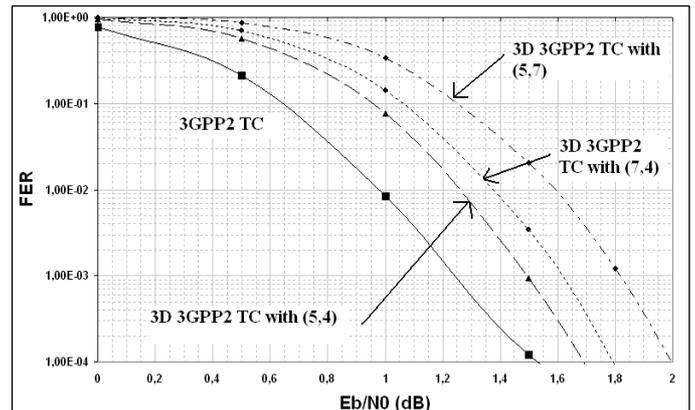


Figure 4. FER performance of the 3D 3GPP2 TC with  $\lambda = 1/4$  for  $k = 570$  bits,  $R = 1/3$  and comparison with the 3GPP2 TC. All simulations used the Max-Log-MAP algorithm with 10 decoding iterations.

### C. Permutations $\Pi$ and $\Pi'$

The 3D TC is characterized by two permutations denoted by  $\Pi$  and  $\Pi'$ , as shown in Fig. 1. In theory, both permutations should be jointly optimized. However,  $\Pi$  is the internal permutation of the TC, and we keep  $\Pi$  unchanged with regard to the original code for reasons of backward compatibility.  $\Pi'$  is used to spread a fraction  $\lambda$  of the parity bits before feeding them to the post-encoder. To optimize  $\Pi'$  different types of interleavers were tested starting from random permutations to more structured permutations such as the regular interleaver. It was observed through the different simulations that the important property is the spread. In fact, performance of an interleaver is degraded by low values of spread. And the regular permutation is an interleaver achieving a spread of  $\sqrt{2k}$  [7], where  $k$  is the size of the frame. So it performs better than a random interleaver in terms of MHD and convergence.

Fig. 5 shows the simulated performance of the 3D 3GPP2 TC with an interleaver  $\Pi'$ , random but also regular, for code rate  $R = 1/2$ ,  $\lambda = 1/8$  and  $k = 762$  bits. Performance of the 3D 3GPP2 TC using a random permutation  $\Pi'$  is not good in terms of MHD, but also in terms of convergence. However, the use of a regular permutation  $\Pi'$  results in an increase in the MHD of the 3D 3GPP2 TC by more than 60 % compared to the standardized 3GPP2 turbo code; which provides a gain of more than 2 decades in the error floor. These simulation results were confirmed with the asymptotical bounds as shown

in Fig. 5. Note that the permeability rate has an effect on the performance of the 3D TC similar to the doping ratio concept of [8].

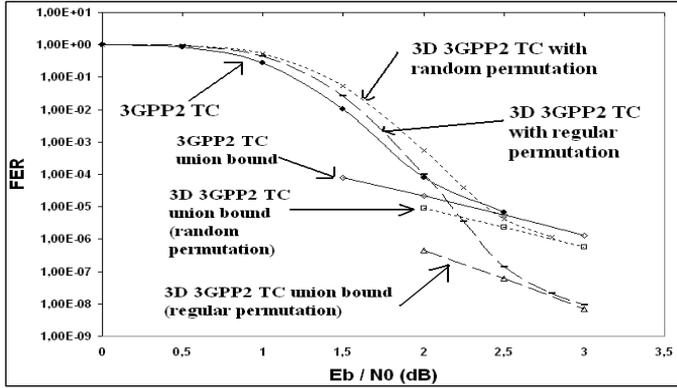


Figure 5. FER performance of the 3D 3GPP2 TC with  $\lambda = 1/8$  for  $k = 762$  bits,  $R = 1/2$  and comparison with the 3GPP2 TC. All simulations used the Max-Log-MAP algorithm with 10 decoding iterations. The all-zero iterative decoding algorithm [9] was applied to obtain the distance spectrum.

### III. COMPLEXITY ANALYSIS OF 3-DIMENSIONAL TURBO DECODERS

In [3], the complexity increase was estimated to be less than 10% with respect to classical 2-dimensional TC. In this section, we propose a more detailed analysis of the complexity of a 3D TC. In fact, compared to a classical turbo decoder, the additional complexity of the 3D turbo decoder is mainly due to the implementation of the binary 4-state decoder but also to the calculation of the extrinsic information about the post-encoded parity bits. Let us consider a RSC code with the following parameters:

- $v$  is the memory length of the code,
- $n$  is the number of coded bits provided by the encoder at each trellis stage (when no puncturing is performed),
- and  $k$  is the trellis length. It is also the length of information sequence, in terms of binary bits.

Table I summarizes the resulting complexity for the process of a trellis stage, or equivalently of an information bit. The corresponding numerical values are given in Table II. In order to compare the complexity of the different families of decoders, it is assumed that addition/subtraction and compare-select operators have similar hardware complexity.

On the other hand, the memory requirements for the turbo decoder are the amount of both RAM and ROM memory. A very small amount of ROM memory is required to store the turbo code permutation parameters. This amount of memory is the same for all coding schemes under consideration. But for the RAM memory, two input buffers are necessary for each data sequence, including systematic and parity bits, stemming from the transmission channel. Thus, if  $k$  is the length of the information sequence,  $2k/R$  input samples, quantized on  $q_x$  bits, have to be stored at the decoder input. In addition,  $2k$  extrinsics (dual-port RAM) need to be stored (quantized on  $q_x + 1$  bits). For a 3D TC, additional extrinsics ( $2 \lambda k$ ) related to re-encoded redundancy bits need to be stored. Then, the

hardware decision at the decoder output requires  $k$  memory bits (single-port RAM). Finally, sliding window [10] processing is performed to reduce the amount of memory required by SISO decoding; and state metrics at the window sides have to be stored at each iteration.

TABLE I. COMPUTATIONAL COMPLEXITY OF THE MAX-LOG-MAP ALGORITHM.

	Add (or subtract)	Compare-select
Branch metrics (forward or backward recursion)	$2^{n+1} - 2$	
One step of recursion (forward or backward)	$2^{v+1}$	$2^v$
A posteriori LLRs and hard decision	$2^{v+1} + 1$	$2^{v+1} - 1$
Extrinsic LLRs for information symbols	4	
Extrinsic LLRs for redundancy bits	2	$2^{v+1} - 2$
Total computational requirement per information bit for classical TC	$3 * 2^{v+1} + 2^{n+2} + 1$	$2^{v+2} - 1$
Total computational requirement per information bit for 3D TC	$3 * 2^{v+1} + 2^{n+2} + 3$	$3(2^{v+1} - 1)$

Table II compares the hardware complexity of the 3GPP2 turbo decoder and the corresponding 3D decoder for the worst case, when  $\lambda = 1/8$  is used, in terms of memory size:  $k = 1530$  bits and  $R = 1/2$ . Table II provides:

TABLE II. SUMMARY OF COMPLEXITY ANALYSIS FOR 3GPP2 AND 3D 3GPP2 TURBO DECODERS FOR  $k = 1530$  BITS,  $R = 1/2$  AND  $\lambda = 1/8$ .

	Overall SISO HW complexity (number of add / compare-select operators)		
	$P = 1$	$P = 2$	$P = 4$
3GPP2	112 = $C_1$	224 = $C_2$	448 = $C_4$
3D TC based on 3GPP2	176 = $C_1 + 57\%$	304 = $C_2 + 36\%$	560 = $C_4 + 25\%$
RAM (equivalent single-port memory in bits) Input quantization: 6 bits			
	$P = 1$	$P = 2$	$P = 4$
3GPP2	101,510 = $M_1$	106,630 = $M_2$	126,251 = $M_4$
3D TC based on 3GPP2	= $M_1 + 9.2\%$	= $M_2 + 8.8\%$	= $M_4 + 8.0\%$

- the complexity of the overall hardware dedicated to SISO decoding with the Max-Log-MAP algorithm in terms of add / compare-select operators,
- the amount of RAM memory required for the implementation, in terms of equivalent single-port RAM bit (1 dual-port RAM bit = 2 single-port RAM bit).

The number of SISO decoders placed in parallel,  $P$ , depends both on the required data throughput and on the hardware implementation technology. Table II presents complexity figures for  $P = 1$ ,  $P = 2$  and  $P = 4$ . This complexity assessment does not take the size of the SISO internal operands

into account. The implementation of the control part (state machines) and interleavers is not taken into account either. Note that the complexity of the state machines does not differ a lot between the different families of decoders.

To conclude, the first estimation of the complexity of in [3] was optimistic. And Table II shows that the more important the degree of parallelism is, the less the impact (additional complexity) of using a 3D TC is.

#### IV. REDUCING THE CONVERGENCE LOSS OF 3-DIMENSIONAL TURBO CODES

The 3D TC improves performance in the error floor compared to the TC, at the expense of a loss in convergence and an increase in complexity. In this section, we propose a time varying construction of the post-encoded parity bits to reduce the loss of convergence at high error rates. Then, we show that there is no need to use the time varying technique when the code is associated with a high order modulation because the observable loss of convergence "disappears" when a specific permutation before the mapping is used.

##### A. Time Varying 3-Dimensional Turbo Codes

1) *Time Varying Encoding*: The proposed time varying (TV) encoding consists in alternating two redundancies in time  $W_1 = 4$  and  $W_2 = 7$ , instead of having only one. It is a mixture of the code (5,4) of Fig. 2(a) and the code (5,7) of Fig. 2(c) to benefit from the better performance of the latter in the error floor region and that of the code (5,4) in the waterfall region. In fact, the EXIT curves in Fig. 3 corresponding to the post-encoders of Fig. 2(a) and 2(c) cross around input MI 0.1. For high input MI the curve related to code (c) indicates a better behavior in the error floor region. For this reason, the principle of the time varying encoding is to combine the two encoders. Unfortunately, the distance of the time varying code (5,4:7) is only 2 compared with 3 for the RSC code (5,4) and 5 for the RSC code (5,7).

To avoid this problem, the idea proposed in [11] was to replace some redundancies 4 by other redundancies 7 to get closer to the code (5,7). And the replacement period is denoted by  $L$  (see [12] for details).

2) *EXIT chart analysis*: To generate the EXIT chart of the 3D TC, we have to consider that the two 8-state decoders exchange also extrinsic information about the post-encoded parity bits with the 4-state SISO pre-decoder. As the extrinsic information about these parity bits changes every iteration, the curves of mutual exchange between the two decoders change from an iteration to the other one.

Fig. 6 shows an EXIT chart of a 3-dimensional TV turbo code for  $E_b/N_0=1.58$  dB, where  $E_b/N_0$  denotes the signal-to-noise ratio, at code rate  $R=2/3$  and  $\lambda=1/4$ . The transfer characteristics of the two decoders are no more symmetric. In fact, for the post encoder, two redundancies  $W_1=4$  and  $W_2=7$  are alternated in time, but  $W_1$  is periodically replaced by  $W_2$  with period  $L=30$ . This replacement generates the asymmetry between the transfer characteristics of the two 8-state SISO

decoders. Note that, after the seventh iteration, the transfer characteristics remain almost unchanged.

The convergence threshold of the 3D TV turbo code is 1.58 dB for code rate  $R=2/3$  and  $\lambda=1/4$ , i.e. the minimum signal to noise ratio where the tunnel between the EXIT curves opens. These results were confirmed by simulations of the code. On the other hand, the convergence threshold of the TC at code rate  $R=2/3$  is estimated around 1.49 dB and that of the 3D TC is 1.67 dB. As a conclusion, the use of TV 3-dimensional 3GPP2 TC reduced the loss of convergence by 50% from 0.18 dB (1.67 -1.49) to 0.09 dB (1.58- 1.49) at code rate  $R=2/3$  and  $\lambda=1/4$ . And among the simulated cases it was observed that the time varying parity construction reduces the observable loss of convergence by 10% to 50% of the value expressed in dB.

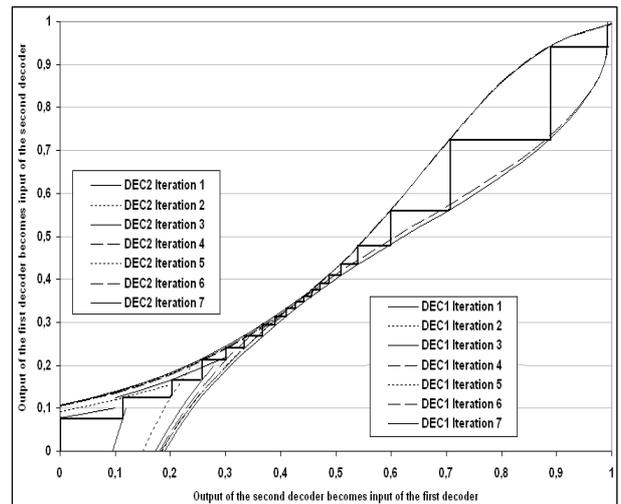


Figure 6. EXIT chart of a time varying 3D TC at code rate  $R=2/3$ ,  $\lambda=1/4$  and  $E_b/N_0=1.58$  dB.

##### B. Turbo Coded Modulations using 3D TCs

1) *Transmission scheme*: We consider the coded modulation scheme depicted in Fig. 7, based on the so-called pragmatic or BICM approach [13]. Fig. 7 shows a 3D turbo encoder and a 16-QAM modulator that follows a Gray mapping. At the receiver side, the demapper computes the Log Likelihood Ratio (LLR) related to each bit of the information sequence. This symbol-to-bit LLR calculation is followed by a 3D turbo decoder that uses the MAP algorithm. It is known that among the four bits forming a symbol in 16-QAM, the average probability of error is smaller for the first and third bits than for the second and fourth bits [14].

After turbo encoding, several constellation mappings, all compliant with Gray labeling, were performed. First, the mapping is uniformly distributed on the entire constellation. Then the systematic bits are protected in priority, and all the other bits are distributed the same way. Finally, the systematic bits as well as the post-encoded parity bits are more protected by the 16-QAM modulation than the other non re-encoded parity bits. This choice is made because the systematic bits, as well as the post-encoded parity bits, are used by the two

decoders during the decoding process. And protecting them should reduce the loss of convergence.

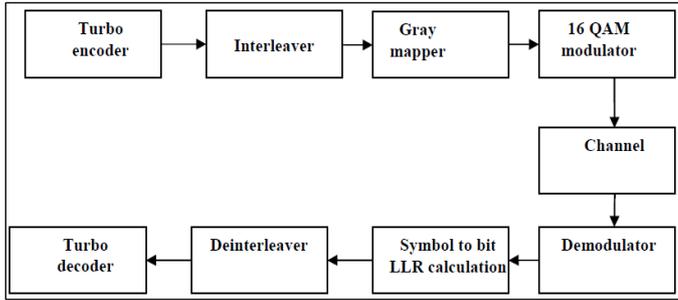


Figure 7. Transmission scheme.

2) *Simulation Results:* The FER performance of the 3D 3GPP2 TC has been simulated with  $\lambda = 1/8$  at code rate  $R = 1/3$  for  $k = 2298$  bits. Fig. 8 shows that the use of the 16-QAM modulation, as explained above, allows the observable loss of convergence of the 3D 3GPP2 TC to be reduced and even be transformed into a gain in the waterfall region of 0.22 dB compared with the 3GPP2 standardized TC. Whereas, for a QPSK modulation, the convergence loss of the 3D TC was estimated to 0.26 dB at code rate  $R = 1/3$  and  $\lambda = 1/8$ . These simulation results were confirmed by an EXIT chart analysis. In fact, the convergence threshold of a TC with 16-QAM modulation at code rate  $R = 1/3$  is 2.08 dB and that of the 3D TC with 16-QAM modulation, where the systematic bits and the post-encoded parity bits are well protected, is 1.86 dB at code rate  $R = 1/3$  and  $\lambda = 1/8$ . This confirms the observed gain of 0.22 dB in the waterfall region.

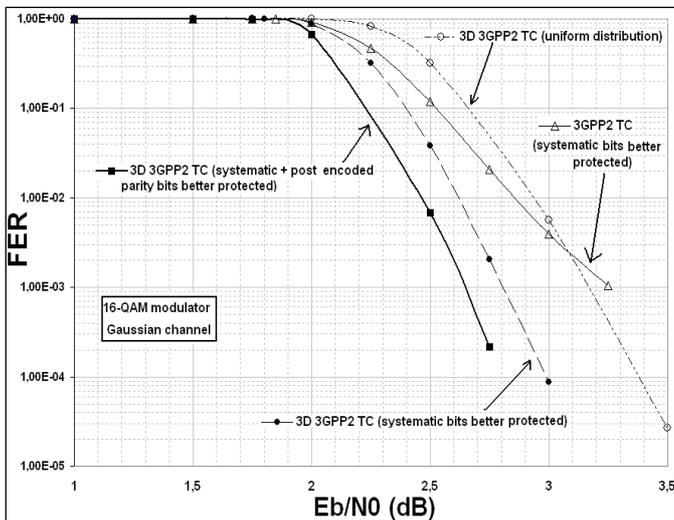


Figure 8. FER performance of the 3D 3GPP2 TC with  $\lambda = 1/8$  for  $k = 2298$  bits,  $R = 1/3$  and comparison with the 3GPP2 TC. All simulations used the MAP algorithm with 10 decoding iterations and 16 QAM modulation.

## V. CONCLUSIONS

The 3D TC, recently introduced by Berrou *et al.*, calls for both parallel and serial concatenation and increases the MHD

with respect to the classical TCs. In this paper we discussed how to choose a post-encoder by means of an EXIT analysis. Then, a complexity study of 3D TCs was presented to estimate the additional complexity. When high throughputs are required for a given application, many processors can be placed in parallel; which decreases the relative additional complexity of the 3D coding scheme. Furthermore, we proposed an approach to reduce the observable loss of convergence of 3D TCs at high error rates by using a TV construction of the post-encoded parity. This technique allows reducing the loss of convergence by 10% to 50%. However, when the code is associated with high order modulations, there is no need to use a TV trellis and a specific mapping allows obtaining even a gain in the waterfall region. Therefore, the 3D TC is adapted to be used in high spectral efficiency transmission systems

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