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HIGH-VOLTAGE LOW POWER ANALOGUE-TO-DIGITAL CONVERSION FOR ADAPTIVE ARCHITECTURES OF CAPACITIVE VIBRATION ENERGY HARVESTERS

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Abstract: This paper presents a design and modeling of a block allowing converting a high voltage into a digital code which is used in a smart adaptive conditioning circuit to calibrate an electrostatic harvester for vibration energy. A smart energy management in the harvester is needed to achieve an optimal conversion of the vibration energy. This block is achieved with a successive approximation analogue-to-digital converter (SA ADC) and a voltage divider to reduce the voltage applied on the ADC. The design is done in Austrian Microsystem CMOS035HV technology. This study is validated by VHDL-AMS/ELDO modeling for the harvester, the divider and the harvester.

Keywords: Energy harvesting, successive approximation ADC, VHDL-AMS, calibration, MEMS.

INTRODUCTION

The energy capacity, as well as lifetime of the existing sources is limited, and alternative energy sources are needed. Extracting the power from the ambient energy sources such as light, temperature gradients, and mechanical vibration is therefore a subject of research. The energy harvesting source converts the mechanical energy to electrical energy using an electrostatic transducer, which operates as a variable capacitor implemented in a MEMS technology. The harvester needs a smart control to achieve optimal electromechanical conversion of the vibration energy. This control requires some measurements of high voltages (10-50 V) and should consume low power. Thus, a low power ADC must be used. Power saving can be achieved in ADC through the selection of a suitable low-power ADC. The successive approximation ADC is known as one of the best candidates in terms of low-power [2]. In this paper, we explain how we use the SA ADC and the voltage divider in the harvester conditioning circuit.

HARVESTER OPERATION

An electrostatic energy harvester consists of a mechanical resonator, an electromechanical transducer (based on MEMS technology) [3] and an electrical conditioning circuit managing the operation of the transducer and providing an interface with the load [1] as shown in Fig.1. One of the possible architecture of conditioning circuit, initially proposed by Yen [4], is composed of two main parts: a charge pump and a flyback circuit controlled by a switch SW (*Fig. 1*). The charge pump circuit transfers electrical charges from a large initially pre-charged capacitor C_{res} toward a small temporary storage C_{store} with the use of variable transducer capacitor Cvar. The energy for this charge pumping comes from the mechanical domain through the variations of the transducer capacitor. During the pumping, the converted energy is stored in the C_{store} capacitor, the C_{store} voltage U_{store} increases and C_{res}

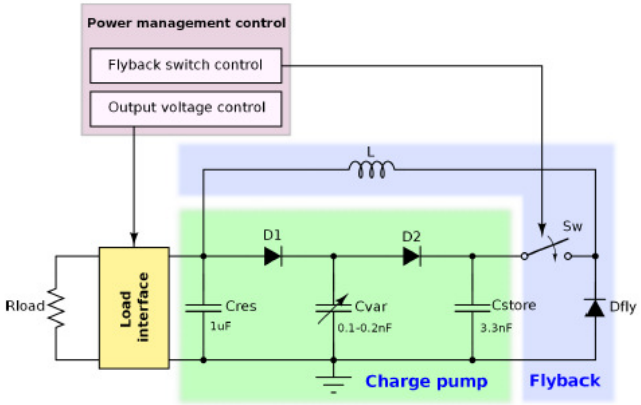

Fig. 1: Conditioning circuit of the vibration harvester.

voltage U_{res} decreases very slightly (since C_{res} >> C_{store}). *Fig. 3* shows that the energy conversion is maximal for a particular range (U_1, U_2) of U_{store}[1] and when U_{store} reaches the upper border of this range U_2, a part of the charges of C_{store} must be returned to C_{res}, so to put U_{store} at the low limit U_1 of this range. This is performed by the inductive flyback circuit. Topologically, the flyback circuit is similar to a Buck DC/DC converter, but with an output voltage U_{res} needed to be pulled up as efficiently as possible using the energy of C_{store}. As soon as U_{store} reaches U_2, the switch SW is set on by external control blocks and C_{store} starts to discharge on C_{res} through the inductor. When U_{store} is reduced to U_1, the switch becomes off and the inductor discharges on C_{res} through the diode D3. After this, a new charge pump operation cycle starts. From theoretical investigation [5] U_1 and U_2 parameters are calculated as:

$$U_1 = U_{res} + 0.1(U_{store\max} - U_{res}) \quad (1)$$

$$U_2 = U_{res} + 0.6(U_{store\max} - U_{res})$$

Here, U_{store} max is the saturation voltage of the charge pump given by [4]:

$$U_{store\ max} = \frac{C_{\max}}{C_{\min}} U_{res} \quad (2)$$

where C_{max} and C_{min} are the maximal and minimal values which takes the transducer capacitance. From eq. (2), $U_{store\ max}$ depends on the ratio between C_{max} and C_{min} that are, in turn, related to the resonator vibration parameters such as frequency and amplitude, which usually vary in the time. Consequently, $U_{store\ max}$ voltage is not a fixed value and moreover cannot be measured directly since during charge pumping U_{store} never reaches the saturation [1]. However, that $U_{store\ max}$ can be measured in an ad-hoc calibration cycle, which repeats periodically (much more rarely then a charge pump+flyback cycle).

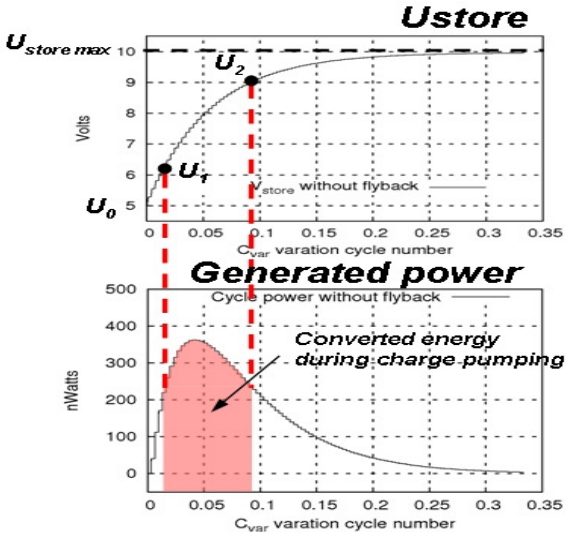

Fig. 3: Operation of the harvester with basic conditioning circuit architecture.

In order to calculate U_1 and U_2 during the system calibration, we need to measure $U_{store\ max}$ and U_{res} (High Voltage). Consequently, to interface analog voltages with the digital electric circuit, we need to use a voltage divider and an analog-to-digital converter. Vibration energy harvesters provide low values of powers (tens microwatts), hence, the conditioning electronics, including ADC, should consume as few as possible. In this work, we demonstrate the design of a very low power consumption successive approximation ADC.

SUCCESSIVE APROXIMATION ADC ARCHITECUTRE

In *Fig. 2*, we can see how different parts of the successive approximation ADC are connected. In our topology, the signal is sampled in the first clock cycle and is converted in the next N clock cycles, where N is the number of bits. The sample and hold operation is achieved with the use of the digital to analogue converter (DAC), when it is set in"*sampling*" mode. The DAC, allowing to achieve the successive approximation of the input voltage value, contains an array of binary weighted capacitors whose topology can be reconfigured by switches. The DAC output is connected to the negative input terminal of the comparator as it is shown in *Fig. 4*, while the common mode voltage U_{cm} is connected to the positive input terminal and the comparator output is connected to the control unit. The control unit represents the successive approximation register (SAR) that controls the DAC switches allowing to switch capacitors terminals to the three reference voltages: the supply voltage U_{dd}, the common mode voltage $U_{cm} = U_{dd}/2$ and the ground *gnd*. It generates the output digital word representing the digitally approximated input voltage. This ADC uses 2 digital clocks F_{start} to sample the signal and F_{clock} internal clock that equals to $(N+1).F_{start}$. This architecture was described in details in [6].

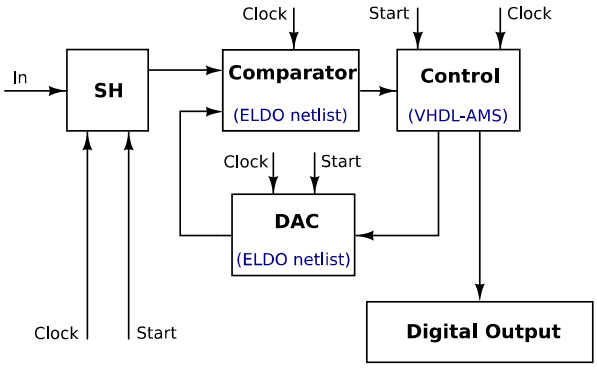

Fig. 2: Successive approximation ADC architecture.

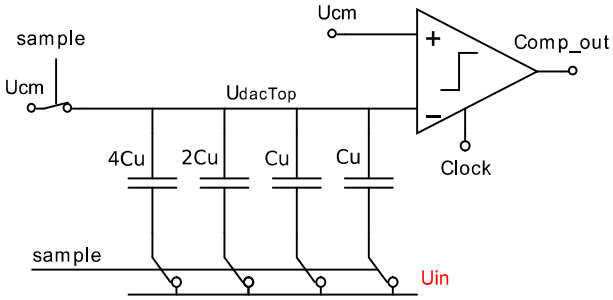

Fig. 4: Sampling mode in successive approximation ADC with 4 bits (given for example).

Successive approximation ADC modes

The conversion of the ADC is achieved in 3 different modes. In the first half of the first clock cycle, the input signal is connected to the bottom plates of the DAC capacitors while the upper plates are connected to U_{cm}, this is the *sampling* mode and corresponds to the configuration shown in *Fig. 4*. In the second half of the first clock cycle, all the bottom plates are connected to U_{cm}, this is the *inversion* mode. After the first cycle, the control unit checks the comparator output (*comp_out*). If it is high, it connects the largest capacitor bottom plate to U_{dd}, if it is low; the control unit connects the largest capacitor bottom plate to gnd. This mode is called *charge redistribution* mode. The same is repeated with all capacitors in the array, in N clock cycles. At i^{th} clock cycle, the output of the comparator corresponds to i^{th} bit of the output ADC word. This bit value is saved by the control unit and after the end of the charge redistribution mode; the digital output of the control unit is equal to the digitally approximated input voltage. In *Fig. 5*, we can see how the voltage of the

DAC top plates changes in every mode on the example of 8-bit successive approximation ADC.

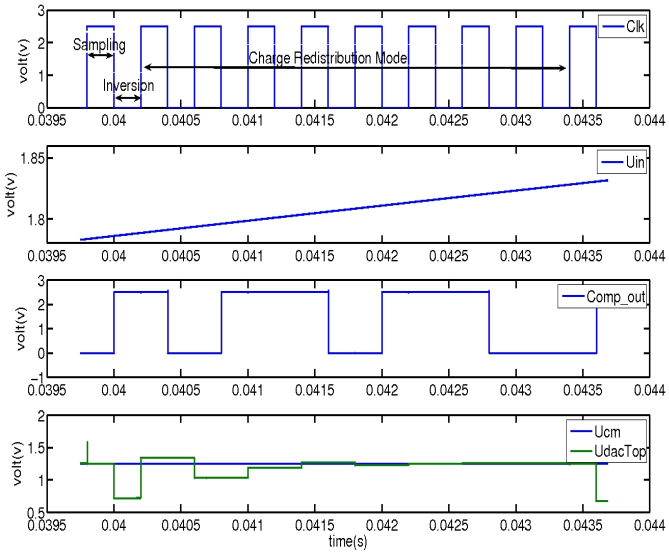

Fig. 5: 8-bit successive approximation ADC operation.

In our system, we use 8-bit SA ADC with sampling frequency F_{start}=277.8 Hz, i.e one sample every 3.6ms, F_{clock}=2.5 KHz and 2.5 V supply voltage.

VOLTAGE DIVIDER CIRCUIT

In present work the division factor of divider is 20, since the maximal value for U_{store} is limited by 50V and the voltage supplied by the ADC is 2.5V. The proposed divider consists of 2 resistors connecting in series, 2 switches and an output capacitor as shown in *Fig. 6*. At every sample, resistors divide U_{store} by 20, and the divided voltage is stored in the capacitor C_{div}, so that the successive approximation ADC can sample this value. The clock used in the divider (CLK_DIV) has the same sampling frequency but with the smaller pulse width to decrease the power consumption.

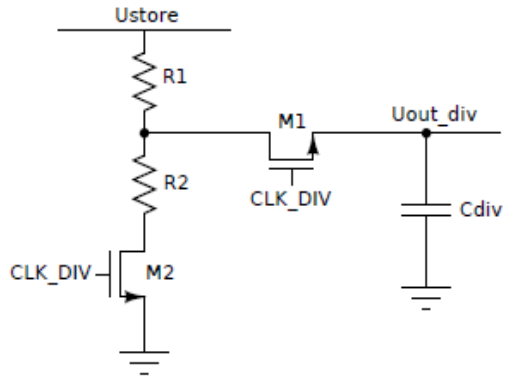

Fig. 6: Voltage divider circuit interfacing the harvester with the ADC

The relation between U_{store} and the divider output U_{out_div} can be calculated based on equation:

$$\frac{U_{store}}{U_{div\_out}} = \frac{R_2 + R_1}{R_2} = 20 \quad (3)$$

Hence, from eq. (3) we have $R_1 = 19R_2$. The time of charging C_{div} is determined by:

$$\tau = R_1 \parallel R_2 . C_{div} \quad (4)$$

The presented voltage divider circuit is designed in CMOS 0.35µm high voltage technology of Austrian Microsystem (AMS035HV).

CALIBRATION OF THE HARVESTER USING SUCCESSIVE APPROXIMATION ADC

In this section, the whole system is connected; the divider circuit is interface between the harvester and the ADC, the ADC output bits are connected to the flyback control switch as shown in *Fig. 7*. The flyback control enables the ADC during the calibration mode and disables it in normal mode.

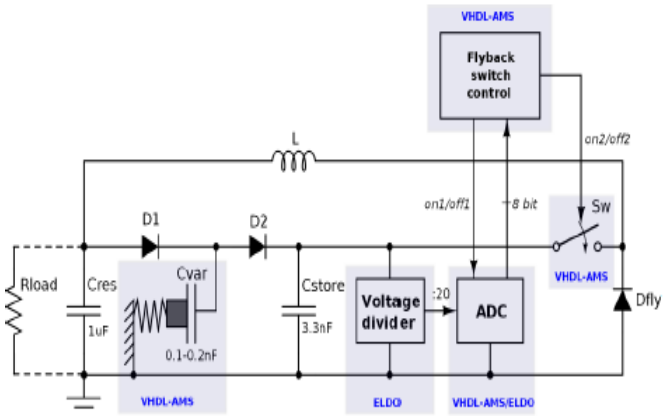

Fig. 7: Functional schema of harvester system.

The calibration cycle starts with putting U_1 to a very low value (zero), so that C_{store} voltage becomes equal to C_{res} voltage. During 20 ms U_{store} remains at the U_{res} value, which gives to the ADC enough time to measure it. After that, the flyback switch control orders the charge pumping to start, and U_{store} starts to increase, up to the saturation. During this charge pumping, the voltage U_{store} is measured with 3.6 ms sampling step. The goal of this measurement is to detect the $U_{store\ max}$ value.

The digital values corresponding to the neighboring samples of U_{store} are compared, and when there are 2 consecutive steps have the same value, their value is considered as measured $U_{store\ max}$ (it means that U_{min} mentioned equals to the ADC resolution). At the end of the calibration cycle the flyback switch control block turns off the ADC and U_1 as well as U_2 are calculated. Then, the normal mode (periodic charge pump+flyback cycles) starts till the next calibration cycle begin as it is shown in *Fig. 8*.

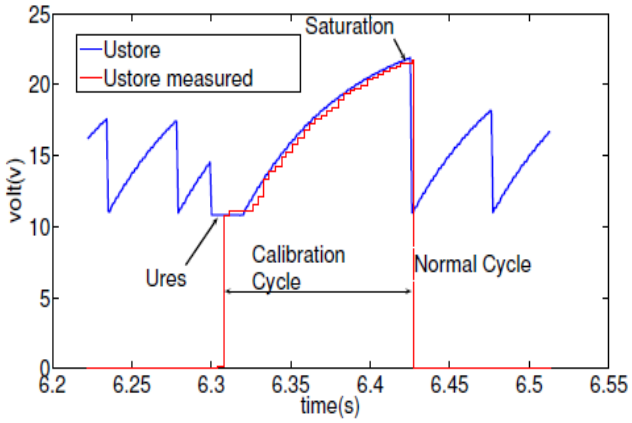

Fig. 8: Calibration cycle of the harveste.r

MODELATION RESULTS

In this paper, we present simulation results which demonstrate the harvester operation with ADC during almost 11 seconds. Here, calibration cycles repeat every 900 ms, such a low interval is chosen in order to reduce the modeling time, in reality the calibration phase should be less frequent (tens of seconds) to reduce the power consumed. In the top part of the *Fig. 9*, U_{store} is plotted together with the measured U_{store} voltage. We can see that during the calibration cycle there is a good matching between them because of the good resolution of the ADC. In the bottom part of the *Fig. 9*, the real U_{res} is plotted with the measured U_{res} voltage. The increase in the real U_{res} value is explained by the accumulation of the energy of the system (i.e., a normal harvester operation). As we see, U_{res} is measured only once during the calibration cycle. In the normal operation mode between calibration cycles ADC is deactivated by the signal off1. The measured $U_{store\ max}$ value is reset to 0 and the equivalent U_{res} is saved until the next calibration cycle.

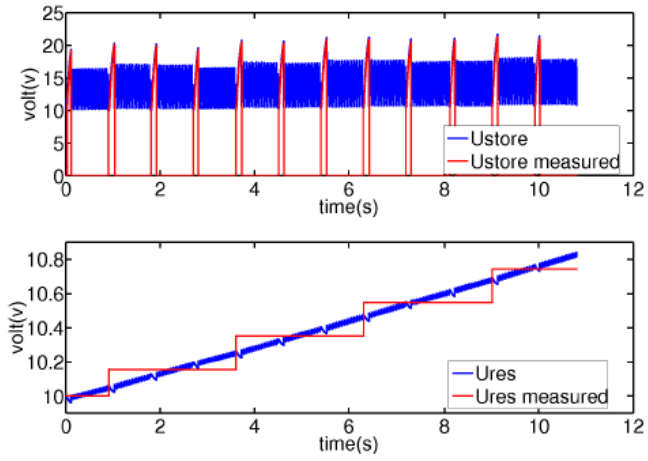

Fig. 9: Simulation result of harvester operation using the SA ADC.

CONCLUSION

In this paper, we presented the architecture design and modeling of the electrostatic vibration energy harvester with a successive approximation ADC and a voltage divider. The use of such ADC in energy harvester application is suitable for low power consumption. The whole system of the harvester including the SA ADC is simulated with VHDL-AMS/ELDO mixed model using the cadence environment. Simulation results of the harvester with the use of 8-bit SA ADC demonstrate a good matching between U_{store} and the measured from ADC $U_{store\ mes}$ during the calibration cycle. The estimated power consumption of the ADC is around 1.25µW for one step conversion. The comparator is the dominating block in power consumption of ADC with the used sampling frequency and 8-bit resolution, whereas the DAC has much less contribution.

REFERENCES

[1]. Andrii Dudka, Dimitri Galayko, and Philippe Basset.Vhdl-ams modeling of adaptive electrostatic harvester of vibration energy with dual-output dc-dc converter. *In IEEE International Behavioral Modeling and Simulation Conference (BMAS 2009).*

[2]. Michael D. Scott, Bernhard E. Boser, and Kristofer S. J. Pister. An ultra low-energy adc for smart dust. *IEEE JOURNAL OF SOLID-STATE CIRCUITS, JULY 2003.*

[3]. P. Basset, D. Galayko, A. M. Paracha, F. Marty, A. Dudka, and T. Bourouina. A batch-fabricated and electret-free silicon electrostatic vibration energy harvester. *Journal of Micromechanics and Microengineering, 2009.*

[4]. B. C. Yen and J. H. Lang. A variable-capacitance vibration-to-electric energy harvester. *IEEE TCAS, 53(2):288–295, february 2006.*

[5]. D. Galayko and P. Basset. Mechanical/electrical power-aware impedance matching for design of capacitive vibration energy harvester. *In PowerMEMS2008 workshop, Sendai, 2008.*

[6]. Mootaz Allam. Systematic design of a successive approximation analog-to-digital converter. *Master's thesis, Faculty of Engineering,Cairo University, Giza, Egypt, 2008.*