Mixed Cartesian Feedback for Zero-IF WCDMA Transmitter

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***Abstract*—In this paper, a new adaptive power amplifier (PA) linearization technique is presented. The idea is to consider a classic WCDMA Zero-Intermediate Frequency (Zero-IF) transmitter with a modified Cartesian feedback (CFB) loop. The new transmitter architecture consists of an analog stage including forward I/Q modulator and feedback I/Q demodulator and a digital stage adjusting the phase rotation around the loop. The digital phase-alignment system consumes 2.94 mW (tree time less than a full-analog system).**

***Keywords*—Cartesian feedback loop; WCDMA transmitter; Architecture matching algorithm**

I. INTRODUCTION

Third generation wireless communication standard WCDMA uses non-constant envelope modulation techniques to increase spectral efficiency for high data rates [1]. Those modulations require high linear radio-frequency (RF) power amplifier (PA), whereas, power efficiency is maximized when the PA operates at its non-linear region. The current state of the art is to design a moderately linear PA and to employ some linearization technique. The amplifier operates as close as possible to saturation, maximizing its power efficiency, and the linearization system maximizes the spectral efficiency in this near-saturated region. Many methods (analog or digital) are proposed to reduce the effects of nonlinearities like Pre-distortion [2], Post-distortion [3], Feedback [3] and Feed-forward [2] techniques. Among these, Cartesian feedback (CFB), which forms an alternative feedback technique, is an attractive option for two reasons: first it automatically compensates all process variations and secondly its linearization process is applied to all components in the loop. Nevertheless, historically the technique has suffered from practical shortcoming; it needs a phase corrector to compensate delay around the loop. In addition, the analog implementation of phase corrector is difficult to realize and highly area expensive. In this paper, authors propose a new solution to overcome this problem with a digital phase rotator approach. Due to the increasing demand of cost reduction, a Zero-Intermediate Frequency (Zero-IF) architecture avoiding the use of external filter has been chosen. Moreover, CFB with a Zero-IF architecture brings few additional components for an efficient linearity improvement. Full-analog CFB architecture has been studied and realized [3]. There are some drawbacks associated with this solution such as high area occupation and high power consumption. Delegating the phase rotation adjustment processing to a digital stage provide flexibility, higher integration and less area size than in full-analog architecture.

The paper is organized as follow. Section II presents Zero-IF transmitter with the CFB linearization loop and design consideration. Section III deals with implementation study of the digital stage where two solutions are presented and discussed. Section IV shows synthesis results such as occupied area and power consumption for ASIC target.

II. CARTESIAN FEEDBACK TRANSMITTER

A. Linearization Technique

Proposed linearization technique architecture based on a digital CFB implementation is shown in "Fig. 1". Quadrature baseband signals are directly up-converted to 1.95 GHz [1]. The RF signal is then amplified thanks to PA.

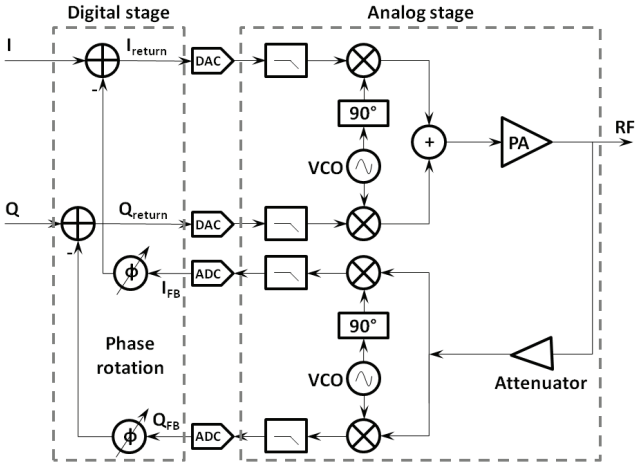

Figure 1. Zero-IF WCDMA transmitter with digital CFB loop

In the feedback path, the PA output is attenuated, down-converted to the baseband quadrature signals and filtered out. After the analog to digital convertor (ADC), a phase adjustment is applied to I_{FB} and Q_{FB} in order to cancel phase rotation around the loop. Feedback signals are subtracted from the input to provide return signals I_{return} and Q_{return}. These signals include the forward path non linearity. By loop effect, forward path non linearity is subtracted from input signals. Thus, input I/Q signals are pre-distorted to provide a linearized PA output. CFB transmitter is commonly implemented as a

fully analog circuit [3]. In such topology, subtraction operator and phase corrector have to be highly linear with low noise components. A digital implementation of subtraction and phase corrector relax linearity and in-band noise constraints than a full analog circuit. By having an optimized and high integrated digital stage, lower power consumption can be reached than analog configuration.

B. CFB Digital Stage and Design Consideration

Delay in the loop can lead to Error Vector Magnitude (EVM) degradation and instability [3]. The baseband loop filters in the feedback path lead to delay and symbol rotation when feedbacks signal and input signal are subtracted. Phase variations are cancelled by using the circular transformation given in (1), where θ is the phase correction value "Fig. 2".

$$\begin{bmatrix} I_c \\ Q_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} I_{FB} \\ Q_{FB} \end{bmatrix} \quad (1)$$

θ is calculated by comparing forward and feedback paths phases. Two architectures are evaluated for the circular transform implementation. The first architecture uses lookup table (LUT) and complex multiplier which is an expensive solution in terms of area occupation. The main advantage of this solution is to not introduce a large delay into the loop. The second architecture uses a Coordinate Rotation Digital Computer (CORDIC) algorithm [4] which requires less area than a complex multiplier when the data path exceeds 10 bits. Pipelined CORDIC introduce latency in the loop, a tradeoff between area occupation, latency and throughput is revealed, a fine tuning of the implementation variables will lead to optimal solution. Delay in the loop is limited by period of WCDMA data (T_{chip}) for stability consideration [3]. Digital stage operating frequency threshold is set to 242 MHz due to DAC and ADC characteristics "Fig. 1".

III. DIGITAL CFB IMPLEMENTATION

As already presented, the main task of the digital stage is to perform the vector rotation. Previously, the angle of rotation has to be estimated. This angle is the difference between the phase of the direct channel I/Q and the return channel I_{FB}/Q_{FB}. Therefore, the digital CFB architecture is organized using three blocks as shown in Fig. 2.

- phase estimation,
- vector rotation,
- subtraction.

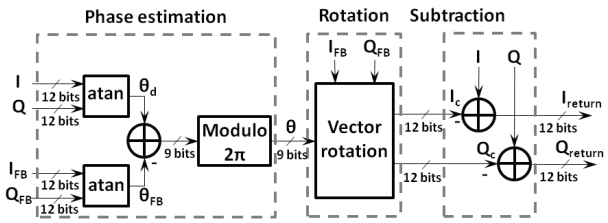

Figure 2. Digital stage architecture

A. Phase Estimation

Regarding phase estimation, it is very important to notice that phase subtraction must be done "modulo 2π" to keep the same range of variation of the angle applied to the next block (vector rotation). It implies that the phase estimation block is divided into two sub functional units: direct, feedback phase estimations (atan function) and modulo function.

1) "atan" function implementation

Different implementations of the digital atan function are proposed in the literature [5] and one of them, which is the most trivial, uses a look up table (LUT) [6]. This solution seems to be over-sized and very tasty in Silicon consumption in comparison with other alternatives such as the CORDIC algorithm. A comparative study regarding implementation of these two solutions is presented, as well as output performances.

a) LUT based architecture

LUT based solution, illustrated in Fig. 3, consists first making the division of "Q" to "I" and then going through an interpolation table (LUT) where all the values of the atan function are stored. LUT length is function of the phase estimation precision so "1" deg precision lead to 1440 bits ROM. Thanks to symmetry properties of atan function, size of the LUT can be limited to the half [7].

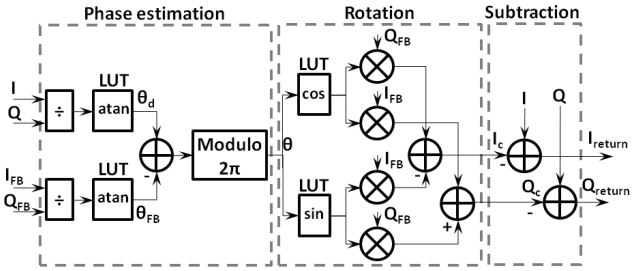

Figure 3. LUT based solution

To implement the division, multitude algorithm solutions can be considered. An algorithm called "Restoring Division Algorithm" [8] is used since it allows a very adequate operating frequency. This algorithm requires that the operands are positive and the numerator is greater than or equal to the denominator. Additional developments can process negative operands. Division by "0" results in saturation at the maximum value.

b) CORDIC based architecture

Another alternative for atan function implementation is to use an iterative algorithm called "CORDIC algorithm" [4]. CORDIC based solution doesn't require division as shown in Fig. 4. It takes as input the two coordinates of the vector and provides its phase [4]. This algorithm was designed to use adder and subtractor resources only as presented in Fig. 5. It was subsequently improved in order to calculate trigonometric functions (exp. cos, sin, atan ...) and this is done by configuring wisely its inputs variables.

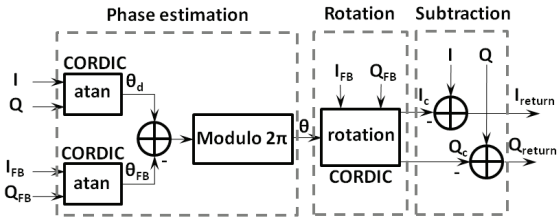

Figure 4. CORDIC based solution

Implementation of CORDIC algorithm can be done with several ways [9]. A tradeoff between throughput and design area is required by application as specified in section 2. The small computation complexity of the algorithm and its modularity gives considerable flexibility in the implementation phases and a full-pipelined architecture was adopted.

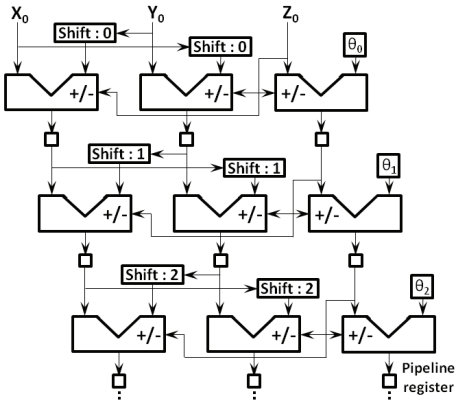

Figure 5. CORDIC example implementation

2) "Modulo" function implementation

Due to the extensive range of phase variation, the subtraction can overflow and so, it should be standardized to be adequate for the input of the next stage. It consists in calculating modulo 2π function. The idea is to calculate the remainder of the Euclidean division of the wanted angle by K*2π. A smart implementation of this function can be described by an algorithm organized as follows. First, a sign test is effectuated to benefit from the symmetry property of this function. Then the angle value is tested if it has exceeded a full circle turn. If so, 2π is subtracted from it and the test continues, else this value is retained as the output result.

B. Vector Rotation

1) LUT and multipliers solution

This first solution consists in following precisely the mathematical function of the rotation vector as it is described in equation (1). Fig. 3 shows an implementation example. Thanks to the phase cosine and sinus values, the complex multiplication can be done. To compute those coefficient; LUTs that contains the values of sine and cosine function can be used. An optimization step uses a single LUT (e.g. cosine) and trigonometric relationships to move from one function to another. A second optimization step exploits quarter wave symmetry.

2) CORDIC based solution

As shown in Fig. 4, the CORDIC algorithm can perform a vector rotation without multiplier resources allocation. A simple initialization on his entries, with the vector on which we rotate: namely I_{FB}/Q_{FB} and the angle to perform, is enough.

C. Subtraction

Subtraction is simple enough to be implemented in digital. Indeed, it is necessary to calculate the two's complement of the second operand and then use an adder.

IV. System Validation and Synthesis Results

A. Linearization Technique Validation

All building blocks making the digital stage have been designed in hardware descriptive language (HDL) with ModelSim® and have been characterized stand-alone. Now, we are able to realize system level simulations in order to validate the overall architecture, whyfor ADS Software have been used.

Fig. 6 and Fig. 7 depicts the output spectrum of the PA with and without CFB technique for a same output power [10]. This last exhibits clearly a decrease of the distortions on the adjacent channel due to CFB loop (Adjacent channel power ratio (ACPR) receives an improvement of 22dB at 5MHz from the carrier). In fact comparing with the mask define by the standards UMTS [1], the output spectrum for a Zero-IF architecture is out of specifications, in opposite with the output spectrum of the CFB loop.

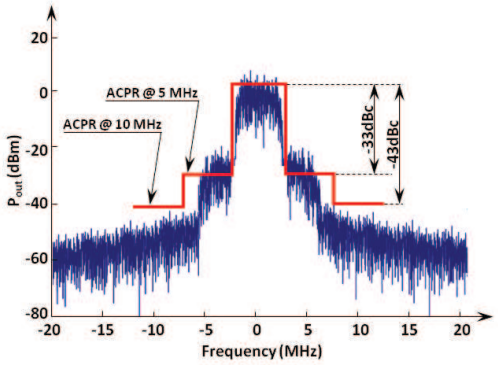

Figure 6. Output spectrum without CFB

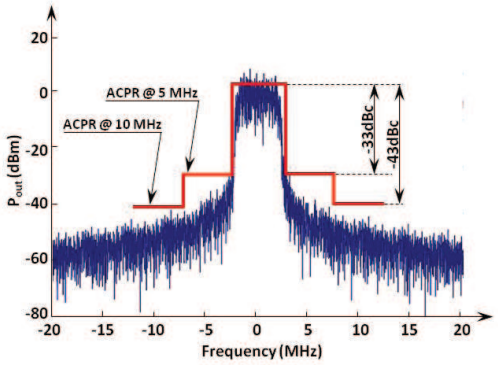

Figure 7. Output spectrum with CFB loop

B. *Implementation Results*

To validate this digital stage, we compared results obtained by floating simulation on Matlab® with those provided by HDL on ModelSim®.

Fig. 8 shows results of the phase alignment stage simulation. Note that the impact of the resolution (number of bits chosen) ensures convergence. The algorithm begins to track the desired value with acceptable accuracy after certain latency fixed by the number of internal registers. We also note that the algorithm oscillates around the solution when the values are close to "0".

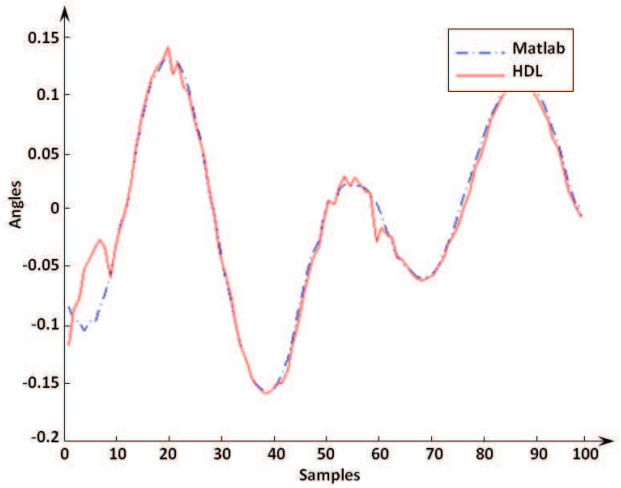

Figure 8. Outputs stage simulation

To respect the real-time constraint, the point on which we will act is none other than the throughput of the synthesized circuit, so it is imposed as 242 MHz.

Table 1 summarizes ASIC synthesis results on 65nm technology (CORE65LPLVT1.00V) in terms of area occupation and energy consumption for our two considered solutions (CORDIC and LUT). Two power types are presented: the dynamic power which depends on throughput and the leakage power whose consumption is constant.

TABLE I. ASIC SYNTHESIS RESULTS

		CORDIC	LUT
Phase estimation	***Occupation***	6656 µm^2	4480 µm^2
	Dynamic Power	1.01 mW	0.46 mW
	Leakage power	2.95 µW	2.09 µW
Rotation	***Occupation***	9477 µm^2	14935 µm^2
	Dynamic Power	1.4 mW	1.19 mW
	Leakage power	4.17 µW	5.72 µW
Subtraction	***Occupation***	613.6 µm^2	
	Dynamic Power	0.098 mW	
	Leakage power	0.277 µW	
Whole solution	***Occupation***	23402 µm^2	24461 µm^2
	Dynamic Power	3.77 mW	2.94 mW
	Leakage power	10.35 µW	10.24 µW

LUT based solution consumes less energy in comparison with the CORDIC one with almost likely surface occupation; therefore it is more adequate for our application. Nevertheless, hybrid architecture could be considered by combining the LUT solution for the phase estimation bloc and the CORDIC one for the vector rotation bloc. It is important to notify that the proposed solution tree time less energy than the full-analog one; 2.94 mW for our solution compared to 8.8 mW in the case of full-analog architecture [3].

V. CONCLUSION

The problem of phase alignment has stood as the primary barrier to the widespread use of the Cartesian feedback technique. In this paper a Cartesian feedback direct conversion transmitter with digital processing has been presented and evaluated for a Zero-IF WCDMA transmitter. This mixed-signal architecture allows the linearity constraints on the subtractor, on the phase corrector and also on the DACs to be relaxed.

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