A Real-Time Predictive-Maintenance System of Aluminum Electrolytic Capacitors Used in Uninterrupted Power Supplies

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***Abstract*—This paper presents a low-cost method to realize a real-time condition monitoring and a predictive-maintenance system of an electrolytic capacitor used in uninterruptible power supplies (UPSs). This method consists in detecting the changes in real time of the equivalent series resistance and the capacitance C values of the electrolytic capacitors. Simulation and experimental results are presented to illustrate the proposed monitoring technique. The proposed method can be used in UPS where waveforms are continuously varying in amplitude, frequency, and temperature. The proposed online failure prediction method has the merits of using only the existent resources in UPS and with the use of known algorithms.**

***Index Terms*—Electrolytic capacitors, identification, Kalman filtering, predictive maintenance, real time.**

I. Introduction

ELECTROLYTIC capacitors have been widely used in power-electronic systems because they can achieve high capacitance and voltage ratings with volumetric efficiency and low cost. This type of capacitors has been traditionally used for filtering, coupling, timing networks, bypass, and many other applications in power electronics requiring a cost-effective and volumetrically efficient component. It is known that the common faults in electrolytic capacitor include initial catastrophic failures due to manufacturing or misapplication defect and wear-out faults, which cannot be avoided. Unfortunately, electrolytic capacitors are one of the weakest components in power-electronic converter [1]–[13]. For example [1], [4], in uninterruptible power supplies (UPSs), they are responsible for about 50% of the cases of power-electronic component failures. An electrolytic capacitor has a number of root causes and failure modes. Degradation of this component is due to a combined effect of electrical, thermal, mechanical, and environmental stresses. The main wear-out failure mechanism is the evaporation of the electrolyte solution which is accelerated with temperature rise during the operation and due to ripple currents. This causes a decrease in C and an increase of the equivalent series resistance (ESR) which further increase the temperature (losses). Standard [2] suggests that the capacitor should be considered as failed if there is an increase that is double the initial ESR value and a 20% decrease in the capacitance value. Hence, estimation of ESR and the capacitance by taking into account the temperature is important for condition monitoring of the electrolytic capacitor. The purpose of this paper is to propose a method to detect in real time the changes in the value of the ESR and also of the capacitance in order to create a real-time predictive system of electrolytic-capacitor failures. It is further shown in this paper that the proposed method can be applied even in the nonstationary system, such as UPS, where capacitor ripple voltage and current are continuously varying in amplitude and frequency. They also depend on the ambient temperature where the converter operates.

Many papers have proposed different methods or algorithms to determine the ESR and/or capacitance C of the electrolytic capacitor [2]–[13]. However, many parameters, such as offline additional measurements, and many computations are required, which makes it complicated, difficult, expensive, and impractical for actual application.

Modern UPS can utilize a variety of accurate sensors, numerical treatment systems, and powerful computation resources which are used to control and regulate the UPS in order to improve its performance and efficiency. The suggested method has the merits of making a real-time predictive-maintenance system of electrolytic capacitors by using existing resources in the UPS. This predictive-maintenance system works in background tasks and without disturbing the regulation and the operating system.

II. Electrolytic-Capacitor Technology

A. Electrolytic-Capacitor Modeling

The structure of a screw-terminal electrolytic capacitor [16] is shown in Fig. 1.

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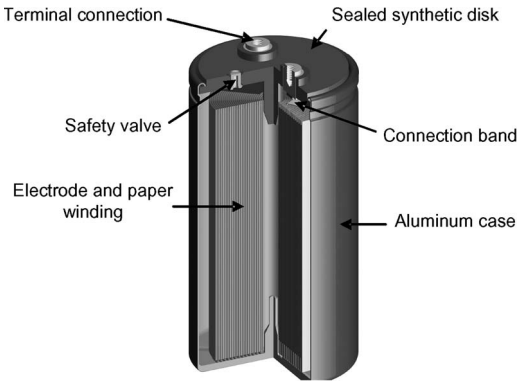

Fig. 1. Structure of a screw-terminal electrolytic capacitor [16].

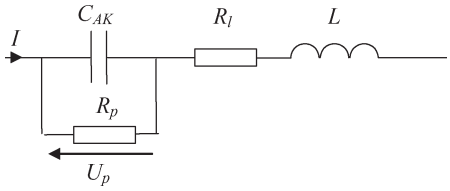

Fig. 2. Electrical equivalent circuit of an electrolytic capacitor.

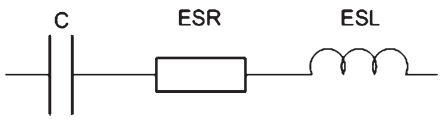

Fig. 3. Normalized electrical equivalent circuit of an electrolytic capacitor.

Due to physical design elements and construction, aluminum electrolytic capacitors are modeled by the electrical equivalent circuit [14], [17] shown in Fig. 2. This model, which is the most used one, is rather simple and gives a good frequency response.

In Fig. 2, C_{AK} is the ideal capacitance between anode and cathode, R_p is the parallel resistance which represents all the losses in the dielectric and the leakage between the two electrodes, R_l is the connection and electrode serial resistance, and L is connection and winding equivalent series inductance (ESL). This circuit can be simplified with the normalized representation given in Fig. 3. It is a series combination of an ESR which represents all the component losses, a capacitance C, and an ESL, which is due to the wound structure of the capacitor.

From the impedance equality between the circuit elements shown in Fig. 2 and those represented in Fig. 3, we can conclude the following equations, where ω is the electrical pulsation:

$$C = C_{AK} \cdot \left(1 + \frac{1}{R_p^2 C_{AK}^2 \omega^2}\right) \tag{1}$$

$$ESR = R_l + \frac{R_p}{1 + R_p^2 C_{AK}^2 \omega^2} \tag{2}$$

$$ESL = L. \tag{3}$$

This capacitor representation is important because it is directly given from the impedance frequency measurements. Therefore, the resonant frequency f_r of the capacitor is given by

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{ESL \cdot C}}. \tag{4}$$

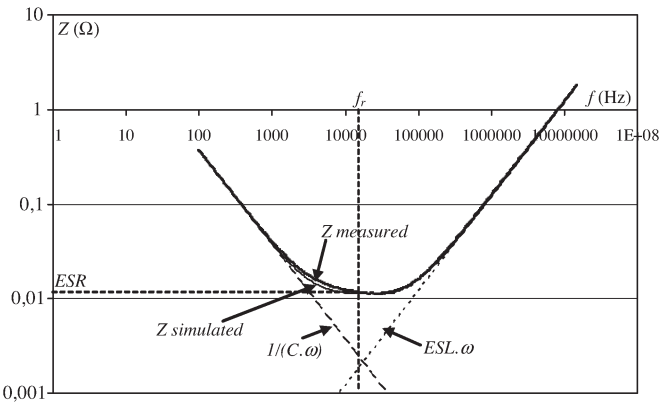

Fig. 4. $Z(f)$ for aluminum electrolytic capacitor of 4700 μF/500 V.

In addition, this simplified equivalent circuit can give a first approximation of the capacitor behavior without taking into account parameter variations of C, ESR, and ESL versus frequency. This theory can be demonstrated by the figure shown in Fig. 4, which represents the module Z of the complex impedance $\underline{Z}$ versus frequency, of an aluminum electrolytic capacitor of 4700 μF/500 V. As can be observed from the bode plot, there exist three widely separated frequency bands. The capacitance of the capacitor is dominant in low-frequency band. ESL is dominant in high-frequency band, and ESR is dominant in the midfrequency one.

Equations (1) and (2) show that ESR and C can be considered separately from the frequency when the latter is not too low. Therefore, the resistance R_p has an effect only on very low frequencies (less than several tens of hertz). This is shown in Fig. 5, which represents the effect of R_p versus frequency f on the ESR and C parameters. It is an example of an electrolytic capacitor with a nominal capacitance value of 4700 μF and a nominal ESR of 20 mΩ.

B. Electrolytic-Capacitor Aging

Fig. 6 [17] shows the majority of electrolytic-capacitor failure modes and their root causes. As can be seen, the estimation of ESR and C can provide at least all the normal and use-failure defects. Therefore, the estimation of these two parameters is important to realize a real-time predictive-maintenance system of electrolytic capacitor.

III. Electrolytic-Capacitor Monitoring

A. Estimation of ESR and C

As we have just seen before, the electrolytic capacitors can be modeled as a serial combination of a capacitance, an ESL, and an ESR, as shown in Fig. 3. The bode plot of an electrolytic capacitor with $ESR = 74$ mΩ, $ESL = 10$ nH, and capacitance $C = 470$ μF is shown in Fig. 7. Therefore, the converters in the UPS works at a low-frequency band compared with the resonant-frequency one (4), so ESL is usually neglected, and the equivalent model of the capacitor is given by an ESR in series with a capacitance (C).

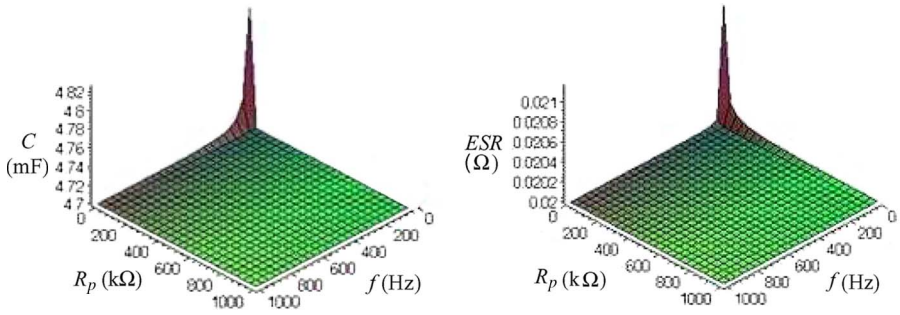

Fig. 5. $Z(f)$ for aluminum electrolytic capacitor of 4700 μF/500 V [17].

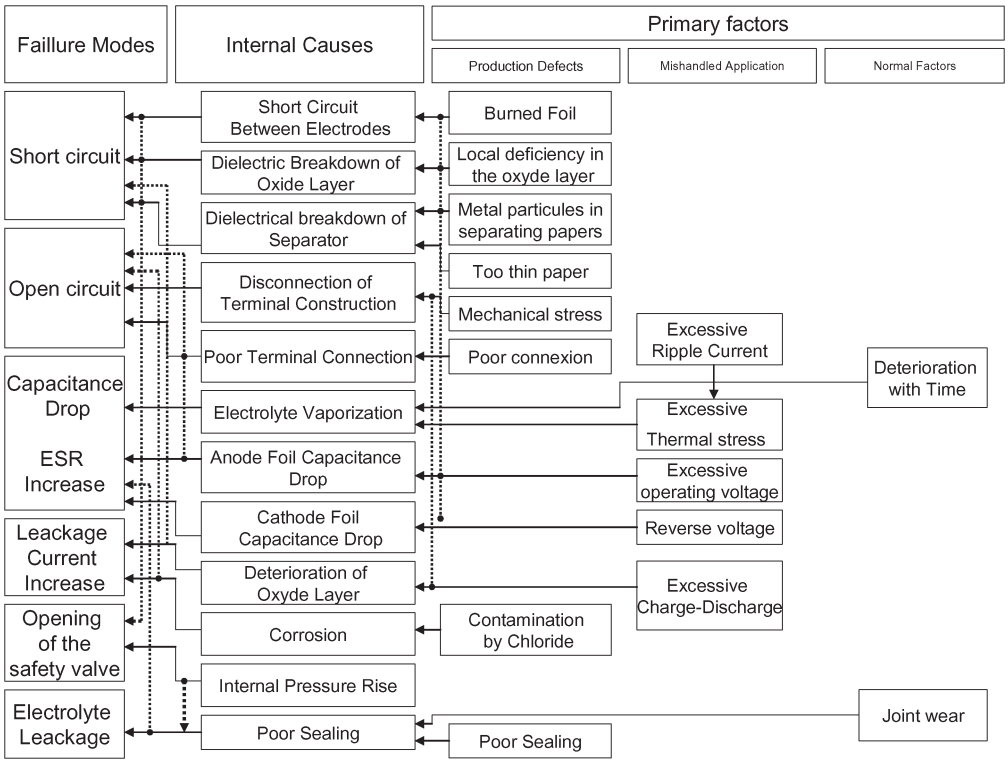

Fig. 6. Capacitor failures and their causes [17].

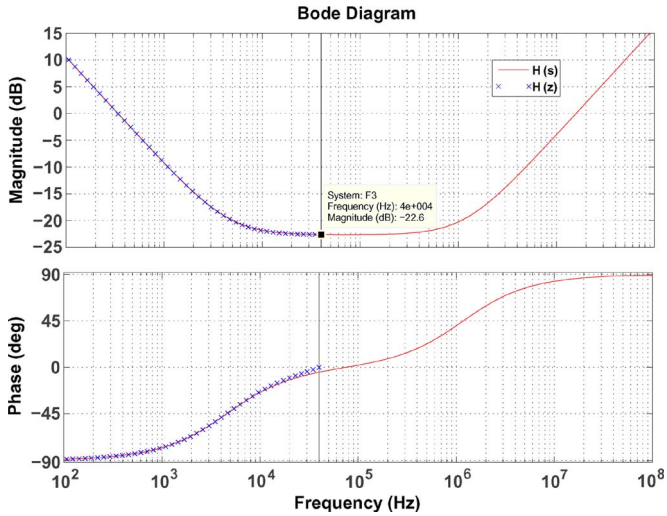

Fig. 7. Bode diagram of an electrolytic capacitor in continuous- and discrete-time domain.

The transfer function of this model is given by

$$H(s) = \frac{Uc(s)}{Ic(s)} = \frac{ESR \cdot C \cdot s + 1}{C \cdot s}. \tag{5}$$

However, converters are controlled by using digital treatments. We can consider the z-transform corresponding to (5) to represent the discrete-time domain by using the bilinear method of Tustin and which is given by (6), where Ts is the sampling period

$$\begin{aligned} H(z^{-1}) &= \frac{b_0 + b_1.z^{-1}}{1 - z^{-1}} \\ &= \frac{\left(ESR + \frac{Ts}{2.C}\right) + \left(\frac{Ts}{2.C} - ESR\right).z^{-1}}{1 - z^{-1}}. \end{aligned} \tag{6}$$

The bode plot in Fig. 7 shows that the continuous- and discrete-time domain for a sampling period of $Ts = 12.5$ μs are equivalent if we use the bilinear-method discrete time.

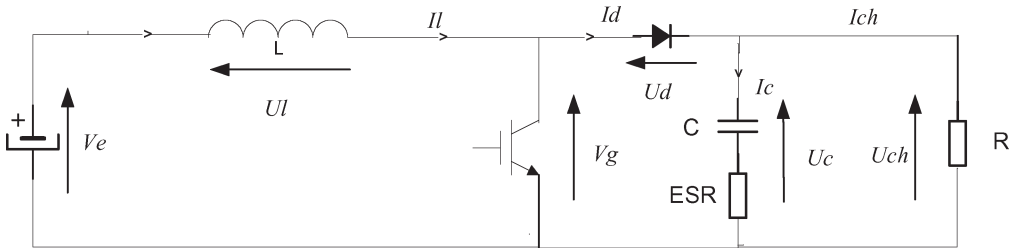

Fig. 8. Schematic of a boost-converter circuit with a dc capacitor circuit.

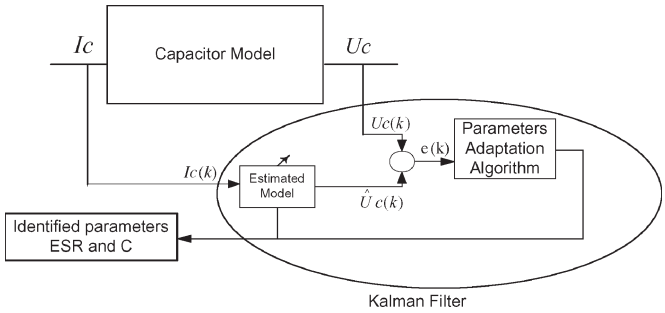

Fig. 9. Parameter identification using Kalman filter.

To identify b_0 and b_1 for the two parameters ESR and C, we use different forms of Kalman filter.

A Matlab simulation was performed using dynamic equation from the equivalent circuit shown in Fig. 8 of a boost-converter with a 50-V dc voltage input, with a switching frequency of 5 kHz and which is regulated to have a 200-V dc voltage output.

A recursive least square algorithm, which is a particular case of Kalman filter, was used as shown in Fig. 9.

In practice, we do not have a capacitor current sensor because it is difficult and expansive to implement in UPS. To perform and regulate the output voltage, we only dispose of one current sensor used to have the input current inductance L of the boost converter. However, we can identify the capacitor current using Kirchhoff's laws referring to the schematic of the boost converter shown in Fig. 8

$$Ic = Id - Ich. \tag{7}$$

When the insulated-gate bipolar transistor is off (the pulsewidth modular PWM $= 0$), we have $Id = Il$, so we can conclude the following:

$$Id = Il * \overline{PWM}. \tag{8}$$

In stationary process, the average capacitor current Ic is equal to zero, so, for one regulation period, we have the following:

$$Ic = Il * \overline{PWM} - \text{avg}(Il * \overline{PWM}). \tag{9}$$

Respectively, the simulation results of the capacitor ripple voltage and capacitor current identified with the use of (9) are shown in Fig. 10.

The simulation results presented in this section are summarized in Table I.

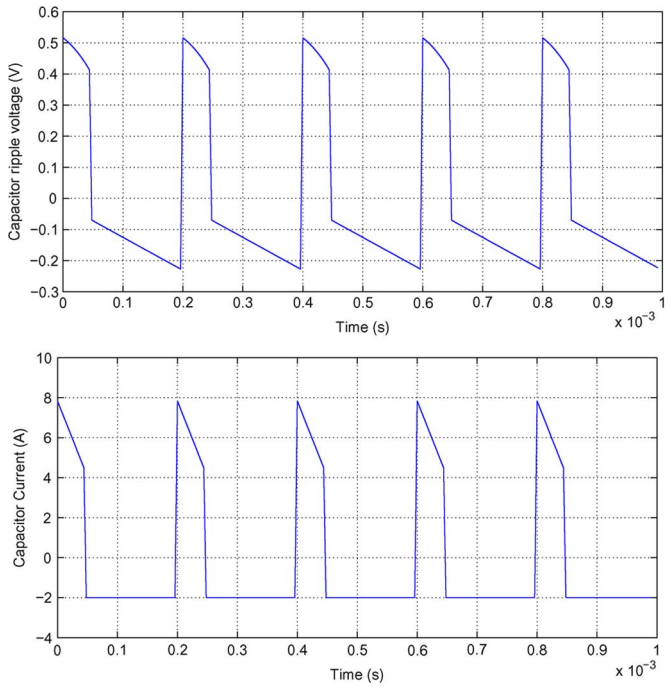

Fig. 10. Matlab simulation results of capacitor ripple voltage ΔUc and capacitor current Ic.

TABLE I
SIMULATION RESULTS FOR ESTIMATED PARAMETERS

ESR_{fixed}	$\text{ESR}_{estimated}$	% error
74 $m\Omega$	74.2 $m\Omega$	2.2
C_{actual}	$\text{C}_{estimated}$	% error
470 μF	466 μF	2.7

B. Aging Algorithm

The aging algorithm, which takes into account the temperature, is given in the following.

The evolution of ESR and C versus ambient temperature T_a is given by the following equation [14] where α, β, γ, χ, ν, and λ are experimental parameters and depend on the used capacitor:

$$ESR(T_a, t) = \alpha + \beta \cdot \exp\left(-\frac{T}{\gamma}\right) \tag{10}$$

$$C(T_a, t) = \chi + \lambda \cdot \exp\left(-\frac{T}{\nu}\right). \tag{11}$$

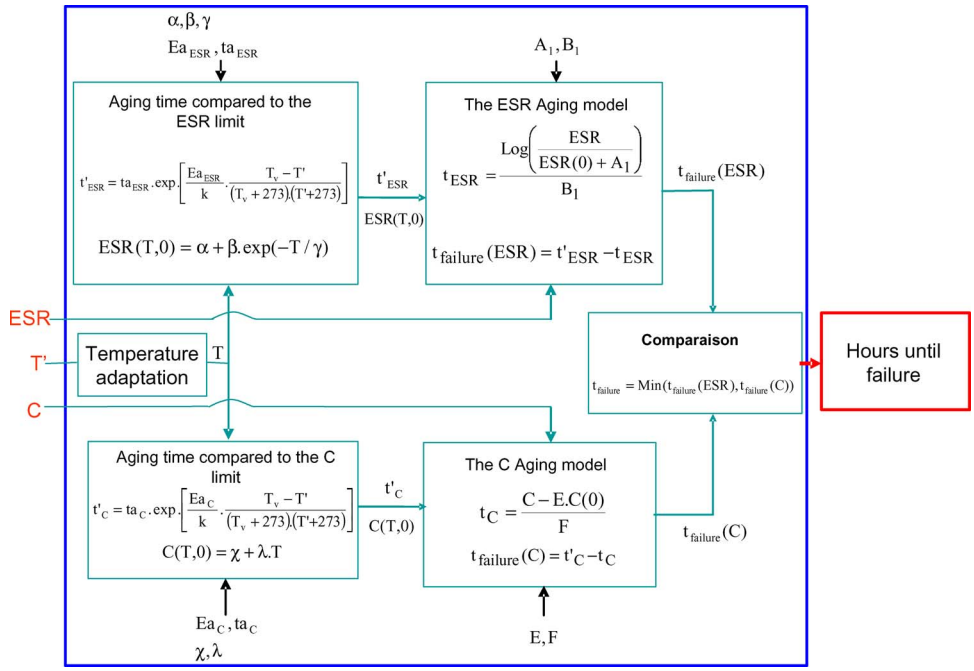

Fig. 11. Aging algorithm.

The time until failure compared with failure limits of ESR and C can be calculated by using the following [14]:

$$\frac{t'_{ESR}}{ta_{ESR}} = \exp\left[\frac{Ea_{ESR}}{k} \cdot \frac{T' - T_a}{(T'+273)\cdot(T_a+273)}\right] \quad (12)$$

$$\frac{t'_{C}}{ta_{C}} = \exp\left[\frac{Ea_{C}}{k} \cdot \frac{T' - T_a}{(T'+273)\cdot(T_a+273)}\right] \quad (13)$$

$$ESR(t_{ESR}) = (ESR(0) + A_1)\cdot\exp(B_1 \cdot t_{ESR}) \quad (14)$$

$$C(t_C) = E \cdot C(0) + F \cdot t_C \quad (15)$$

where

T_a	Ambient temperature (25 °C for example).
T'	Aging temperature (85 °C for example).
ta_{ESR}	Aging time for the ESR limit at T_a.
ta_C	Aging time for the C limit at T_a.
t'_{ESR}	Lifetime limit at T' with ESR aging indicator.
t'_C	Lifetime limit at T' with C aging indicator.
t_{ESR}	Time until failure with ESR aging indicator.
t_C	Time until failure with C aging indicator.
k	Boltzmann constant (8.617 times 10^{-5} eV/°K).
Ea_{ESR}	Activation energy with ESR aging indicator.
Ea_C	Activation energy with C aging indicator.

A_1, B_1, E, and F are experimental parameters and also depend on the used capacitor.

From (10)–(13), the time until failure of the capacitor is given by the lower computed time between ESR lifetime limit and C lifetime limit, as shown in Fig. 11.

We have, for these works, different types of capacitors from four different manufacturers.

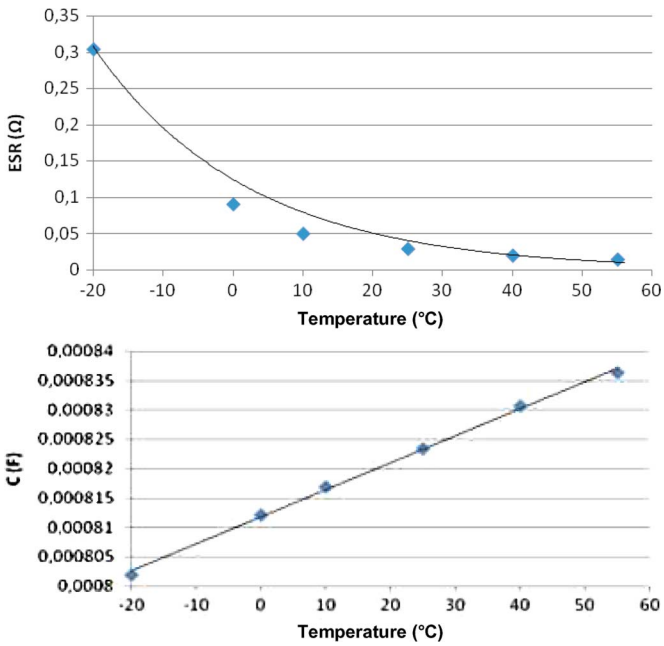

Fig. 12. Electric parameter variations versus temperature of one capacitor (1000 μF/450 V).

All capacitors are first characterized versus temperature to determine the parameter-evolution laws versus temperature.

The parameters of (10) are determined by the nonlinear least square method of Levenberg–Marquardt which allows a very close approximation of the model.

For the example shown in Fig. 12, the method gives the following values for ESR:

$$\alpha = 0.013055\ \Omega \quad \beta = 0.75844\ \Omega\ \gamma = 14.888386\ ^\circ\text{C}.$$

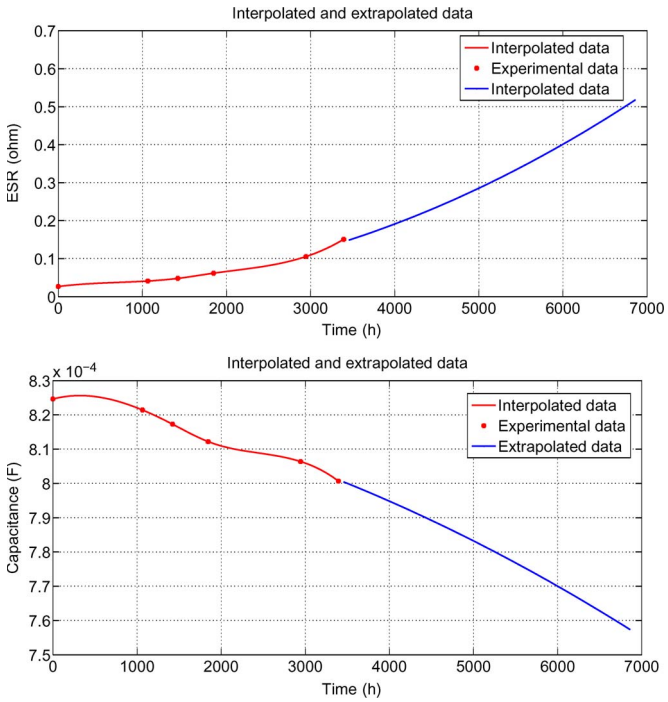

Fig. 13. ESR evolution at 5 kHz and C evolution at 200 Hz for one capacitor (1000 μF/450 V).

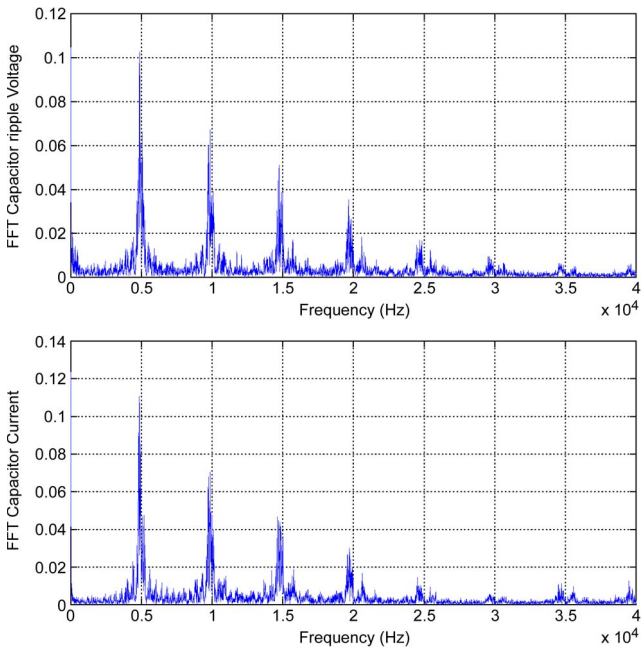

Fig. 14. FFT analysis of capacitor ripple voltage and capacitor voltage for a sampling frequency $f_s = 80$ kHz.

The parameters of (11) are determined in the same way as those identified in ESR. For the example shown in Fig. 12, we have the following values for C:

$$\chi = 0.000812 \text{ F} \quad \lambda = 4.600790 \text{ times } 10^{-0.007} \text{ F/°C}.$$

Some experimental results show the parameter evolutions of ESR and C after 3390 h of aging (about 5 mo) at 90 °C. Also, we use a Matlab algorithm to make a linear interpolation and extrapolation with the use of experimental data. This allows us to find the parameter-evolution laws and also the time until failure corresponding to the ESR and the capacitance C limit. The ESR and C variations versus temperature for a capacitor of 1000 μF/450 V are shown in Fig. 12.

We show in Fig. 13 the interpolated and extrapolated data with the use of experimental measurements for ESR and C parameters of one capacitor (1000 μF/450 V).

C. Experimental Study

1) Experimental Setup: To verify the validity of the proposed method, an experimental study was performed on a boost converter with a 50-V dc input, 470-μF–450-V capacitor, an R load of 100 Ω, and a switching frequency that is fixed at 5 kHz. Therefore, a fixed-point DSP controller (TMS320F2812) was used for Il, Uc, Ic, and capacitor ripple voltage ΔUc acquisition measurements and switching operations required to perform the 200-V dc output voltage. To do that, we choose the two imbricated-loop principles, one fast current loop with a proportional/integrator controller to perform the current reference and another external voltage loop with a deadbeat controller to perform the 200-V dc output voltage. Moreover, a recursive least square algorithm (a particular case of Kalman filter) has been implemented to identify the two parameters ESR and C.

In literature [15], we know that using different cases of Kalman filter provides cutoff of the dc component of the input and output measurements, which are, respectively, capacitor current (recovered using the inductance current) and capacitor voltage. Therefore, the capacitor voltage and the inductance current are passed through a high-pass filter with cutoff frequency of around $f_c = 200$ Hz to suppress the dc component of the voltage measurements and without including phase shift. Consequently, we have only the capacitor ripple voltage which is in phase with the capacitor current.

A fast Fourier transform (FFT) analysis respectively on the capacitor ripple voltage and capacitor current is shown in Fig. 14, and we see that the bandwidth of the system is about 40 kHz. Therefore, with respect to the Shannon theorem and to have a good ESR and C estimation, we choose a sampling frequency $f_s = 80$ kHz.

To eliminate signal distortion, an antialiasing filter [15] with a cutoff frequency $f_c = (f_s/2) \approx 40$ kHz is used, as shown in the global capacitor condition monitoring scheme Fig. 15.

2) Adjusting Channels: The amplitudes of the measurements used to identify ESR and C are variable, depending on several parameters of the system in real time such as temperature, input voltage, and load applied to the power converter. To always have a full scale (3 V) on the DSP entrance for a good accuracy of identified parameters, we choose to apply a system to adjust automatically the amplitude of each measurement channel needed for identification. This system was performed by using a single eight-channel demultiplexer (M74HC4051) for each measure. Each demultiplexer was controlled independently by DSP to implement a variable gain. The gain choice is given by a well-defined algorithm shown in Fig. 16.

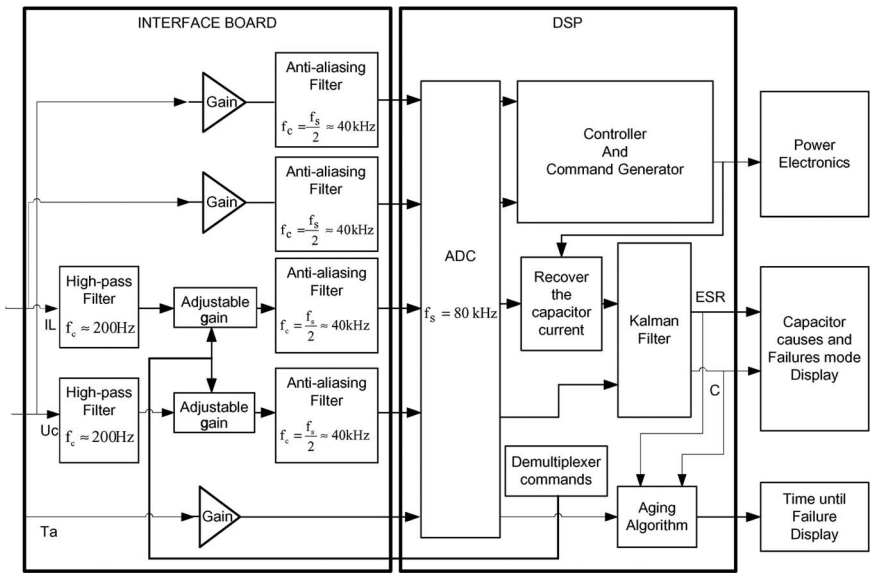

Fig. 15. Real-time electrolyte capacitor condition monitoring in UPS.

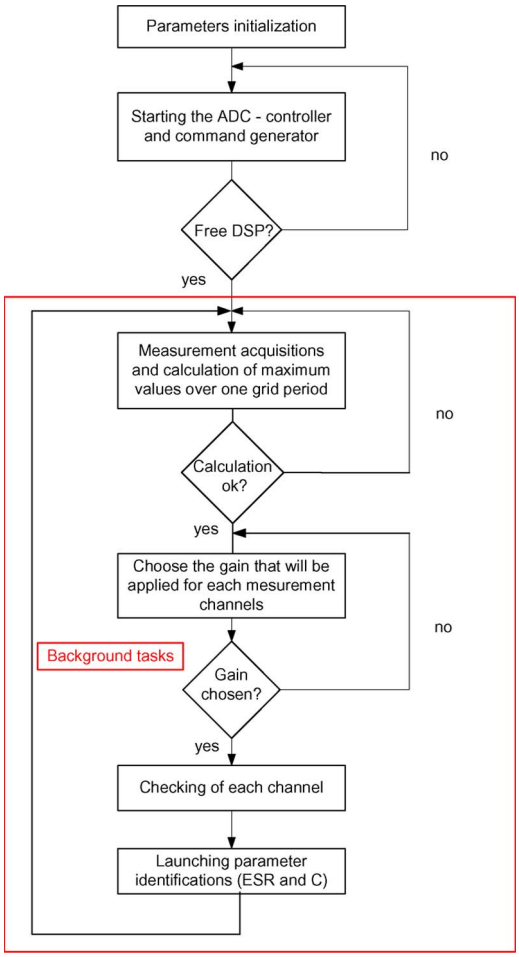

Fig. 16. Online gain choice algorithm.

This algorithm runs in real time and with less priority compared with the system regulation. The coding used to select the variable gain is optimized with minimizing loops (for, if, while, . . .) to have few DSP clock cycles used.

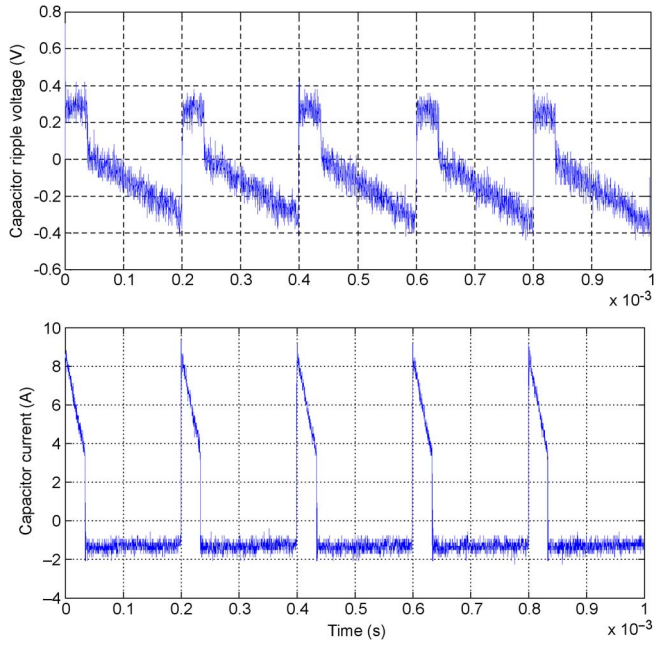

Fig. 17. Capacitor ripple voltage and capacitor current.

3) Experimental Results: The experimental measurements on the scope of capacitor ripple voltage and capacitor current (given by a current probe) are shown in Fig. 17.

The corresponding numerical DSP measurements (after the analog-to-digital converter) of the capacitor ripple voltage and recovered capacitor current (9) are shown in Fig. 18.

The experimental results for the estimated parameters are summarized in Table II.

The least-squares algorithm implemented on DSP uses about 1 kB of a 16 bits word of DSP memory and takes about 2 s to converge and gives the ESR and C estimated values. This time is too small compared with the lifetime of a capacitor. Also, from experiments, a good and fast parameter identification is given by a decreasing forgetting factor. At every turn, the

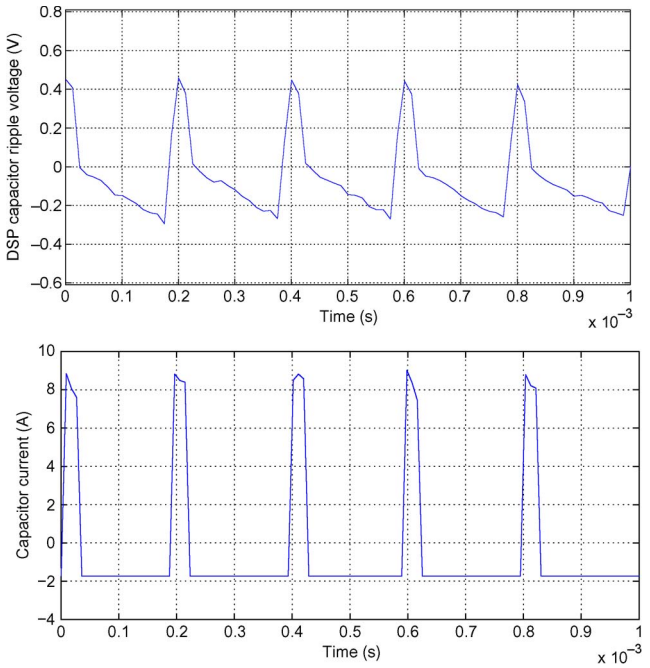

Fig. 18. Capacitor ripple voltage and capacitor current recovered on DSP with a sampling frequency $f_s = 80$ kHz.

TABLE II
EXPERIMENTAL RESULTS FOR ESTIMATED PARAMETERS

ESR_{actual}	$\mathrm{ESR}_{identified}$= [$\mathrm{ESR}_{min}$;$\mathrm{ESR}_{max}$]	% error
75.1 mΩ	[71.3 mΩ,78.8 mΩ]	$+/-5$
C_{actual}	$\mathrm{C}_{identified}$=[C_{min};C_{max}]	% error
472 μF	[466 μF, 518 μF]	$+/-10$

algorithm starts with the last identified parameters of ESR and C.

It can be clearly seen that there is a nonsignificant error between the estimated and actual values of ESR and C.

These results are consistent with the measured value using an impedance meter.

IV. CONCLUSION

Due to their large capacity and low cost, electrolytic capacitors, with the abilities of energy storage and voltage regulation, are used for almost all types of power-electronic system. Electrolytic capacitors, which are usually affected by wear-out faults, play a very important role for the quality and reliability of power-electronic system. Therefore, it is important to monitor the condition of an electrolytic capacitor in real time to predict the failure. A new method has been proposed to detect in real time the changes in the ESR and capacitance C values by taking into account the ambient temperature in order to create a real-time failure prediction of an electrolytic capacitor. For the proposed method, capacitor-current and capacitor ripple-voltage measurements using cheap and simple analog circuits are required. Simulation results and hardware experiments show that the proposed electrolytic-capacitor failure-prediction technique can be applied to a power-electronic system successfully.

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