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# On the Susceptibility of Micro-controller to Radio Frequency Interference

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*Abstract* – Electromagnetic compatibility (EMC) has recently focused more attention on Integrated Circuits (ICs). This work deals with immunity of micro-controllers to Radio Frequency Interference (RFI). The susceptibility test methods are reviewed, the test bench setup in our labs is presented, and some aspects of defensive software are detailed.

## I. INTRODUCTION

Susceptibility to radio frequency interference is becoming a major concern for integrated circuits (IC) [1], with the multiplication of powerful parasitic sources such as mobile phones, high speed networks and wireless systems (Fig. 1). As the operating clock frequency increase and the supply voltages become lower, the susceptibility of ICs is increased.

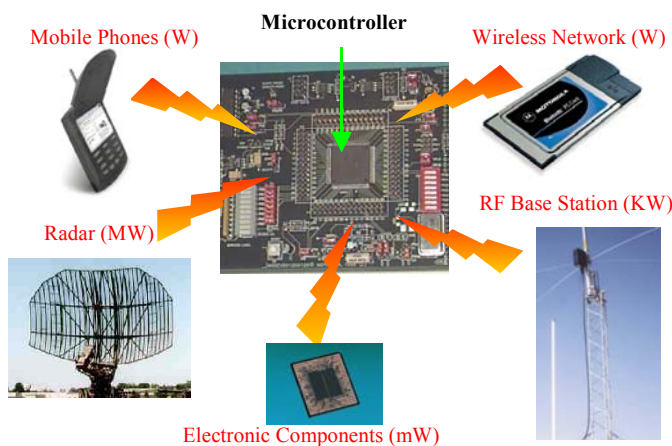


Fig. 1 The main powerful parasitic sources of RFI which could affect IC's immunity.

This work mainly deals with micro-controllers. These kinds of devices manage various signals such as analogue signal, digital signal, communication protocol (I<sup>2</sup>C, CAN, Ethernet...), external RAM memory bus or external interrupt signal, which are potential paths to introduce RFI into integrated circuits (Fig. 2).

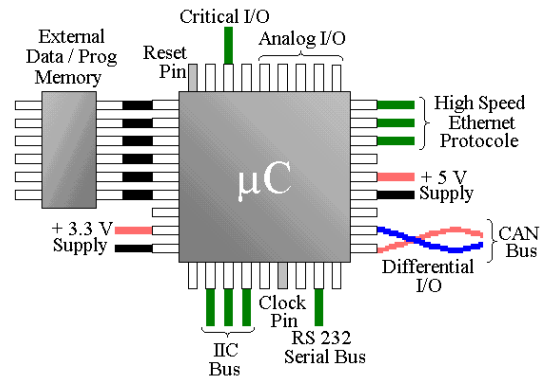


Fig. 2 Potential paths for RFI coupling into micro-controllers.

## II. IMMUNITY MEASUREMENT METHODS

The susceptibility standards are at IEC under reference IEC 62132 [2]. The parameters, the general setup and the conditions three test methods are described in these standards:

- The workbench Faraday cage (WBFC) [3] is a method for measuring the IC susceptibility level in common mode. The test setup is based on a shield box inside which the integrated circuit under test is placed. The measurement test setup operates within the frequency range 150 kHz to 1 GHz.
- The bulk current injection (BCI) method [5] allows to measure the IC susceptibility level with inductive coupling on wires connected directly to the integrated circuit. The measurement is valid within the frequency range 15KHz to 400 MHz. The method consists in injecting a current using a magnetic probe on the input or output of the integrated circuit.
- The direct power injection (DPI) method [6] allows to measure the IC susceptibility level with capacitance coupling directly on the integrated circuit within the frequency band 10 kHz to 1GHz.

### III. TESTING THE DEFENSES

This research work on susceptibility analysis of micro-controllers uses the DPI standard [6]. The test-bench used at LESIA is presented in Fig. 3. The RFI wave is amplified and superimposed to functional signals, via a coupling capacitance.

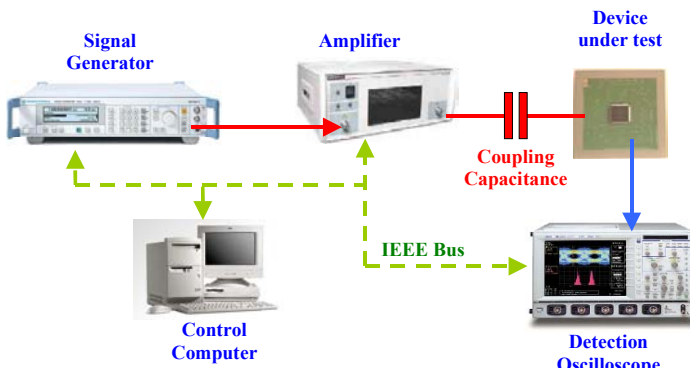


Fig. 3 Test bench used to perform the measurement of integrated circuits immunity.

A specific printed circuit board (PCB) has been developed for immunity tests. On one side of the PCB, the micro-controller under test is implemented. On the other side, peripheral components are placed, as well as supply connectors, disturbance injectors and measurement probes.

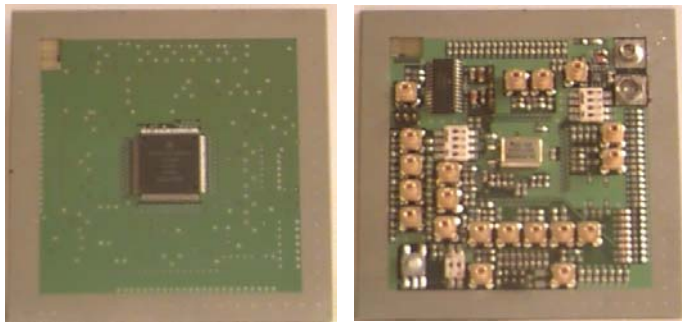


Fig. 4 Printed circuit board developed to perform the measure of IC's immunity.

A first approach is to force the micro-controller to transmit a periodical pulse to prove that it is normally working. An other criterion consists in measuring the supply current without RFI source, and to establish a template form based on this reference measure. In the presence of RFI source, the device is considered out of working when a current over-consumption is detected on supply paths.

Several results have been obtained showing a significant dependence of the ICs to frequency, in accordance to most experimental results on this subject. The experimental analysis reported in figure 5 concerns a RFI range from 1MHz to 1GHz. It clearly demonstrates that the IC fails when a 80MHz wave is injected to the IC, but is almost insensitive to 20MHz or 900MHz input waves.

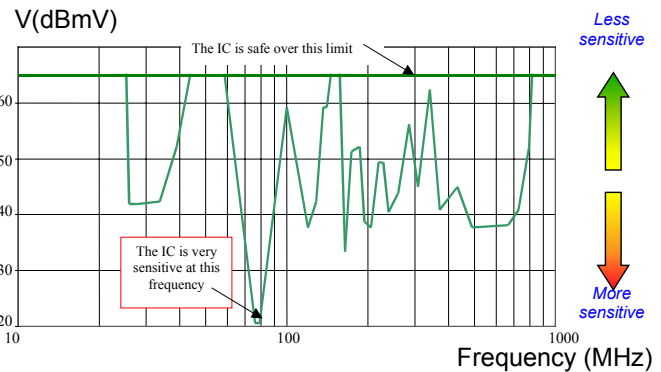


Fig. 5 Immunity versus frequency

To protect integrated circuits from RFI, some hardware techniques exist such as Schmidt trigger, clamp junctions, etc. These hardware solutions reduce IC's susceptibility in particular cases, but they are not adequate to detect the RFI source and consequently invalidate error data acquisition.

Some intermediate techniques between hardware and software solutions exist such as internal watchdog, power on reset, error encoding and checking, redundancy [7] [8]. These techniques allow to properly reset a micro-controller when the embedded software lost handshake, or when power supply is not stable enough.

Complementary software solutions have been presented by [7] and [8] to improve immunity of application using defensive software. For example it is recommended to fill empty program memory with known instructions, such as NOP (no operation) and jump to reset address, to protect application from involuntary loose of program counter.

### IV. MODELLING

Although a EMC model exists for the prediction of IC emission (ICEM) [9], the modelling of susceptibility has not reached a sufficient maturity either from a research and a standardisation point of view. The next goal of our work is to reuse the ICEM model for susceptibility prediction.

### REFERENCES

- [1] E. Sicard, C. Marot, J.Y. Fourniols, M. Ramdani, "Electromagnetic Compatibility for Integrated Circuits", URSI Review of Radio Sciences 1998-2000, 2002, IEEE press.
- [2] International Electro-technical Commission [1999] "IEC 62132: Integrated Circuits, Measurements of Susceptibility", IEC standard. www.iec.ch
- [3] IEC 62132 part 3, 47A/529NP, "Measurement of electromagnetic immunity of integrated circuits in the range of 150kHz to 1GHz"
- [4] F. Fiori "Integrated circuits immunity evaluation by different test procedures", Proceedings of the International Symposium on Electromagnetic Compatibility EMC'2000 Brugges, pp. 286-289, 2000.
- [5] IEC 62132 part 4 issued from group 47A/526/NP, "Integrated circuits, immunity test to narrow-band disturbances by Bulk Current Injection (BCI), 10KHz-400MHz"
- [6] IEC 62132 part 2, 47A/529/NP, "Direct RF power injection to measurement method"
- [7] D.R. Coulson, "EMC Techniques for Microprocessor Software", IEE Colloquium on EMC for Small Business 1998, N°1998/420.
- [8] T. Williams, "EMC for product designer", 2<sup>nd</sup> Edition, Publitrone / Elektor, ISBN: 2-86661-106-3, Chapter 6, pp.216-224, March 1999.
- [9] IEC 62014-3 "EMC for components - Part 3: Integrated Circuit Electrical Model"