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Single die multiple 600V power diodes with vertical voltage terminations and isolation

K. Vladimirova, J.-C. Crébier, Y. Avenas, C. Schaeffer, T. Simonot

Grenoble Electrical Engineering Lab (G2Elab)
961 Houille Blanche Street, 38402 St Martin d'Hères, France
e-mails: vladimirova@g2elab.grenoble-inp.fr, crebier@g2elab.grenoble-inp.fr

Abstract – Integrating multiple power devices in the same die makes their implementation more simple and reliable. In this paper, a new concept for low cost and high efficiency monolithic integration of 600V vertical power diodes is proposed and experimentally validated. The concept relies on the creation of vertical voltage terminations on the periphery of the devices, thus allowing to terminate and to isolate each one of the integrated power devices. Simulation results show that the stress of the electric field can be minimized by introducing an angle on the vertical termination walls. The fabricated prototypes fulfill the initial design electrical specifications with excellent dynamic and operational behavior.

I. INTRODUCTION

Recently, the interest in power conversion systems such as interleaved converters or multiphase structures with intercell coupling device has grown up [1]. These structures offer the advantage to increase the apparent switching frequency of the converter and to improve the dynamic response and performance of the system while drastically reducing the sizes of the passive components. In order to do so, many inverter legs and interconnections are needed, thus leading to complex implementation and reliability problems. A possible solution of those problems is the monolithic integration of the active devices, of their drivers and associated functions [2]. This leads to a reduced amount of power dies and interconnections and simplifies their implementation. But the cohabitation of multiple vertical diodes or transistors in the same die requires isolation techniques to limit the electrical interactions such as the leakage currents among the power devices [3]. To separate active regions of vertical power devices integrated in a common die, a trench termination technique can be used [4]. Originally appeared in the scientific papers as a technique that allows to terminate each device by reducing the surface electric field so that the breakdown voltage is near ideal [5,6], this technique can also be used to isolate each drift region of the monolithically integrated multiple power devices. As a result, it becomes possible to integrate several power devices in a single die, all sharing the same backside contact (drain, cathode or collector).

This paper presents the monolithic integration of multiple 600V vertical power diodes. The idea is to use a deep trench vertical termination, filled with dielectric material, to terminate and to isolate each device from its neighbor while maximizing their voltage handling capability using the same termination. The paper focuses on the special care taken to minimize the stress of the electric field on the periphery of the device, acting on the angle of the termination walls. Power diodes in the range of 600V are fabricated and experimentally tested. The obtained results proved the initial design specifications.

II. DESIGN AND REALIZATION

A. Concept

The concept of the vertical voltage termination technique is to create a deep trench termination on the periphery of the device. Using a deep reactive ion etching (DRIE) technological step to obtain the desired depth and wall angle of the termination, multiple devices can be integrated in a single power die. Figure 1 shows a schematic view of the principle using power diodes as example.

As figure 1 indicates, the vertical voltage termination technique allows the parallel implementation of multiple ‘island’ power devices on common degenerated semiconductive layer – the semiconductor substrate itself - or the metal layer.

A key benefit of the vertical voltage termination is the possibility to electrically isolate the different power devices who share the same backside (cathode) electrode. This authorizes the connection of the anodes of all the devices at different potentials at the same time and with no electrical interaction among them.

The technique is also advantageous because of the opportunity to distinguish the different patterns by the etching step. In this way, assembly of several power devices can be achieved at wafer level with minimum back end additional process steps. At the same time, it simplifies the assembly and the package of multiple dies and reduces the final cost of the power module.
The technique was developed on an epitaxial wafer but is easily transferable on homogenous substrates. With such surface treatment and edge termination, power devices could also benefit of 3D interconnections replacing the wire bonds by massive copper connections. Figure 2 presents the possible evolutions of the package for multiphase bridges assembled in a 3D Power Chip on Chip configuration [7].

**B. Theoretical results**

In order to evaluate the effectiveness of the vertical voltage terminations, a detailed analysis with 2D finite elements simulations (SILVACO) has been carried out. In figure 3 is depicted the electric field distribution and the isopotential contours at the reverse voltage of 800V for a vertical PIN diode having the following characteristics – 110µm thickness of the Si substrate where 0-3µm is the depth of the P region with 3.10e17/cm3 concentration, 3-50µm is the drift N region with 2.10e14/cm3 concentration and 50-110µm N region with 1.10e19/cm3 concentration.

Figure 6 summarizes the possible effects of the addition of an angle on the wall termination as a result of the reduction of the section of the device from the P region to the N region (fig. 5). Figure 5 shows that the result of non vertical walls of the termination is a curvature to the bottom of the potential lines, which is advantageous for the voltage handling capability of the device but also for the dielectric material. As it can be seen in figure 6, the lower the angle the lower the surface electric field. However, very low angles (below 45°) are not commonly used because they require very high consummation of silicon.

![Fig. 2. Schematic view of the package using the vertical voltage termination technique. Example of a power transistor, six diodes with common cathode and a six legs polyphase rectifier](image)

![Fig. 3. Electric field distribution contours and potential lines at reverse voltage of 800V and vertical voltage termination of 100µm depth, 100µm width and 90°angle](image)

![Fig. 4. Current-voltage reverse biased characteristic of the simulated structure](image)
We have also analyzed the optimum trench depth. The results showed that the vertical voltage termination is functional to terminate and to isolate the active regions of the devices from each other only if its depth exceeds the drift and lightly doped N region depth of the substrate. In our case the drift region has a depth of 50µm coming from an epitaxy on a heavily doped substrate of 500µm and the surface electric field was found to be significantly reduced when the trench depth is greater than 50µm. Table 1 summarizes the results for the simulations of a structure with deep trench termination with 45° angle of the wall and completed with a field plate on the surface.

<table>
<thead>
<tr>
<th>Trench depth (µm)</th>
<th>Maximum electric field (kV/cm)</th>
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<tbody>
<tr>
<td>100</td>
<td>120</td>
</tr>
<tr>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>50</td>
<td>280</td>
</tr>
<tr>
<td>40</td>
<td>350</td>
</tr>
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</table>

C. Realization

Figure 7 presents SEM pictures of the realized vertical voltage termination diodes. In our case 500µm N type (100) substrate plus 55µm lightly doped (20 Ω cm) epitaxial layer was used for the fabrication of the prototypes.

All process steps except for the trenches realization – wet etching of the metal on the surface and deep reactive ion etching (DRIE) for the terminations - were performed without the need of any photolithography steps. No post processes for surface or wall treatment were performed after the silicon etching step. We obtained silicon etch rate of about 11µm/min using SF₆, C₄F₈ and He gases. We used a resist layer as masking material. The selectivity of silicon to the resist is almost 160:1. After the DRIE step the obtained depth of the vertical termination is about 100µm with 300 µm width and an angle of the termination wall of almost 87° (fig. 8).

The vertical voltage termination technique can easily be applied on homogenous substrates too. In that case silicon etching should be performed until the common metal contact layer is reached. The mechanical support for the multiple ‘island’ power devices must then be assured by the metal layer. In order to do so, it is required that the metal layer should be significantly thicker. A possible technique that can be considered is the wafer bonding of silicon and a thick metal plate (copper or molybdenum). Figure 9 shows a schematic view of the concept.
III. EXPERIMENTAL RESULTS AND DISCUSSION

For the experimental validation, the fabricated power diodes (600V, 10A) were packaged and passivated with silicone gel to protect the trench terminations and the whole power die. A metallic isolated substrate for improved thermal management was used to access the devices electrodes. The common cathode was soldered while the ‘multitude’ of anodes were wire bonded (the dies are 8x8mm²). Figure 10 shows the realized packages for 4 and 9 vertical 600V PIN diodes with common heavily doped Si layer as common cathode electrode.

![Fig. 9. Schematic view of the vertical voltage technique in the case of homogenous substrates](image)

A. Static characterization

The packaged prototypes were experimentally tested in a first time with a static characteristic power curve tracer HP 371A. Figure 11 shows the reverse characteristics of each power device in the case of testing the monolithic integration of 4 diodes (prototype figure 10a). The four curves correspond to the four power diodes integrated in the same die. All four devices fulfill the initial design specifications considering the breakdown voltage rating of 600V.

![Fig. 11. Static characteristics of the reverse biased power diodes](image)

The results show clearly that all four diodes have different voltage handling capabilities. It can be noticed in fig.10 that one of the diodes has a leakage current of 10µA while the others have leakage currents in the range of 200 µA. It has been demonstrated in previous studies [8] that the possible reason for large leakage currents is the imperfect sidewall treatments exposed the metallurgical junctions. However, in this case passivation of the power die and the termination walls was performed in a non protected atmosphere and the probable reason of the different blocking capability of the devices is a possible dust coming after dicing and before passivation of the walls.

![Fig. 12. Static characteristics of the direct biased power diodes](image)

B. Dynamic characterization

To experimentally validate the blocking capability of the diodes with vertical voltage terminations, one of the characterization tests included their implementation in a Buck power converter. The diode was not implemented as an operational switch but as a device under test to be exited by the high dv/dt created by the commutation cell of the converter. The experimental setup is shown in figure 13.

![Fig. 13. Diode with vertical voltage terminations implemented in a Buck converter](image)

The diode was connected in antiparallel with the main switch (a MOSFET transistor) and the tested diode was
excited with the same voltage as the transistor. No load current was allowed to flow through the device under test, and only HF currents created by the dynamic behavior were observable. The aim of this test was to evaluate if the diode was able to sustain the dynamics of the commutation and to maintain the voltage handling capability of the power MOSFET.

Fig. 14. Dynamic characteristics of the fabricated power diode a) current and voltage at the switching periods of the MOSFET, b) zoom at the off state with $\frac{dV}{dt}=450V/50ns=9kV/\mu s$

In figure 14 are depicted the obtained results with corresponding switching voltage waveforms (red curve) and dynamic current through the diode under investigation (blue curve). The diode demonstrated an excellent functional behavior of $9kV/\mu s$ ($dV/dt$).

C. Implementation of the multidiode device into an interleaved converter

In order to validate the approach, the implementation into an interleaved converter has been carried out. This validation is only partial since the converter was initially designed for 200V devices. Nevertheless, it gives an idea of the operation of several power devices sharing the same substrate and being islanded by the technique and the approach we have presented in this paper. The topology considered is a boost chopper with three commutation cells and three inductors, the diodes in the commutation cells are all sharing the same cathode electrode. The topology is depicted on figure 15a).

Figure 15b) presents a picture of the converter where its boost diodes have been replaced by our multidiode chip. Figure 16 and 17 present practical results where it is possible to observe one transistor VDS voltage (dark blue curve on fig.16 and fig.17) and several current waveforms in the diodes (black curve on fig.16, black, grey and clear blue curves on fig.17) and current in one of the inductors (clear blue curve on fig.16). The waveforms exhibit high frequency oscillations at numerous time locations during the switching period because the interconnections have poor quality and the duty cycles have been phase shifted at 120° in order to take advantage of the structure from a filtering point of view.

Fig. 15. Multidiode chip implemented in an interleaved Boost converter a) schematic view, b) picture of the experimental setup

Fig. 16. Experimental results for one commutation cell -VDS voltage waveforms for the transistor, current trough the diode and current trough the inductor
Fig. 17. VDS voltage waveforms for one of the transistors and current through the tree diodes of the multidiode chip.

The results correspond to what could be expected from the converter. The correct sharing among the boost legs indicates that they are very comparable since no feedback was implemented to equally split the load current among the three boost converters.

IV. Conclusion

The integration of multiple power diodes into a single die was presented. It is based on vertical voltage termination and isolation technique. The proposed technique contributes considerably to integrate the active parts of the complex converter by reducing the interconnections among the power devices.

The fabricated prototypes proved that the vertical voltage termination improves the electrical performance of the devices in terms of breakdown voltage while completely isolating their active regions – there is no electrical interaction between the different power devices other than the common backside potential.

The proposed technique simplifies the packaging. Using a deep reactive ion etching process step as a final processing step allows distinguishing the different patterns while maintaining simple the fabrication of the devices. The cost trade-off between packaging saving and wafer process additions should be further investigated.

The thermal coupling of the devices and the effects on trench isolation on the reverse biased leakage current and its temperature behaviors should be the purpose of future research studies.

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