# Package Influence On Conducted Mode Emissions in a Digital Integrated Circuit : a case study

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# *Package Influence On Conducted Mode Emissions in a Digital Integrated Circuit : a case study*

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***Abstract***
*The work presented in this paper deals with the study of conducted-mode parasitics generated in digital circuits. Current propagation between ground connection of the integrated circuit and the global ground was experimentally analyzed and simulated with its short connections as well as with its package . Validation of our method was done by comparison between measurements and simulation.*

## 1. Introduction

Nowadays, it is clearly stated that perturbations generated by digital integrated circuits have to be taken into account as soon as in the design phase. These perturbations rise from current pulses related to state changes in logical gates. However, the characteristics of these pulses closely depend from the environment of the integrated circuit, thus making it compulsory to model its behavior towards these transitions.

In high density integrated circuits containing hundreds of thousand of gates (and even more), the behavioral study in components can be achieved by an analog simulation of the digital core. The method presented in this paper consists in rebuilding the power supply network current profile.

In order to improve this model, a study was conducted from a 16-bit asynchronous counter in 0,6 µm CMOS technology, the parameters of which are well known.

## 2. Measurement methodology

The setup which makes this study possible is built on a square, double-sided PCB (10 cm for each side). Both ground planes are connected by vias. The integrated circuit lies on one side

which is covered by the ground plane except on the area where the chip, the pads used for bonding and the vias that connect with the other face are located.
The other side includes power supply, clock, reset connections and also passive components, all useful for our experiment.

## 2.1 Printed circuit board

In fact, the counter chip was laid out on a PCB with connections as short as possible ; then, current pulses were measured from the voltage generated on the terminals of a 1–Ω resistor in series between chip ground and PCB ground. This work allowed us to present a model taking into account the behavior of both the chip and its environment as it is shown in figure 1 and figure 2.

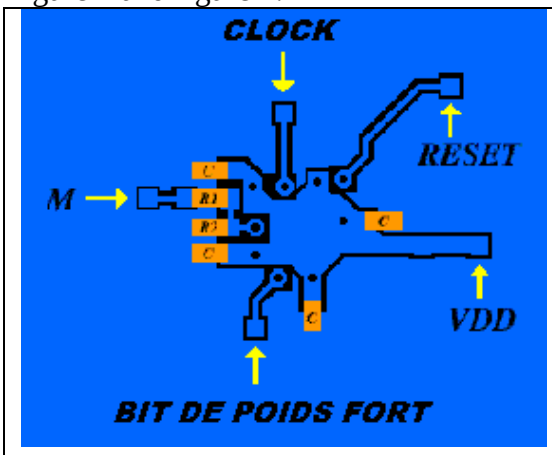


Figure 1

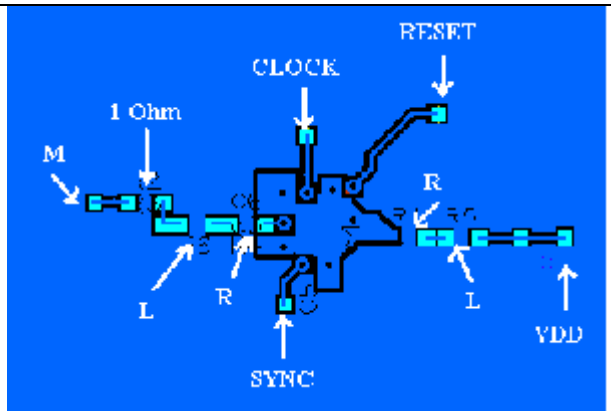


Figure 2

Figure 1:PCB in case of short connections
Figure 2 : PCB with R and L in place of package

On figure 2, package is replaced by passive elements such as resistance R and inductance L.

## 2.2 Consumed current measurement

In order to measure the consumed current in the integrated circuit, the voltage across a 1 Ohm resistance between the chip ground and the PCB ground has been measured. Figure 3 shows the principle of this method.

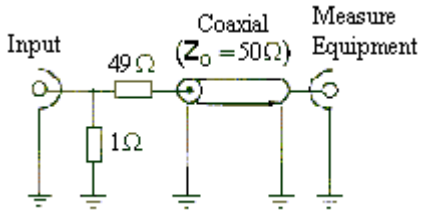


Figure 3 : Measurement setup

## 2.3 Environmental measurement

To study the simulated response of the circuit, it seems necessary to characterize the measured circuit with respect to frequency. This becomes possible with the help of a network analyzer HP8753D which provides S parameters in 30kHz-3GHz frequency band.

Between the chip ground and the PCB ground, the environment is supposed to be a quadripole whose input is chip ground and PCB ground and output is the measurement setup (50 ohms) as shown in figure 4 where solid lines represent measurement results.

The input impedance of this quadripole has been modelled as two parallel branches in an electrical circuit : the first branch is 1 ohm resistance in series with and an inductance (35 nH) and the second branch is a capacitance (1.26 pF) in series with an inductance (4nH). This impedance is represented in figure 4, dotted lines represent the impedance obtained with these elements.

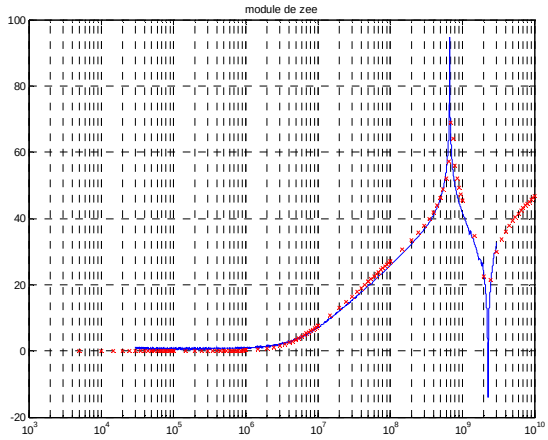


Figure 4 : Input impedance of the quadripole and modelled impedance ( L, R and C)

Figure 5 displays the impedance between the power supply connection and the PCB ground modelled as a dipole

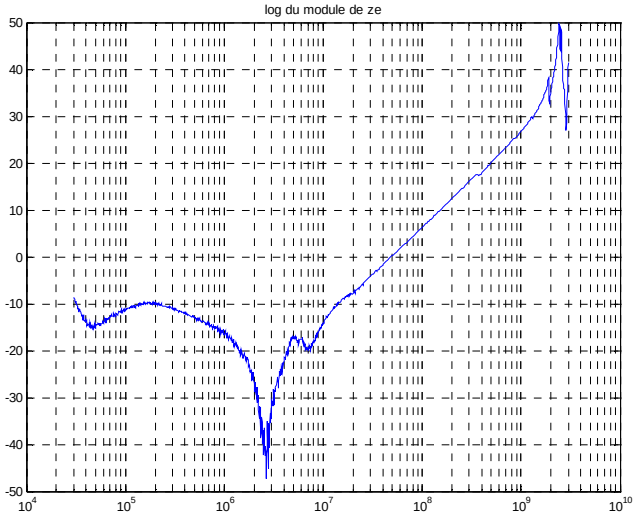


Figure 5 Power supply-ground PCB impedance

## 3 . Measurement results

In order to study the chip behavior, measurements were performed in the case of short connections. Research was further conducted in order to model the behavior of the chip now inserted in its package. In fact, by supposing that the influence of the package was concentrated on the power and ground supply connections of the chip, and that these could be replaced by a resistor R in series with an inductor L, the study was carried out by placing the die on a PCB including the measurement circuitry as well as the elements representing the package. In order to compare simulation and measurements, the behavior of the circuitry external to the die (PCB tracks, R and L devices, power supply) was studied from S-parameters. In this last case, measurements were achieved with R=0 and R=0,6 Ohm and with L=2.7 nH and L=20 nH.  The results presented below concern the short connections case and the case where  R=0 Ohm and L=20nH.

Figure 6 shows the obtained results with short connections whereas figure 7 shows the case where  R=0 Ohm and L=20nH.

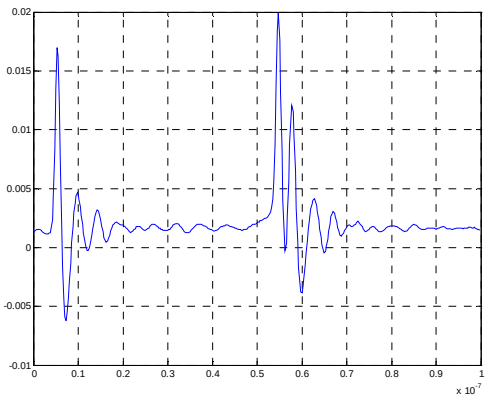

Figure 6

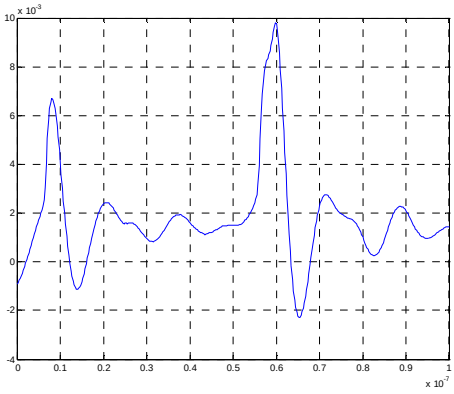

Figure 7

Figure 6: Short connections case
Figure 7: Case: R=0 and L=20nH

## 4. Simulation results

### 4.1 Short connections

Simulation was performed first with a circuit extracted from chip layout (figure9) and then with an equivalent electrical schematic (figure 8).  The obtained results seem to be identical.

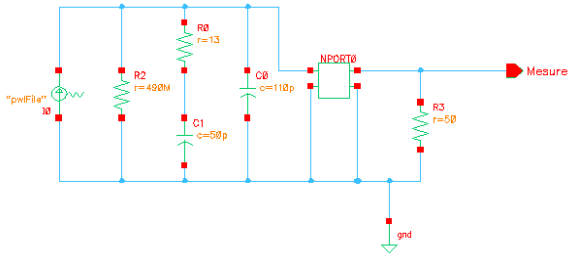


Figure 8  Equivalent electrical scheme used for simulation

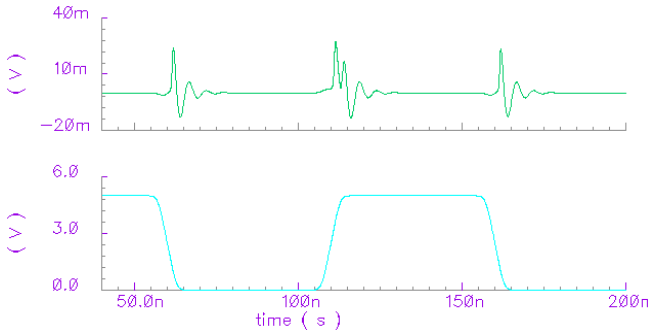


Figure 9 : Simulation results in case of electrical circuit extracted from layout

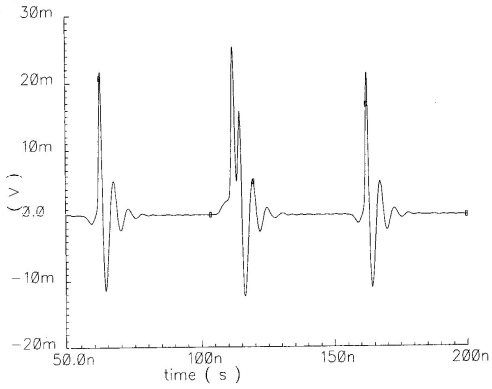


Figure 10 : Simulations results with the short connections and equivalent electrical schematic

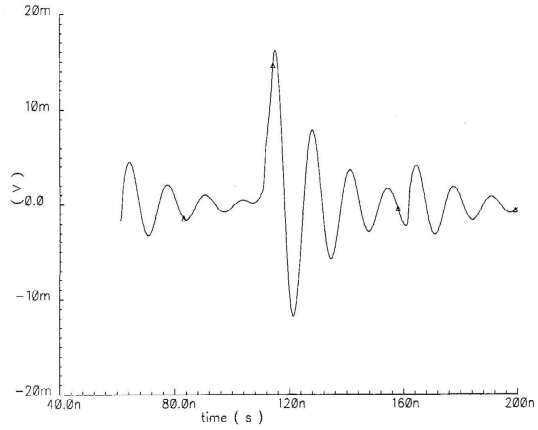


Figure 11: Simulation results with R and L and equivalent electrical schematic

## 4.2 Chip with package

Starting with the equivalent electrical schematic and also with the circuit extracted from layout , we obtained the results shown respectively in figure 11 and 12. Correlation between these results and experimental results illustrated in figure 7 does not seem so good.

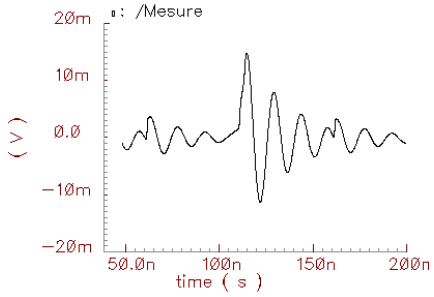


figure 12 : Extracted circuit simulation

The chip behavior (chip isolated from the remaining circuit) in terms of frequency was studied starting from S parameters. The input impedance (in dB) is represented in figure 13. This circuit can be modelled as a circuit containing a 2-ohms serial resistance, a 115pF capacitance and 3,7 nH inductance , all in parallel with a 710 ohms resistance. Correlation between results and simulation does not look very good.

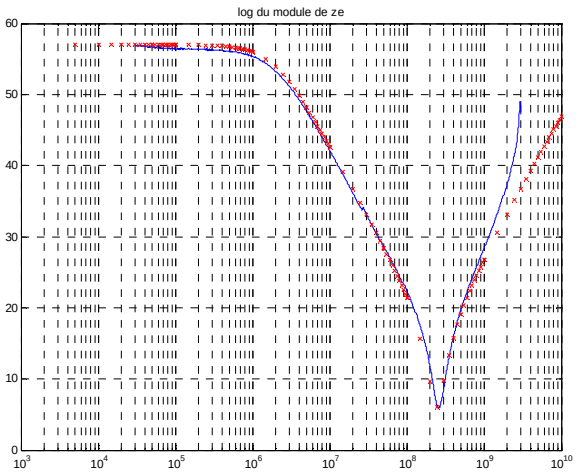


Figure 13 : Measured input impedance of the chip

## 5. Conclusion

In this paper, package influence on conducted mode emission was studied. A comparison was done between simulations and measurements with a chip with short connections as well as with its package modelled as a resistance R in series with an inductance L. In the first case, the correlation between simulations and measurements seems to be correct. In the second case, the comparison shows some discrepancies because there are differences in the spectra of current pulses in both studied cases, and also because the i(t) current which propagates during a state change does not charge only the parasitic capacitance of the chip, and also because both transistors in CMOS cells are in the ON state during a very short time.
Further research is being conducted to take this effect into account in order to improve our model.