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80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes

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This paper presents the high frequency performance of single-walled carbon nanotube (SWNT) field-effect transistors, with channel consisting of dense networks of high purity semiconducting SWNTs. Using SWNT samples containing 99% pure semiconducting SWNTs, we achieved operating frequencies above 80 GHz. This record frequency does not require aligned SWNTs, thus demonstrating the remarkable potential of random networks of sorted SWNTs for high frequency electronics. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3155212]

As a result of their excellent electrical and mechanical properties, semiconducting single-walled carbon nanotubes (SWNTs) are considered prime candidates for the "beyond complementary metal-oxide-semiconductor" era.[1] Using individual SWNTs as a device channel, logic devices and circuits such as field effect transistors[2–4] (FETs), complementary metal-oxide devices,[5,6] and ring oscillators[7] have been demonstrated. In the field of analog circuits, devices based on individual nanotubes face two major problems: the high input impedance of a SWNT and low drive currents in the on state. To circumvent these issues, devices based on an array of SWNTs as the channel are required.[8–13] However, all nanotube synthesis methods invariably produce a mixture of both metallic and semiconducting nanotubes. As a consequence, the performance of network-based devices[8,9,14,15] has been limited by the presence of metallic nanotubes.

In this work, we demonstrate that high performance SWNT FETs can be produced using SWNT solutions consisting of 99% pure semiconducting nanotubes. These highly enriched nanotube dispersions produced using density gradient ultracentrifugation[16] are used to form a dense network of randomly oriented SWNTs. Briefly, the device structure [Figs. 1(a) and 1(b)] is similar to the one described in our previous work. The device is made on a high-resistivity silicon substrate. The device is a back gated transistor with a 2 nm thick aluminum oxide dielectric layer fabricated from a thin film of aluminum oxidized at low temperature. SWNTs were deposited on the gate area using a combination of surface chemistry[17–19] and dielectrophoresis (DEP). Because of the semiconducting nature of the SWNTs used, DEP does not induce alignment (in the range of the deposition frequencies used), in strong contrast with conventional SWNT solutions.[14] Figure 1(c) shows a randomly oriented SWNT network deposited on the gate electrode before source and drain contact formation. The final SWNT FET structure is a dual gate FET with gate length of 300 nm, and total width of 20 μm (10 μm per gate).

Direct current (dc) characterization (Fig. 2) shows high drain to source current (I_{DS} up to -10 mA at $V_{GS}=-1$ V in the best case) in good correlation with the high density of nanotubes in the device channel. The devices do not show pinch-off, most likely as a result of small numbers of metallic nanotubes in the channel, which may be preferentially deposited by DEP.[20] The maximum dc transconductance is close to 2.66 mS at $V_{DS}=-2.5$ V, with the minimum dc conductance g_d close to 4 mS.

Considering our previous work on SWNT FET devices with unsorted nanotubes as the channel, we can define, at a given V_{DS} bias, a factor of merit as a ratio of the effective contribution of semiconducting nanotubes to the total dc current versus the associated gate control bias range,

$$f_{Merit}=\frac{\Delta I_{sc}}{\Delta V_{GS}}=\frac{I_{DS\,max}-I_{DS\,min}}{\Delta V_{GS}}.$$

This factor (which has the same units as transconductance) is related to the number of nanotubes per unit area and to the

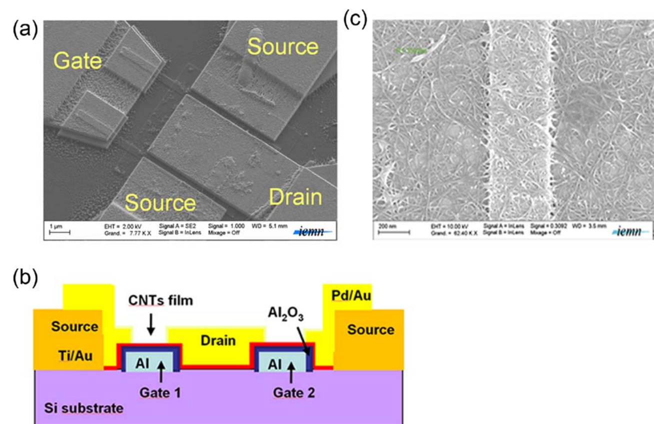

FIG. 1. (Color online) SWNT FET schematic representation: (a) plan view, (b) cross-sectional representation, (c) scanning electron microscopy image of carbon nanotubes deposited on the gate electrode, before source and drain contacts deposition.

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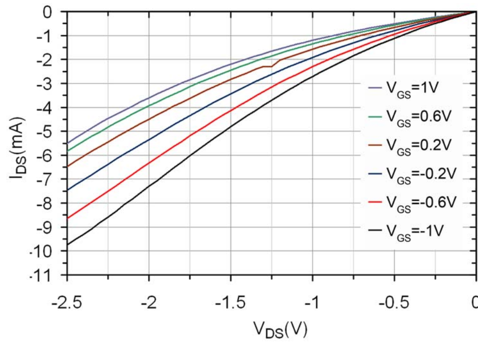

FIG. 2. (Color online) Measured dc I_{DS} vs V_{DS} at different V_{GS}.

ratio of semiconducting and metallic nanotubes. We report in Table I characteristics of three device types, each having the same structure at similar bias points.

In the first case (I),[9] a conventional SWNT solution with ~2/3 of semiconducting nanotubes is used in combination with a surface chemistry selective deposition technique. In the second case (II),[14] DEP is employed in addition to selective deposition in order to increase the area density and alignment of nanotubes. Unfortunately, DEP strongly favors the deposition of metallic nanotubes. The contribution of metallic to the dc current is thus very high.

In the third case (III), a solution with 99% pure semiconducting nanotubes is used with the same combination of DEP and surface chemistry as in case (II). The influence of DEP during deposition is negligible.

One can observe that f_{Merit} increases as the area density of semiconducting nanotubes increases (case I to case II) and that the best value is obtained in case III where the density of semiconducting nanotubes is maximized. Even though the nanotubes are randomly oriented, a significant improvement of dc performance is obtained. In the following, we show how it impacts rf performance.

Microwave measurements were performed using an Agilent E8361A PNA series network analyzer from 100 MHz to 55 GHz. The measurement and de-embedding techniques are similar to those described in our previous work.[14] To calculate extrinsic parameters, the influence of coplanar accesses are removed from the S parameters measurements using specific structure illustrated in Fig. 3(a). These extrinsic parameters are considered as the actual high frequency characteristics.

TABLE I. Characteristics of three device types. Case I corresponding to a FET where conventional SWNTs were deposited by selective surface chemistry. Case II corresponding to a FET where conventional SWNTs were deposited by DEP. Case III corresponding to a FET where 99% pure semiconducting SWNTs were deposited by DEP.

	Case I (V_{DS}=1 V)	Case II (V_{DS}=1.5 V)	Case III (V_{DS}=1.5 V)
$I_{DS\ max}$	1.53 mA (V_{GS}=−2 V)	21 mA (V_{GS}=−2 V)	5.0 mA (V_{GS}=−1 V)
$I_{DS\ min}$	0.8 mA (V_{GS}=2 V)	20 mA (V_{GS}=0 V)	2 mA (V_{GS}=1 V)
ΔV_{GS}	4 V	2 V	2 V
f_{Merit}	0.18	0.5	1.5
g_m (dc)	220 μS	500 μS	1.6 mS
g_d (dc)	0.8 mS	15 mS	4 mS
g_m/g_d	0.275	0.03	0.4

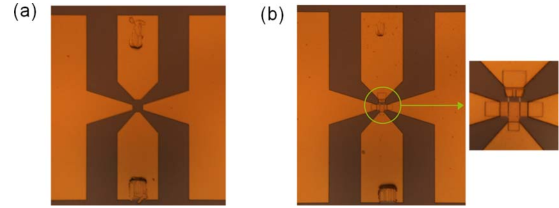

FIG. 3. (Color online) Structures used for de-embedding. (a) Structure used to extract extrinsic performance. (b) Structure used to extract intrinsic performance.

To calculate intrinsic parameters, an "open" test structure is used [Fig. 3(b)] for de-embedding. This open structure is strictly identical to the active structure with CNTs except that no nanotube is deposited in the gate area. So every parasitic parameters close to the gate-electrode regions (fringing capacitances, gate-drain and gate-source overlap capacitances, etc.) are removed. With this technique, contact resistance between accesses (source and drain) and array of nanotubes are not removed. It should be noted that test structures, which are passive, are fabricated on the same wafer as active structures (SWNT FETs).

The current gain (H_{21}), the unilateral gain (U) and the maximum stable gain (MSG) characteristics obtained from this de-embedding procedure are plotted in Fig. 4. H_{21} and MSG curves present −20 and −10 dB/decade slopes, respectively, in agreement with theory. The extrinsic and intrinsic current gain cutoff frequencies (f_{t_ext} and f_{t_int}) are ~15 and ~80 GHz, respectively (Fig. 4). The unilateral gain, deduced from S parameters shows the maximum frequency of oscillation f_{max}=3 GHz, which is smaller than f_t. This limitation is due to some parasitics such as the gate resistance, contact resistance, etc.

Considering a device without parasitic losses, f_t is defined by $f_t = g_m / 2\pi C_{gs}$ so that improvement of g_m is directly reflected in f_t. Figure 5 shows the comparison of current gain in our three device types. The improvement of cutoff frequency is related to the high density of semiconducting SWNTs in the channel. Indeed, in the case III, current is mainly due to the semiconducting tubes contrary to case II, where the density of metallic tubes is higher. As a consequence, the factor of merit of the new device is three times higher than the previous one (case II), even if the maximum

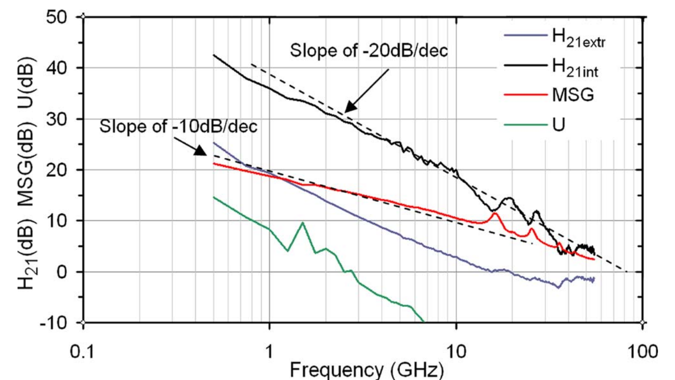

FIG. 4. (Color online) Current gain 10 log 10($|H_{21}|^2$), MSG, U (in decibels), extracted from the S parameters. The dashed lines correspond to the ideal slopes of −20 dB/decade for $|H_{21}|$ and −10 dB/decade for MSG.

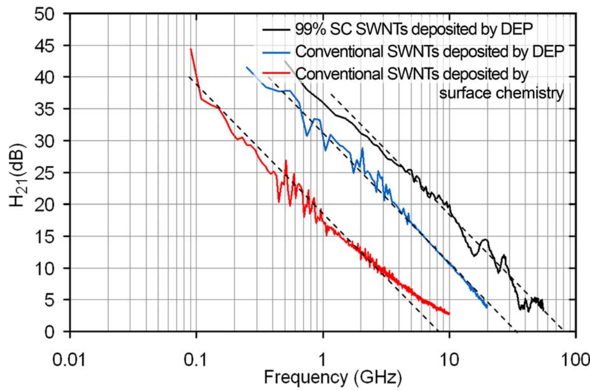

FIG. 5. (Color online) Current gain 10 log 10($|H_{21}|^2$), extracted from the S parameters for the three SWNT FET cases. The dashed lines correspond to the ideal slopes of −20 dB/decade for $|H_{21}|$. The respective f_t are: 8 GHz, 30 GHz and 80 GHz.

current is two times lower. The same improvement is obtained with f_t. These experimental results are in accordance with trends of simulation results.[21]

In summary, solutions of 99% pure semiconducting nanotubes were used to fabricate SWNT FETs for rf analog applications. The device channel is composed of a high area density network of randomly oriented SWNTs. The dc characterization indicates improvement in terms of current level and ratio between semiconducting nanotube current versus metallic nanotube current. The high frequency characteristics also indicate significant improvement in terms of both extrinsic and intrinsic cutoff frequencies. The extrinsic and intrinsic current gain cutoff frequencies are ~15 and ~80 GHz, respectively. The maximum available gain is positive up to 3 GHz. Most importantly, this work shows that precise alignment of SWNTs is not required to achieve high frequency performance. This lifts a strong constraint in terms of fabrication processes, thus opening the route for realistic application of nanotubes in randomly oriented networks.

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