

Phase Noise Analysis of PLL Based Frequency Synthesizers for Multi-Radio Mobile Terminals

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Abstract— This paper deals with phase noise analysis and design aspects of PLL based frequency synthesizers for cognitive multi-radio mobile terminals. Principal features of PLL based frequency synthesizers are presented and simulated. This document describes various issues of the loop filter design and the overall impact on the frequency synthesizer performance in terms of the phase noise, settling time and the spurious suppression capability. Phase noise requirements for main communication standards in the frequency band 800 MHz to 6 GHz are investigated as well.

Keywords—frequency synthesis; phase locked loop; phase noise; cognitive radio; multi-radio

I. INTRODUCTION

During the recent past, there has been a significant progress in wireless communications in terms of the integration of various communication standards into a single mobile terminal. Instead of using multiple transceivers for different standards, the goal is to employ a single reconfigurable radio transceiver that is able to achieve all requirements of different communication standards. The goal of this evolution is to reduce the number of external components and to increase the integration in the low-cost CMOS technology. Another stage which pursues the evolution towards the cognitive radio and implies flexibility of each stage of the communication chain is the cognitive multi-radio. Cognitive multi-radio has the capability of the multi-standard concept and moreover it is capable to perform an efficient environment spectrum scanning in order to switch accordingly to an appropriate communication standard.

Single chip radios that support WLAN 802.11 a/b/g standards have already been proposed in [1], [2]. Another example of integration of cellular standards GSM 900/1800 and UMTS in a single chip can be found in [3]. These multi-standard proposals are mainly based on the direct conversion technique which is the most suitable techniques for 2G, 3G and 4G multi-radio terminals [4]. This is due to the fact, that the direct conversion eliminates the sensitivity to the image frequency and hence, it is not necessary to build any additional filters for the image rejection. One of the most challenging tasks in the multi-radio transceiver is the design of the frequency synthesizer. Frequency synthesizer has to provide all necessary frequencies for the down and up conversion with

proper channel spacing that corresponds to the channel bandwidth and the raster of the communication standard. Frequency switching has to be performed agilely, with respect to settling time requirements. Moreover, the local frequency synthesizer has to fulfil the tightest signal purity requirements which can be expressed in terms of the phase noise and the spurious output. These requirements given by standards in the frequency band 800 MHz to 6 GHz, namely by GSM, UMTS, Bluetooth, WiFi and Mobile WiMAX, are summarized in Table 1 [5]-[9].

It can be seen, that the most critical local oscillator requirements in terms of the phase noise are imposed by the GSM standard. This is due to the fact that the powers of the in-band unmodulated interfering signals, so called blockers, are at a very high level. Fig. 1 displays the in-band blocking profile of the GSM 900 standard with three unmodulated blockers at different offset frequencies from the desired GMSK signal. The desired GMSK modulated signal is 3dB above the sensitivity of the receiver [10].

TABLE I. RF SPECIFICATIONS FOR THE MULTI-RADIO FREQUENCY SYNTHESIZER

Standard	Frequency Band [MHz]	Channel / Raster [MHz]	Settling Time[μ s]	Phase Noise [dBc/Hz]
GSM 900/1800	880-960	0.2/0.2	577	-122@0.6 MHz
	1710-1880		150 (GPRS)	-132@1.6 MHz -139@3 MHz
UMTS FDD/TDD	1920-2170	5/0.2	200	-132@3 MHz
	1900-2025			-132@10 MHz -144@15 MHz
Bluetooth	2402-2480	1/1	150	-84@1 MHz -114@2 MHz -129@3 MHz
Mobile WiMAX IEEE 802.16e	2300-2400	3.5-10 / 0.25	< 100 (HFDD)	Phase Jitter < 1° rms
	2305-2320			
	2469-2690			
	3300-3400			
	3400-3800			
WiFi IEEE 802.11a	5150-5350	20/20	500	-102@1 MHz -125@25 MHz
	5470-5825			
WiFi IEEE 802.11b	2412-2472	20/5	225	
WiFi IEEE 802.11g	2412-2472	20/5	225	

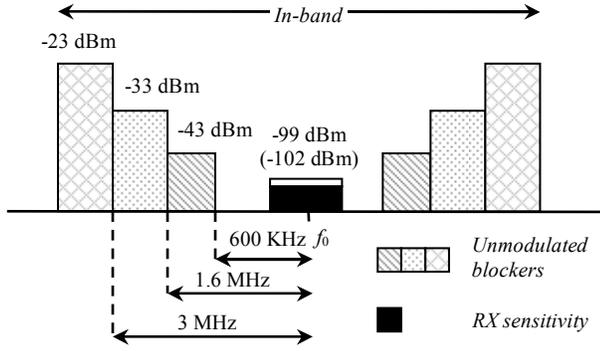


Figure 1. GSM 900 in-band blocking profile.

Since the local oscillator generates undesired sideband energy rather than a pure frequency tone, reciprocal mixing will occur during the direct conversion. The reciprocal mixing can potentially result in a translation of the undesired blocker into the desired band at the output of the mixer. This will lead into a rapid signal-to-noise deterioration. Hence, the frequency synthesizer must be designed in such a manner, that the reciprocal mixing of the phase noise of the oscillator with the blocker will produce an interference component far below the desired signal power. Based on the blocking profile defined by the intermodulation test, phase noise $S[dBc/Hz]$ requirements of the local oscillator can be calculated for particular standards as follows:

$$S[dBc/Hz] \leq P_{des.}(dBm) - P_{bl.}(dBm) - SNR(dB) - 10 \log(BW), \quad (1)$$

where $P_{des.}$ represents the desired signal power, $P_{bl.}$ is the blocker power level and BW is the channel bandwidth. SNR defines the required signal-to-noise ratio for given BER.

Various approaches for multi-standard frequency synthesizers have been proposed in [11]-[13], considering wideband tuning range VCO, use of multiple PLL loops or all digital PLL design. Although there are many techniques for frequency synthesis, the dominant technique used in wireless technology is based on the PLL principle. This technique is considered in this article since it offers high performance in terms of the reconfigurability, fine step size and phase noise. First, a linearized PLL model is described along with characteristic transfer functions. Furthermore, the main noise sources in the PLL circuit are studied and simulated with emphasis on the noise analysis of the loop filter.

II. PLL ARCHITECTURE

A. PLL Linearized Model

Fig. 2 displays a simplified linearized model of the PLL. This model includes a charge pump phase-frequency detector CP/PFD with the gain K_d , a loop filter with the transfer function $F(s)$, a VCO with the gain K_0/s and a frequency divider dividing by N . The gain K_d can be written as:

$$K_d [A/rad] = I_{cp} / 2\pi. \quad (2)$$

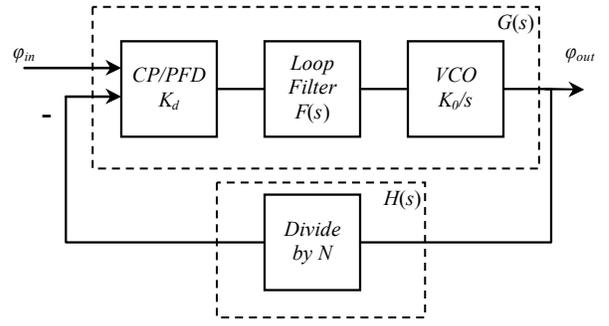


Figure 2. Linearized negative-feedback PLL model.

CP/PFD generates the charge pump current I_{cp} which is proportional to the phase and frequency difference between the reference and the feedback signal. Furthermore, the charge pump current is low pass filtered by the loop filter and is applied to the control input of the VCO. Divide ratio N can be an integer or a fractional value. As explained later, the value of N has a considerable impact on the in-band PLL phase noise performance. According to the control theory, the effect of a closed feedback loop on the input signal φ_{in} can be described by the closed loop transfer function $T(s)$ as:

$$T(s) = \frac{\varphi_{out}(s)}{\varphi_{in}(s)} = \frac{G(s)}{1 + G(s)H(s)} = \frac{\frac{K_d K_0}{s} F(s)}{1 + \frac{K_d K_0}{s} F(s) \frac{1}{N}}, \quad (3)$$

where the $G(s)$ represents the forward transfer function and the term $G(s)H(s)$ open loop transfer function. $H(s)$ corresponds to the division factor $1/N$. Since the input signal at the loop filter is the charge pump current I_{cp} , the filter transfer function represents the transimpedance (current to voltage conversion). For the second order filter, as shown in Fig. 3, the transimpedance is expressed as:

$$F(s) = \frac{1 + sC_2R_1}{s(C_1 + C_2) \left(1 + s \frac{C_1C_2R_1}{C_1 + C_2} \right)}. \quad (4)$$

In order to boost the reference spur suppression at the output of the PLL, additional RC low pass stages can be added [14]. However, additional passive components will contribute to the total phase noise at the output of the PLL.

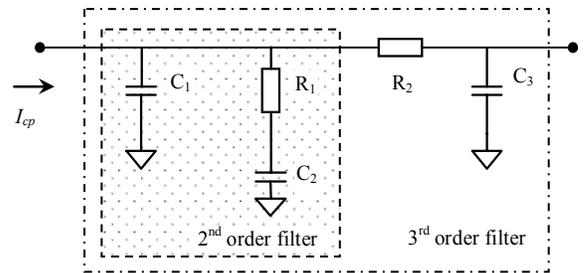


Figure 3. Second and third order passive filter.

III. PLL PHASE NOISE SOURCES

In the PLL based frequency synthesizers, the phase noise performance becomes a very important design issue. The phase noise phenomenon can be a result of the thermal noise, shot noise, $1/f$ noise in all the active or passive components. In this paper, we will analytically describe the phase noise behavior in the PLL circuit for the following noise sources: reference oscillator noise, VCO noise and loop filter noise. Moreover, noise contribution from the loop filter will be examined for different values of the charge pump current.

A. Reference Noise

Phase noise performance of the reference oscillator has been predicted with help of the Leeson's model [15] as

$$S_{ref}(f_m)[dBc/Hz] = 10 \log \left[\frac{FkT}{2A} \left(1 + \frac{1}{f_m^2} \left(\frac{f_0}{2Q} \right)^2 \right) \left(1 + \frac{f_f}{f_m} \right) \right], \quad (5)$$

where f_m is the frequency offset, F represents the noise figure of the oscillator, k is the Boltzmann's constant $1.38 \cdot 10^{-23}$ J/K, T is the absolute temperature, A is the output power of the oscillator, Q is the loaded quality factor of the resonator, f_0 is the carrier frequency and f_f is the flicker corner frequency. According to Fig. 2, the transfer function of the reference oscillator's noise S_{ref} injected at the input of the PLL corresponds to the low-pass filter function G_{LPF} with the loop bandwidth B_{PLL} . B_{PLL} is the frequency at which the open loop gain magnitude equals one. Phase noise contribution $S_{ref,out}$ from the reference oscillator to the PLL output becomes:

$$\begin{aligned} S_{ref,out}(f) &= S_{ref}(f) \left(\frac{1}{H(f)} \right)^2 \left| \frac{G(f)H(f)}{1+G(f)H(f)} \right|^2 \\ &= S_{ref}(f) N^2 |G_{LPF}(f)|^2. \end{aligned} \quad (6)$$

Fig. 4 demonstrates that the reference noise is low-pass filtered and hence the phase noise contribution at the PLL output becomes dominant at lower frequency offsets. Moreover, the reference phase noise is amplified by factor N , which is in this example equal to 2439 (≈ 67.8 dB). In order to keep the in-band phase noise low, the division factor should be set as low as possible. This problem is solved by fractional- N dividers that can provide arbitrary small frequency resolution without the need of low reference frequency. Hence, the in-band phase noise performance is improved significantly [5].

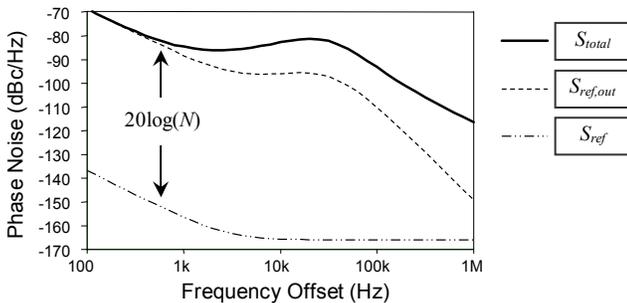


Figure 4. Reference oscillator noise performance at the input and at the output of the PLL. Moreover, total phase noise at the PLL output is shown.

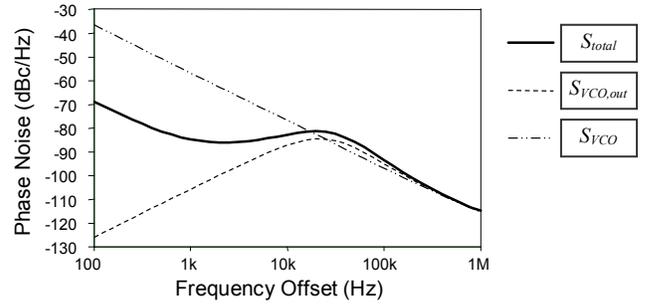


Figure 5. Noise performance of the VCO for open and closed loop case.

B. VCO Noise

VCO phase noise S_{VCO} has been modeled according to the Leeson's model as in (5). The transfer function is calculated similarly as in the reference noise case. The noise injected this time at the output of the VCO is high-pass filtered and hence the contribution of this noise to the PLL output reads:

$$S_{VCO,out}(f) = S_{VCO}(f) \left| \frac{1}{1+G(f)H(f)} \right|^2 = S_{VCO}(f) |G_{HPF}(f)|^2. \quad (7)$$

Due to the high-pass filtering, the VCO noise will be suppressed within the loop bandwidth B_{PLL} and the dominant noise contribution will appear at higher frequency offsets. This phenomenon is depicted in Fig.5. Furthermore, the out-band phase noise will drop to the noise floor of the VCO, which is defined by oscillator's output power A (power available from the frequency selective circuit) and the system's noise figure F . The total integrated phase noise at the output of the PLL can be minimized by means of B_{PLL} reduction, however this will lead to settling time degradation. Hence, the tradeoff between the minimum loop bandwidth and the settling time has to be taken into account for design. A simplified tradeoff is presented in [5] as $B_{PLL} = 4 / t_{lock}$, where t_{lock} is the settling time. Since the settling time requirements differ for various standards, a multiple loop approach or reconfigurable loop filter design might be considered for multi-radio applications.

C. Loop Filter Noise

A passive loop filter consists of only resistive and capacitive components. Hence, the output voltage noise is the result of the thermal noise present in the real part of the complex admittance of the loop filter. Two sided PSD of current fluctuations is defined by the Nyquist equation as:

$$S_{fil}(f) \approx 2kT \text{Re}(Y(f)), \quad (8)$$

where Y is the loop filter admittance that corresponds to the inverse filter transimpedance $1/F(f)$. Furthermore, this thermal noise is band-pass filtered by the PLL and the phase noise contribution to the output of the PLL results in

$$S_{fil,out}(f) = S_{fil}(f) |F(f)|^2 |K_0 / j2\pi f|^2 |G_{HPF}(f)|^2. \quad (9)$$

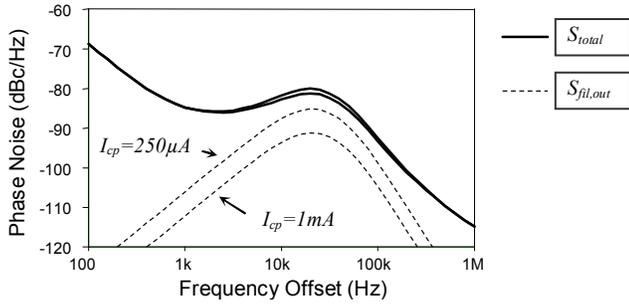


Figure 6. PLL phase noise performance with all phase noise contributors.

Fig. 6 presents the loop filter noise contribution to the PLL output for two different values of the charge pump current. This simulation has been performed for the second order filter. If the charge pump current is increased while keeping the transfer function of the loop filter unchanged, the thermal noise will be reduced since the value of the loop filter resistor had been decreased in order to keep the same output voltage. In this particular simulation, the noise generated by the loop filter was reduced by 6 dB.

Above presented simulations consider only second order filters. However, for more efficient filtering of undesired spurious signals, higher filter order is desired (see Fig. 3). Phase noise analysis of the third order filter has been carried out for two filters with identical transfer functions but different component values. The position of poles and zeros does not differ and hence the stability and the settling time are unaffected in both loop filter configurations. Values of passive components are displayed along with the phase noise performance in Fig. 7. In the first scenario, loop filter passive components add 3.3 dB more to the total phase noise in the B_{PLL} region compared to the second scenario. This deterioration can also be expressed in the time domain as the integrated phase noise (rms phase jitter σ_{rms}) in the band defined by f_1, f_2 .

$$\sigma_{rms} [^\circ] = \frac{360}{2\pi} \sqrt{2 \int_{f_1}^{f_2} S_{total}(f) df} \quad (10)$$

Phase jitter has been calculated within the frequency offsets 1 kHz and 10 MHz from the central frequency of 2.44 GHz. Deterioration of the phase jitter due to the inconvenient loop filter design has reached 0.77 degrees.

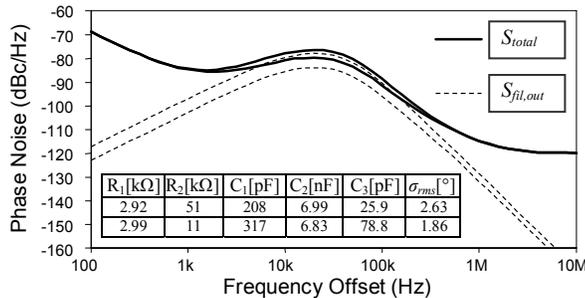


Figure 7. Third order loop filter noise contribution for different component values. Filter transfer function remain constant for both cases.

IV. CONCLUSION

This paper reviews frequency synthesizer requirements of the most common standards in the frequency band 800 MHz to 6 GHz. In order to meet demanding synthesizer requirements for considered standards, understanding of the phase noise behavior in the PLL becomes critical. The most challenging synthesizer design issues for the cognitive multi-radio are dictated by GSM and WiMAX standards. More precisely, GSM standard with very straighten phase noise requirements due to large allowed interferers and WiMAX standard due to very low settling time. Because of the diverse requirements of communication standards, a multiple frequency synthesizers will have to be considered. A very efficient technique for reconfigurable synthesizers comprise fractional- N PLL synthesizers that can achieve very small frequency resolution equal to the fractional portion of the reference frequency and hence improve the in-band phase noise performance compared to the integer- N PLL. It has also been shown that the noise contribution of the loop filter and the phase jitter can be reduced by means of the charge pump current optimization and by optimizing values of loop filter components. This approach for the design of modern high performance frequency synthesizers will have to be considered in order to achieve the high performance of the cognitive multi-radio transceivers.

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