On Flexibility and Reconfigurability of a Hybrid Mode Frequency Synthesizer for Multi- Radio Applications

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Abstract: *This paper describes the background and main outcomes of a research project supported by the Czech Grant Agency under the grant number 102/08/H027. The project describes architecture and performance of a dual mode frequency synthesizer that has been proposed for multi-radio operation. An overview of results that have been carried out during the second year of activity of the grant project is presented as well.*

1. Introduction

The increasing number of wireless communication standards calls for a multi-band and multi-standard radio operation. An approach frequently used in multi-standard wireless devices employs multiple chips, each one dedicated to a particular standard. This approach provides the best RF performance for individual standards, but it significantly penalizes the IC integration and power consumption. Therefore, a single multi-radio transceiver able to fulfil requirements of multiple standards becomes a challenge. Multi-radio transceiver should be able to cope with various waveforms and types of modulation (high vs. low PAPR), different power control dynamics, frequency of operation and different radio bandwidths (narrow vs. wideband operation). In addition to this, the power consumption becomes a very important issue. Different architectures of multi-radio transmitters have been recently proposed and a lot of research efforts have been put particularly in the reconfigurability of RF components and high power efficiency [1], [6]. Moreover, as the frequency spectrum utilization reveals to be very poor [2], [3], [4] a new paradigm in wireless communications based on the spectrum aware cognitive radio becomes widely discussed. In order to adapt to the actual transmission request and the radio spectrum accessibility, the cognitive radio concept will require very high flexibility of RF elements [5].

One of the most challenging components to design in the flexible multi-band RF front-end is undoubtedly the wideband reconfigurable LO (local oscillator). The LO frequency is used to convert the signal from the baseband to the RF and vice versa and it frequently determines overall performance of the system. In the ideal case, only one LO should be able to deliver the appropriate frequency (in quadrature) with respect to requirements of relevant communication standard and common performance metrics such as phase noise, frequency settling time, spurious output, frequency raster etc. Beside the FDD (Frequency Division Duplex) based communication standards, which require simultaneous LO operation in uplink and downlink directions, an additional LO is needed in cases, where the simultaneous voice and data communication is required (e.g. GSM/3G voice along with Bluetooth/WiFi/WiMAX data). Therefore, a frequency plan that suits to the simultaneous radio operation needs to be considered. This brief report presents a CP (Charge Pump) PLL based frequency synthesizer

that combines two different modes of operation (fractional-N and integer-N) accompanied by the loop filter switching technique. More details about this approach can be found in [5].

2. Overview and results carried out during the year 2009

After detailed investigation of requirements for multi-radio frequency synthesizer [7] and study of different techniques for frequency synthesis, a hybrid PLL based synthesizer has been proposed. The overall architecture is shown in Fig. 1. To ensure simultaneous voice and data communications, the multiband synthesizer has been designed for each service separately. The upper LO dedicated to the voice link employs an integer-N PLL, which satisfies GSM/WCDMA LO requirements, while the second LO dedicated to data communication employs a fast hybrid fractional-N/integer-N PLL with switched loop filter. Both PLL circuits use the same 20 MHz crystal reference and moreover, use an identical but separate wideband VCO with capacitor bank operating in the band of 3.2 to 4.2 GHz. This frequency of operation has been chosen due to the use of divide-by-2 prescalers for quadrature signal generation. This approach to the quadrature signal generation offers an accurate I and Q signals with minimal mismatch and a very low power consumption and savings in terms of the die area compared to quadrature VCO design. An important feature is that the VCO frequency is separated from the desired RF frequency, which should prevent pulling of the VCO frequency by the RF output signal of the transmitter [5]. A quadrature balanced mixer has been considered for the quadrature signal generation of 802.11a/b/g, WiMAX (802.16e) and Bluetooth standards. The frequency plan has been chosen according to particular requirements given by multiple standards (RF frequency and channel resolution).

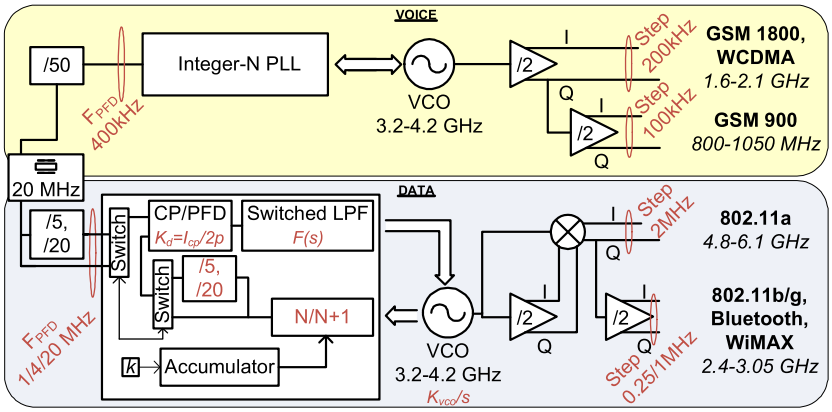

Fig.1: Overall scheme of the proposed multiband frequency synthesizer.

2.1. Hybrid mode of operation

Due to very high settling time requirements given by the Bluetooth and WLAN/WiMAX standards (< 50μs), the above mentioned technique has been adopted for the branch of the data carrier generation, as depicted in Fig. 1. Since the fractional-N PLL mode is employed only during the frequency transition, the fractional spurious suppression circuitry commonly needed in fractional-N PLL's does not need to be implemented, which results in a significant power supply and area savings.

The hybrid integer-N/fractional-N PLL has been designed to deliver frequency raster of the WiMAX standard (250 kHz). Moreover, the required maximum integrated phase noise of 1° rms has been considered in the loop bandwidth optimization. The frequency applied to the PFD reference input varies between three values. Direct 20 MHz reference is applied to the PFD during the fractional-N speed-up mode. The additional dividers are disabled during this phase. In this mode, various bandwidths of the PLL can be set (resulting wide loop bandwidth

is a multiplicative of the reference loop bandwidth by the factor α). The reference loop bandwidth here considered corresponds to the integer-N PLL loop bandwidth during the settled mode and equals to 20 kHz. 20 kHz has been chosen as the optimal value in order to satisfy requirements in terms of the phase jitter imposed by the Mobile WiMAX, which is to be less than 1° rms. This value is critical since the integration frequency can start at about 1/20 of the tone spacing (modulated carrier spacing) and ends up at ½ of the channel bandwidth [13]. Therefore, the integration of the phase noise can start at as low as few hundred Hertz, depending on the FFT size of the OFDM and considered channel bandwidth.

Frequency dividers by 20 and by 5 are employed in the hybrid architecture only during the settled integer-N mode, after the frequency transition. The alternative frequency division enables a dual frequency step of the synthesizer, namely step of 1 and 4 MHz, depending on the choice of the communication standard. 1 MHz step of the PLL applied to the frequency mixture/division circuitry (see Fig. 1) corresponds to the frequency step of 250 kHz required by the WiMAX standard. In order to keep the crossover frequency and the phase margin constant for both integer-N configurations, the charge pump current I_{cp} has to be increased by factor of 4 in the 1 MHz step mode as the division N is increased by the same factor; (I_{cp}=314 μA ⇒ I_{cp}=1.25 mA). This measure enables a simple integer-N PLL reconfiguration without the need of modifying the loop filter components.

To ensure the loop stability during the fractional-N wideband high-speed mode, the PLL parameters I_{cp}, N and R_2 have to be adjusted according to the required bandwidth enlargement factor α, as presented in Tab. 1. $I_{cp(/5)}$ and $I_{cp(/20)}$ represent the resulting charge pump current in the multi-wideband mode comparatively to the charge pump current I_{cp} (charge pump current during the settled integer-N mode). $I_{cp(/5)}$ and $I_{cp(/20)}$ correspond to the required charge pump current for frequency steps of 4 and 1 MHz respectively. The multi-band open loop performance is depicted in Fig. 2 for four wideband configurations (α=2, 4, 6, 8) as well as for the integer-N set-up. Corresponding settling time performance for different factors α is depicted in Fig. 3. Time to lock to 10 Hz frequency error is presented in Tab. 1.

Factor α	**$I_{cp(/5)}$; $I_{cp(/20)}$**	**$R_{(/5)}$ & $R_{(/20)}$**	**Settling Time (to 10 Hz) [μs]**
2	4/5 I_{cp}; 4/20 I_{cp}	R_2/2	168
4	16/5 I_{cp}; 16/20 I_{cp}	R_2/4	61
6	36/5 I_{cp}; 36/20 I_{cp}	R_2/6	38
8	64/5 I_{cp}; 64/20 I_{cp}	R_2/8	28

Tab. 1. PLL parameters as a function of the factor α [5]

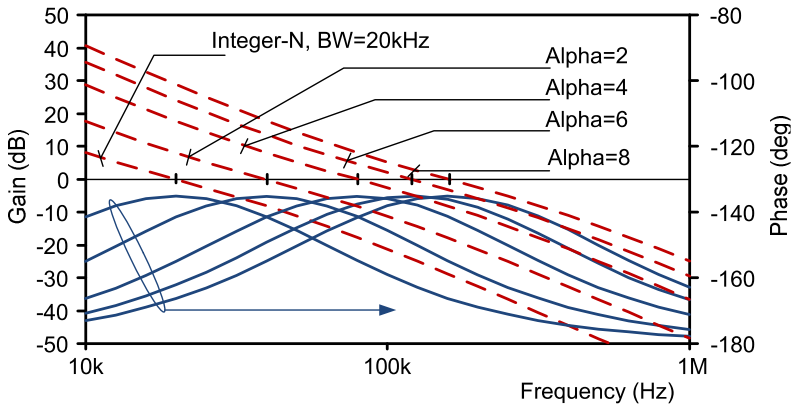

Fig.2: Loop gain (red dashed line) and phase of proposed PLL synthesizer for different factors α. The maximum loop bandwidth 160 kHz is at α =8 [5].

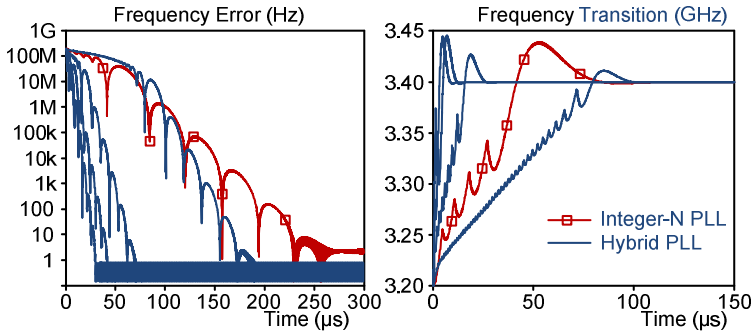

Fig.3: Settling time performance of proposed hybrid synthesizer for different factors α. First figure shows the frequency error in reference to the frequency 3.4 GHz. [5].

3. Perspectives and recommendations for the future research

A brief introduction of the hybrid PLL approach for the frequency synthesis has been given. This promising technique may provide several advantages over the single integer or fractional PLL, namely in terms of high degree of reconfigurability and circuit complexity. In the following research, certain issues such as the switching protocol optimization and the influence of real PLL's components will be investigated.

Acknowledgement

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