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Summary :
4H-SiC asymmetrical gate turn-off (GTO) thyristors have been simulated using the finite element code MEDICI™. The goal of these numerical simulations is a performance analysis of GTO SiC-thyristors having a planar anode. One advantage over the conventional etched anode structure is the avoidance of lithography related problems appearing in the recessed gate groove. From a performance point of view the planar anode and gate geometries allow smaller distances and hence lower specific on-resistance as well as a higher dI/dt. After a detailed description of simulation tool, models used and their parameters, this paper focuses on the dV/dt sensitivity, on the blocking voltage attainable with JTE and on the influence of the geometry on the switching-on. Finally the results will be compared to recessed gate GTO thyristors on SiC.

Introduction :
Like others [1, 2] we have been developing etched gate turn-off (GTO) thyristors on 4H-SiC [3, 4], featuring a recessed gate structure. The electrical results are very encouraging for future high power semiconducting devices based on silicon carbide (SiC). For the etched thyristor, the anode and the gate are not in the same plane (cf. figure n°1). So, in particular for interdigitated structures with small dimensions, it is a problem to realize contacts in the gate groove. The goal of this paper is to give a performance analysis of GTO SiC-thyristors with the anode and the gate on the same plane. The technological solution is to develop the p^+ level of the anode by ion implantation (cf. figure n°1). In the following, this type of thyristor structure is referred to as "planar" thyristor. In figure 1 and 2, we can see the device termination is realized by mesa and an additional junction termination extension (JTE). After a detailed description of the models applied and the parameters entered when using the finite element code MEDICI™, we show results obtained by the numerical simulations. Subsequently, a second part describes the effectiveness of the peripheral protection and gives the parameters to be used for the technological realization.

About the simulator MEDICI™ :
MEDICI™ is a finite element code solving at each mesh node the continuity equations and the Poisson's equation. A model is used for the mobility and is described by equation n°1.

$$\mu_{n,p}(x,y)=MUn,p.MIN+\frac{MUn,p.MAX\left(\frac{T}{300}\right)^{MUn,p}-MUn,p.MIN}{1+\left(\frac{T}{300}\right)^{Xln,p}\left(\frac{N_{total}(x,y)}{NREFn,p}\right)^{ALPHAn,p}} \quad (1)$$

T : temperature [K]
$N_{total}(x,y)$: level doping [cm^{-3}]
In reverse bias, another model is used for the high electrical field with a specified saturation velocity equals to 2×10^7 V·cm^{-1}. The mobility at high electrical field is modelled by the equation n° 2.

$$\mu_{n,p}(x,y)=\frac{mun,p0}{\left[1+\left(\frac{mun,p0.E_p(x,y)}{v_{satn,p}}\right)^{Betan,p}\right]^{\frac{1}{Betan,p}}} \quad (2)$$

$E_p(x,y)$: electrical field module perpendicular to the conduction path
$V_{satn,p}$: saturation velocity is 2×10^7 V·cm^{-1}
The carrier lifetime depends on the doping level and its expression is:

$$\tau_{n,p}(x,y)=\frac{TAUn,p0}{\left(1+\frac{N(x,y)}{NSRHn,p}\right)} \quad (3)$$

For the impact ionisation, the model is described by the equation n°4.

$$\alpha_{n,p}(x,y)=n,p.IONIZA.e^{\left(-\frac{E_{cn,p}}{E_{Para}(x,y)}\right)} \quad (4)$$

$E_{Para}(x,y)$: electrical field module parallel to the conduction.

We used the Schokley, Read, Hall statistic to calculate the generation and recombination of the carriers.

The parameters used in the different models and their values applied are listed in table n°1.

TABLE 1 : Parameter values used for different models

Name	Value
MUn.MAX	947 $cm^2.V^{-1}.s^{-1}$
MUn.MIN	0
NUn	-1,962
XIn	0
ALPHAn	0.61
NREFn	1.94 10^{17} cm^{-3}
MUp.MAX	124[$cm^2.V^{-1}.s^{-1}$
MUp.MIN	15.9 $cm^2.V^{-1}.s^{-1}$
NUp	-1.434
XIp	0
ALPHAp	0.34
NREFp	1.76 10^{19} cm^{-3}
MUn0	500 $cm^2.V^{-1}.s^{-1}$
MUp0	167 $cm^2.V^{-1}.s^{-1}$
TAUn0	500 ns
TAUp0	100 ns
NSRHn	10^{30} cm^{-3}
NSRHp	10^{30} cm^{-3}
n.IONIZA	4,08 10^5 cm^{-1}
E_{cn}	1,67 10^7 $V.cm^{-1}$
p.IONIZA	1,63 10^7 cm^{-1}
E_{cp}	1,67 10^7 $V.cm^{-1}$

Thyristor structures:

For the first thyristors realized by V. Zorngiebel et al. [3], the gate was obtained by etching a part of the P^+ epilayer (c.f. fig. n°1.). So the gate and the anode are not on the same plane, making the realization of the gate contact in the groove difficult, especially for highly interdigitated structures. To avoid this problem, the anode could be realized by ion implantation (cf. fig. n°2). The planar thyristor can be realized using an N^+ wafer and only 3 epilayers (PP^-N).

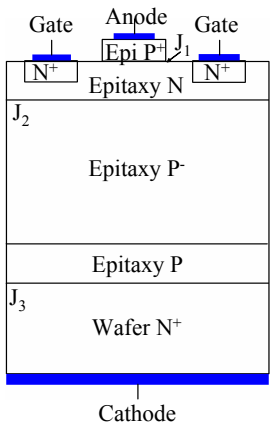

Fig. 1 : Schematic of etched thyristor structure

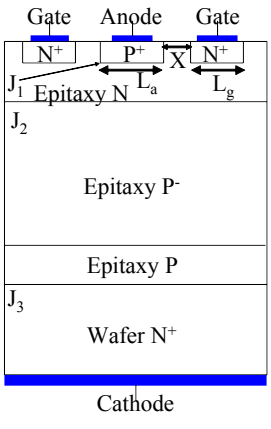

Fig. 2 : Schematic of planar thyristor structure

Simulation results:

Before dealing with the forward blocking state we present simulation results revealing the conditions necessary to switch-on the planar thyristor.

Switch on conditions:

If a positive anode cathode voltage V_{AK} = E (cf. Fig. 3) is applied, the two outer junctions are forward biased (J_1 and J_3), and junction J_2 is reverse biased. This state is called the forward blocking state. To switch on the thyristor, a negative gate current must be injected. A resistance R is used to limit the cathode current in the simulation circuit shown in figure n°3.

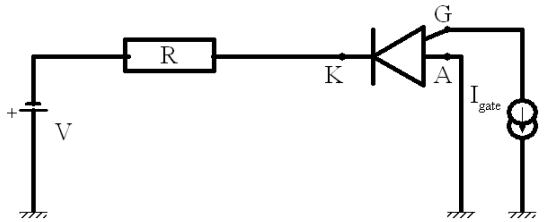

Fig. 3 : Electrical circuit

First, simulations were carried out to see the effect of the $\frac{dV}{dt}$. Figure n°4 shows to which extend the breakover voltage depends on the $\frac{dV}{dt}$. If the $\frac{dV}{dt}$ increases the breakover voltage decreases. At low voltages, junction J_2 is reverse biased. The

junction capacitance was estimated by frequency simulations to be around $C = 10^{-15}\ F \cdot m^{-1}$. For $\frac{dV}{dt} = 10\ V \cdot \mu s^{-1}$ the product $C \cdot \frac{dV}{dt}$ equals to $10^{-7}\ A \cdot m^{-1}$. So it is sufficient to switch the thyristor to on-state

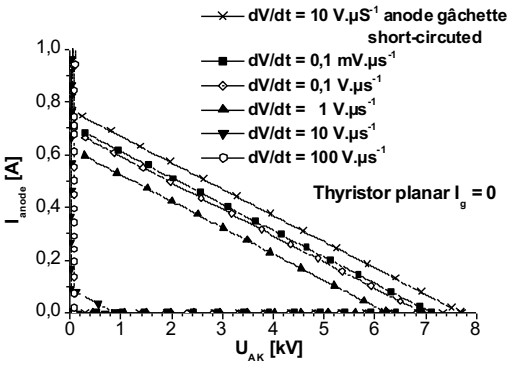

Fig. 4 : Electrical characteristics of the planar thyristor for different $\frac{dV}{dt}$

In summary, these simulations show that the dV/dt must be lower than 0.1 $V.\mu s^{-1}$, to avoid dV/dt related switch-on of the thyristor.

In order to reveal the influence of the anode length on the turn-on time the same simulation circuit is used with a 4 kΩ resistance and a 300 V voltage source. The gate current is a 24 ms pulse. Its maximal value equals to 0.1 mA. The surface of the structure is constant.

The simulation shows that the switching time decreases if the anode length decreases (see Fig. 5).

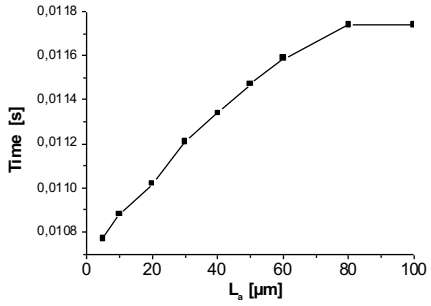

Fig. 5 : Switching time versus L_a

Other simulations with varying gate contact width or gate-anode distance L_G (figure n°2) revealed no change of the switching time for the planar thyristor.

Forward blocking state :

The purpose of the following simulations is to investigate device terminations supporting the blocking junction n°2. For reasons of calculation time needed, the simulation structure used is based on a simple NP^-P diode structure which is shown in figure n°6.

The doping level and the thickness of the P^- epilayer were determined by semi infinite junction simulations (one-dimensional NP^-P structure). The breakdown voltage obtained by simulation is 7.9 kV for a 50 µm epilayer with a doping level equal to $1 \times 10^{15}\ cm^{-3}$.

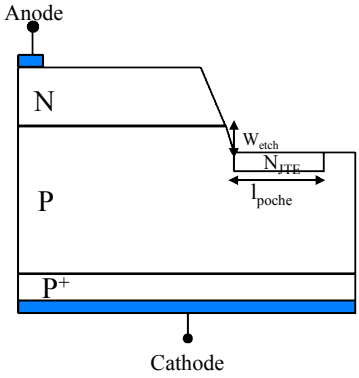

Fig. 6 : NP^-P structure diode

Two types of device terminations have been developed : mesa (cf. figure n°6) and a combination between mesa and JTE (Junction Termination Extension). For the mesa protection, only one parameter, the etching depth (W_{etch}) is be optimized. In figure n°7, the breakdown voltage versus W_{etch} is represented. Note that W_{etch} is the relative etch depth with respect to J_2.

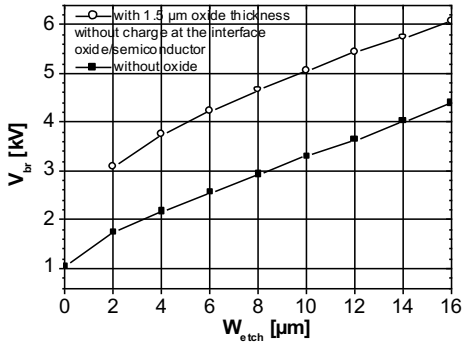

Fig. 7 : Breakdown voltage versus mesa etching depth

To obtain an efficiency of 50 % or more for the mesa termination (4 kV), the etching depth must be greater than 14 µm. With an RIE process etched with typical speed 100 nm/min, the time would be very long (140 min). Therefore, simulations are performed with an implanted JTE region. The results are shown in figure n°8. The simulations are realized for 0.4 µm etching depth. The breakdown voltage depends on the JTE length but for a length greater than 150 µm, the voltage does not change. As can be seen, the attainable forward blocking voltage is maximal in a small range between 9×10^{12} cm^{-2} and 1×10^{13} cm^{-2}.

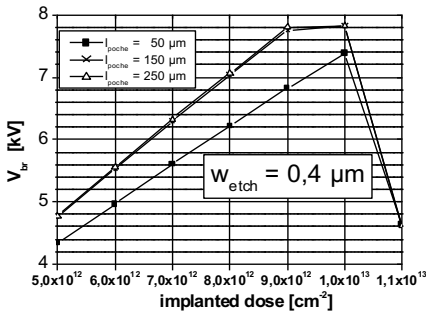

Fig. 8 : Breakdown voltage versus implanted dose in JTE for different lengths

Therefore, it is very important to accurately adjust the implanted dose. Furthermore, because of the sensitivity of the forward blocking voltage on the doping concentration, it is very important to know the exact number of implanted atoms being electrically activated. By comparing CV with SIMS data, Fig 9 indicates 80 % activation of a nitrogen implanted and annealed (1700°C / 30 mn) region on 4H-SiC.

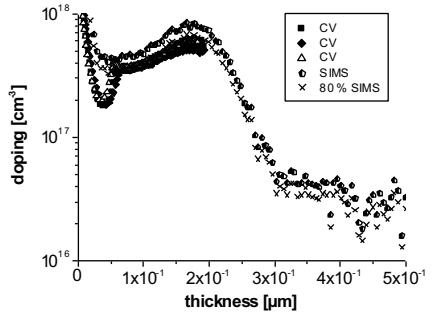

Fig. 9 : N type doping versus the thickness

Conclusion:

Based on numerical simulations using MEDICI™, a planar anode SiC-thyristor was simulated with the aim to improve the trade-off between switching behaviour and blocking features. Voltage transient related turn-on is expected for dV/dt rates in excess of $0.1\ V\cdot\mu s^{-1}$. While the advantageous planar structure gains from the reduction of the anode length in terms of a reduced turn-on time, the anode gate distance and gate width have no influence on the switching speed.

Using a simple mesa termination efforts an etching depth of more than 14 µm to guarantee 50 % of the theoretical blocking voltage. JTE, on the other hand, efforts a proper adjustment of the electrically active dopants. The simulations made indicate the optimal dose being in the range of 0.9 to 1×10^{13} cm^{-2}. Having only 80 % electrical activation the dose used in the impantation process has to be 1.12 to 1.25×10^{13} cm^{-2}.

Reference :

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