Robust Saturated Control for Low-Power Circuits

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***Abstract*—An important issue in the trends of miniaturization of Systems on Chips (SoCs) is to obtain a high energy efficiency. This can be reached by Dynamic Voltage Scaling (DVS) architectures as the novel discrete Vdd-Hopping circuit. Generally, this kind of systems present parameter uncertainties and delays. Likewise, current peaks and energy dissipation must be reduced.**

In this paper, an optimal and robust saturated control law is proposed for this Vdd-Hopping circuit via Lyapunov-Krasovskii theory that ensures asymptotic stability as well as system robustness with respect to delay presence and parameter uncertainties. The closed-loop system presents a regional stabilization due to the actuator saturation. An estimation of an attraction domain is provided. This controller also limites the current peaks and it provides an energy-aware performance. The advantages achieved with this controller are shown in simulation.

I. Introduction

The continuous miniaturization of Systems on Chips (SoCs) is possible from emerging studies about energy saving in Very-Large-Scale Integration (VLSI), especially in portable electronics devices. Dynamic Voltage Scaling (DVS) [1] is a powerful method to reduce the power consumption in micro-circuits and in nano-circuits. The principle of DVS approach is to adapt levels of supply voltage for reducing power consumption. This kind of architectures adapt the core voltage, v_c, of the cluster at the minimum performance level required by the process activity [2]. Generally, a DVS circuit is implemented by integrated dynamic DC-DC converters [3], [4], [5]. However, these DC-DC converters can present some limitations in fine grain. This is the reason why new discrete circuits with reduced size have been developed based on DVS [6], [7], as Vdd-Hopping circuit [8]. This structure allows changing the drain supply voltage level (V_{dd}) in nano-circuits in high speed.

The main control problem for Vdd-Hopping circuit is the adaptation for various loading conditions, achieving high efficiency over a wide load-current range, what is critical for extended battery life. Likewise, other control objectives are to provide a correct and reliable operation during the switches transitions, i.e., small current peaks, faster transient periods, system stability and robustness with respect to delays and parameter uncertainties. Indeed, Vdd-Hopping circuits implemented in these SoC structures present delays at the input and output of its control block [9]. The control block input delay is required to ensure that the system is synchronized with the cluster clock. In the same way, there is a control block output delay associated with computational issues. Moreover, the presence of parameter uncertainties can generate a non-desirable performance and lack of reliability of the system. Other additional and relevant issue is to limit current peaks and energy consumption. In summary, delay presence, parameter uncertainties, current peaks and energy consumption must be considered in the design of the controller.

In this paper, an optimal and robust saturated control law for the Vdd-hopping circuit is proposed in discrete time. This controller limites high current peaks. It provides an efficient tracking capability to handle two voltage levels required by the cluster. As a side effect, it also has high energy-efficiency, achieving fast transient periods. The system is rewritten into a suitable state-space representation to formulate an optimal and robust problem that can be solved by using Lyapunov-Krasovskii theory [10], [11]. In this process, the saturation in the controller is considered [12], [13]. The designed controller guarantees asymptotic stability as well as robustness of the system with respect to delays and uncertain parameters. The problem is expressed in terms of Linear Matrix Inequalities (LMIs). Likewise, an attraction domain is estimated in such a way that a regional stabilization for the saturated control is guaranteed. The robustness properties of the closed-loop system are tested by some simulations.

An evaluation and comparison of this controller with respect to an 'intuitive' controller presented in [6] is performed.

The rest of this work is organized as follows: in Section II, the error equation of the Vdd-hopping system is presented as well as the proposed control law. The robustness and optimization problem statement is presented in Section III and in Section IV, a control design is developed. The control gains are computed in Section V, being tested by simulations in Section VI. A comparison of this controller is performed in Section VII. The work closes with a section of conclusions.

Notation. For a given $x \in \mathcal{R}$,

$$\mathrm{sat}_m^M(x) \triangleq \begin{cases} M & if \quad x > M \\ x & if \quad m \leq x \leq M \\ m & if \quad x < m. \end{cases}$$

and round(x) is the nearest integer to x. $\Delta x \triangleq x^+ - x^-$

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is the value of x in two consecutive sampling time. For a given set $\mathcal{S}$, $\mathcal{C}o(\mathcal{S})$ denotes the convex hull of $\mathcal{S}$.

II. Error equation of the Vdd-Hopping circuit

In [8] a discrete circuit that handles two-voltage levels with a Vdd-Hopping technique accomplishing a DVS architecture was presented.

The Vdd-Hopping circuit is constituted by: a high voltages supply, V_h; a low voltage supply, V_l; a group of PMOS transistors connected in parallel between the V_h and the core voltage, v_c, and a PMOS transistor that connects the V_l to v_c when the low voltage level is the steady-state. This reduces the dissipated energy when the unit running is at low speed. The group of PMOS transistors connected in parallel allow evolving the output voltage from a low voltage level to a high voltage level (rising transient period) and from a high voltage level to a low voltage level (falling transient period). The steady state must correspond to a high voltage level or a low voltage level. For simplicity, the low voltage supply, V_l, as well as its PMOS transistor of connection with v_c are disregarded for control design purposes. The main objective is to ensure that v_c achieves the two voltage levels by switching the PMOS transistors. The sketch of this circuit is shown in Fig. 1. In this configuration, at least, one transistor must always be switched on.

The load model taken in this work is an impedance which depends on the clock frequency, f_{clk}, and sometimes, also on v_c [14]. It is composed of a current supply, I_{leak}, a capacitance, C, and a dynamic resistance, $R_L(f_{clk}, v_c)$, representing the dynamic and short-circuit consumption. I_{leak} is assumed constant.

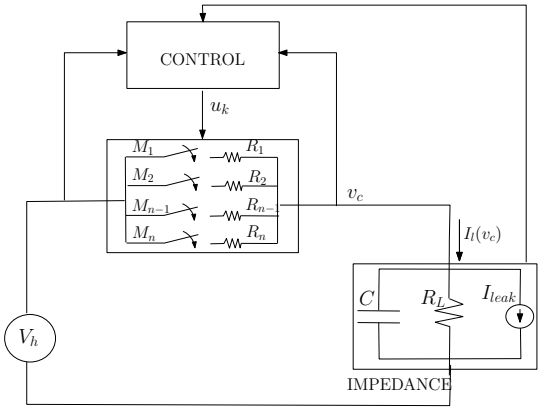

Fig. 1: Vdd-hopping, voltage supply and load.

Assumption 1: PMOS transistors are modeled as ideal resistors, R_0, when they are switched on and, as resistors with infinite resistance when they are switched off. They are considered to have the same electrical characteristic.

In the steady state, the maximum and minimum voltage are $V_h - \Delta_h$ and $V_l - \Delta_l$, respectively. $\Delta_h, \Delta_l \in \mathbb{R}$ depend on several factors and are difficult to estimate. These variables catch the PMOS model errors, current variations, supply voltage and the resistive losses through the PMOS transistors switched on.

Assumption 2: Δ_h, Δ_l are small with respect to v_c, and they do not change the system stability properties.

The voltage loop equation yields the relationship

$$I_l(v_c) = \frac{V_h - v_c}{R_{u_k}}, \tag{1}$$

where $R_{u_k} \triangleq \frac{R_0}{u_k}$, being u_k the number of transistors switched on, thus, $u_k \in \mathcal{U} = \{1, 2, ..N\}$ and it is the control variable.

The discrete Vdd-hopping circuit is connected to a load that can be modeled as an impedance depending on the core voltage, v_c. In this work, the load model presented in [14] is employed:

$$I_l(v_c) = \frac{v_c}{R_L} + I_{leak} + C\frac{dv_c}{dt} \tag{2}$$

Consider $e_k \triangleq v_r - v_{ck}$ where v_r is a constant voltage reference and v_{ck} is the sampling core voltage. Now, from Eqs. (1), (2), the approximate discrete-time voltage error equation is

$$e_{k+1} = (1 - T_s\beta)e_k + T_s b(v_r - V_h)u_k + T_s(\beta v_r + \delta - b u_k e_k), \tag{3}$$

where $\beta \triangleq \frac{1}{R_L C} > 0$, $\delta \triangleq \frac{I_{leak}}{C} > 0$ and $b \triangleq \frac{1}{R_0 C} > 0$. T_s must be less or equal to the smaller $\frac{1}{f_{clk}}$. The approximate time-discretization (3) is performed by using the forward Euler method, by assuming that the sampling time is small enough to the system evolution.

A proposed controller for this system is based on a linear controller [15]:

$$u_k = \text{sat}_1^N \left\{ u_{k-1} + \text{round}\left(K_1 \Delta e_k + K_2 e_{k-1}\right) \right\}. \tag{4}$$

Control (4) presents a simple enough structure such that it requires a small space in the silicon. The saturation function is due to the control signal constraint mentioned before. The control objective is to achieve a set-point reference signal. An approximate control structure for the Vdd-Hopping circuit that manages the current peaks is patent pending under the name of ENergy-AwaRe Control (ENARC) [16].

III. Problem statement

Here, the problem statement is formulated rewriting the closed-loop system of (3) in a state-space form considering delays, uncertain parameters and current peak reduction.

Figure 2 shows the Vdd-Hopping circuit including delays. The system has a h_2-sample-period delay at the control block input and a h_1-sample-period delay at the control block output, as mentioned before.

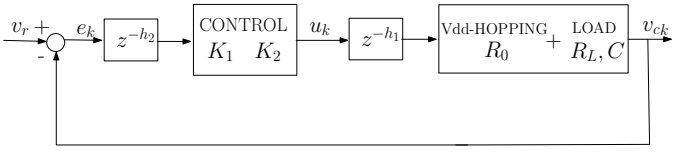

Fig. 2: Block diagram of the circuit control system.

The open-loop system is

$$e_{k+1} = (1 - T_s\beta)e_k + T_s b(v_r - V_h)u_{k-h_1} + T_s(\beta v_r + \delta) - bT_s u_{k-h_1} e_k, \quad (5)$$

and the considered Control (4) is

$$u_{k-h_1} = \text{sat}_1^N\{u_{k-1-h_1} + \text{round}(Kx_{k-h})\}, \quad (6)$$

where $h \triangleq h_1 + h_2$, $x_{k-h} = [e_{k-h} \quad e_{k-1-h}]^T$ and $K = [\bar{K}_1 \quad \bar{K}_2]$, where $\bar{K}_1 \triangleq K_1$ and $\bar{K}_2 \triangleq K_2 - K_1$.

For simplicity, the control variable u_k is considered a real number. Thus,

$$\begin{aligned} u_{k-h_1} &= \text{sat}_1^N\{u_{k-1-h_1} + Kx_{k-h}\} \\ &= \text{sat}_1^N\{u_{k-1-h_1} + \Delta u_{k-h_1}\}, \end{aligned} \quad (7)$$

A rigorous analysis should take $u_k \in \mathbb{Z}$. Note that if Δu_{k-h_1} is bounded above, then, from Eq. (1), the maximum current peaks ($\Delta u_{k-h_1} = \frac{R_0}{V_h - v_c}\Delta I_{l_{max}}$, [17]) are limited. For this purpose, the quadratic cost functions

$$J_k = \sum_{k=0}^{\infty}(x_k^T \mathcal{Q} x_k + \Delta u_{k-h_1}^T \mathcal{R} \Delta u_{k-h_1}) \quad (8)$$

must be minimized. Note that the positiveness of the matrices $\mathcal{Q}$ and $\mathcal{R}$ implies that J_k is strictly positive.

On the other hand, the parameters R_L, R_0 and C that define β, b and δ can be considered uncertain. Each uncertain parameter is within an uncertainty interval, whose corresponding extremes are

- $C \in [C^m, C^M]$,
- $R_L \in [R_L^m, R_L^M]$,
- $R_0 \in [R_0^m, R_0^M]$.

Remark 1: The asymptotic stability of system (5) is guaranteed in a point within an uncertainty interval for the low level voltage, $\mathcal{I}_l$, and within an uncertainty interval for the high level voltage, $\mathcal{I}_h$, bounded by

$$\mathcal{I}_l \triangleq \left[\frac{R_L^m(u_{k_l}V_h - R_0^M I_{leak})}{u_{k_l}R_L^m + R_0^M}, \quad \frac{R_L^m(u_{k_l}V_h - R_0^m I_{leak})}{u_{k_l}R_L^m + R_0^m}\right] \quad (9)$$

$$\mathcal{I}_h \triangleq \left[\frac{R_L^M(u_{k_h}V_h - R_0^M I_{leak})}{u_{k_h}R_L^M + R_0^M}, \quad \frac{R_L^M(u_{k_h}V_h - R_0^m I_{leak})}{u_{k_h}R_L^M + R_0^m}\right] \quad (10)$$

u_{k_l} and u_{k_h} are the lower-bound and the upper-bound of u_k, respectively.

Consequently, the main objective is to design the optimal gain K in such a way that Control (6) is robust with respect to delays as well as parameter uncertainties. Likewise, this optimal gain K must guarantee asymptotic stability and minimum current peaks for the known constant delays, h_1 and h_2.

A. Alternative representation for the saturated control (7) *and the error equation* (5)

Firstly, some lemmas are given to rewrite the saturated control (7) and an alternative form.

Define $\chi_{k-h} \triangleq \begin{bmatrix} u_{k-1-h_1} \\ x_{k-h} \end{bmatrix}$. Note, from Eq.(5), u_{k-1-h_1} directly depends on $x_k = [e_k, \quad e_{k-1}]^T$.

Lemma 1: [18], let $K, G \in \mathbb{R}^{1\times 2}$ be given. For all, $\chi_{k-h} \in \mathbb{R}^{3\times 1}$, if $\chi_{k-h} \in \{\chi_{k-h} \in \mathbb{R}^{1\times 3} : [1 \quad G]\chi_{k-h} \in [1 \quad N]\}$, then

$$\text{sat}_1^N\{[1 \quad G]\chi_{k-h}\} \in \mathcal{C}o\{[1 \quad K]\chi_{k-h}, \quad [1 \quad G]\chi_{k-h}\}.$$

□

Lemma 2: Assume that there exists $G \in \mathbb{R}^{1\times 2}$, $c > 0$ and $\Psi \triangleq \text{diag}\{\rho, P_1\}$, where $P_1{}^{\dagger} > 0 \in \mathbb{R}^2$, $\rho > 0 \in \mathbb{R}^1$ such that for any $\chi_{k-h} \in \mathfrak{X}$, where

$$\mathfrak{X} = \left\{\chi_{k-h} : \chi_{k-h}^T \Psi \chi_{k-h} \leq c^{-1}\right\}, \quad (11)$$

then, $1 < u_{k-1-h_1} + Gx_{k-h} < N$, and Control (7) admits the following representation

$$\begin{aligned} u_{k-h_1} &= [\alpha_k(u_{k-1-h_1} + Kx_{k-h}) \\ &\quad + (1-\alpha_k)(u_{k-1-h_1} + Gx_{k-h})] \\ &= [u_{k-1-h_1} + \alpha_k K x_{k-h} + (1-\alpha_k)Gx_{k-h})] \\ &= [u_{k-1-h_1} + \bar{u}_{k-h}], \end{aligned}$$

where $\bar{u}_{k-h} \triangleq (\alpha_k K + (1-\alpha_k)G)x_{k-h}$ with $\alpha_k \in [0,1]$, for all $k > 0$. □

Then, Eq. (5) can be rewritten

$$e_{k+1} = (1 - T_s\beta)e_k + T_s b(v_r - V_h)(u_{k-1-h_1} + \bar{u}_{k-h}) + T_s(\beta v_r + \delta) - bT_s u_{k-h_1} e_k. \quad (12)$$

B. State-space representation

The saturated control law and error equation, as redefined before, allow to system (5) rewrite it in a state-space form.

From Eq. (5) ,

$$u_{k-h_1} = \frac{e_{k+1} - (1 - T_s\beta)e_k - T_s(\beta v_r + \delta) + bT_s u_{k-h_1} e_k}{T_s b(v_r - V_h)},$$

and, therefore

$$u_{k-1-h_1} = \frac{e_k - (1 - T_s\beta)e_{k-1} - T_s(\beta v_r + \delta)}{T_s b(v_r - V_h)} + \frac{bT_s u_{k-1-h_1} e_{k-1}}{T_s b(v_r - V_h)},$$

which substituted in Eq. (12) gives

$$e_{k+1} = (2 - T_s\beta)e_k - (1 - T_s\beta)e_{k-1} + T_s b(v_r - V_h)\bar{u}_{k-h} - T_s b(u_{k-h_1} e_k - u_{k-1-h_1} e_{k-1}). \quad (13)$$

From Lemma 1 and 2, Eq. (13) can be rewritten in the following matrix form:

$$x_{k+1} = A(u_{k-h_1}, u_{k-1-h_1})x_k + B\bar{u}_{k-h}, \quad (14)$$

where

$$A \triangleq \begin{bmatrix} 2 - T_s\beta - T_s b u_{k-h_1} & T_s\beta - 1 + T_s b u_{k-1-h_1} \\ 1 & 0 \end{bmatrix},$$

$$B \triangleq \begin{bmatrix} T_s b(v_r - V_h) \\ 0 \end{bmatrix}.$$

u_{k-h_1} and u_{k-1-h_1} of matrix A are treated as uncertain parameters in Section IV-D. Their values will be inside the uncertainty interval $[1, N]$.

$^{\dagger}P_1$ is a positive matrix defined to guarantee system stability.

C. Stability and optimization problem

Equation (14) can be rewritten in the following explicit closed-loop form.

$$x_{k+1} = Ax_k + B(\alpha_k K + (1-\alpha_k)G)x_{k-h}, \quad (15)$$
$$x_l = \phi_l, \quad \forall l \in [-h, 0] \quad (16)$$
$$z_k = I_2 x_k, \quad (17)$$

with $C \in [C^m, C^M]$, $R_L \in [R_L^m, R_L^M]$, $R_0 \in [R_0^m, R_0^M]$,

$$u_{k-h_1}, u_{k-1-h_1} \in [1, N] \quad (18)$$
$$\alpha_k \in [0, 1], \quad (19)$$

and where $x_k, z_k \in \mathbb{R}^2$ are the state vector and controlled output, respectively. ϕ_l is the initial condition and $h \geq 0 \in \mathbb{R}$ is a fixed and known delay.

Problem 1: The problem is to find a $\mathfrak{X}(\rho, P_1, c)$, some robust vectors G and K, such that

a) Lemma 2 holds and, hence, the closed-loop system (14) and
b) there exists a Lyapunov-Krasovskii functional $V_k > 0$, a cost function $J_k > 0$ such that $V_{k+1} - V_k + J_k$ along the solution of (15) fulfills

$$V_{k+1} - V_k + J_k < 0. \quad (20)$$

□

The solution to this problem minimizes a performance index that, among other considerations, limites high current peaks. Moreover, this solution guarantees the system stability for the time-delay system (15)–(17).

IV. Optimal robust saturated control design

A mathematical manipulation of Eq. (15) is performed via a descriptor model transformation [19]. The descriptor approach is just a variable change, which makes easier to work with Lyapunov-Krasovskii functional [20].

A. Descriptor model transformation

Equation (15) is manipulated in order to achieve the previous objectives. A descriptor model transformation is applied.

Define $y_k \triangleq x_{k+1} - x_k$, $\psi_k \triangleq \sum_{i=k-h}^{k-1} y_i$. Next, rewrite Eq. (15) in the descriptor form [19]:

$$\begin{bmatrix} x_{k+1} \\ 0 \end{bmatrix} = \begin{bmatrix} y_k + x_k \\ -y_k + Ax_k - x_k + B(\alpha_k K + (1-\alpha_k)G)x_{k-h} \end{bmatrix}$$

From $x_{k-h} = x_k - \psi_k$, this system can be compactly written as:

$$E\bar{x}_{k+1} = \bar{A}\bar{x}_k - \begin{bmatrix} 0 \\ B(\alpha_k K + (1-\alpha_k)G) \end{bmatrix} \psi_k, \quad (21)$$

where

$$\bar{A} \triangleq \begin{bmatrix} I_2 & I_2 \\ A + B(\alpha_k K + (1-\alpha_k)G) - I_2 & -I_2 \end{bmatrix},$$
$$E \triangleq \text{diag}\{I_2, 0_2\}, \quad \bar{x}_k \triangleq \begin{bmatrix} x_k \\ y_k \end{bmatrix}.$$

B. Condition for state-space representation

Condition a) of Problem 1 is satisfied, if

$$1 < u_{k-1-h_1} + Gx_{k-h} < N, \quad \forall \chi_{k-h} \in \mathfrak{X} \quad (22)$$

given in (11) is guaranteed.

Subtracting $\frac{N+1}{2}$ in inequality (22) and from [21], it is seen that, it is necessary satisfy

$$2N - 2 > N(1 + cx_{k-h}^T P_1 x_{k-h} + cu_{k-1-h}^T \rho u_{k-1-h}) - 2$$
$$> 4u_{k-1-h} + 4Gx_{k-h} - 2(N+1) \quad (23)$$

From Lemma 2, relationships (23) correspond to

$$\begin{bmatrix} 1 \\ \pm u_{k-1-h_1} \\ \pm x_{k-h}^T \end{bmatrix}^T \begin{bmatrix} 3N & -2 & -2G \\ -2 & cN\rho & 0 \\ -2G^T & 0 & cNP_1 \end{bmatrix} \begin{bmatrix} 1 \\ \pm u_{k-1-h_1} \\ \pm x_{k-h} \end{bmatrix} > 0 \quad (24)$$

This inequality is satisfied if

$$\Lambda \triangleq \begin{bmatrix} c & -2 & -2Y \\ -2 & \rho 3N^2 & 0 \\ -2Y^T & 0 & 3N^2 \bar{P}_1 \end{bmatrix} > 0 \quad (25)$$

Note that this LMI is equivalent to (24) by means of employing the Schur's complement, defining $Y \triangleq GQ_1$ with $Q_1 \in \mathbb{R}^2$ which is Hermitian, applying $\bar{P}_1 = Q_1 P_1 Q_1$ and pre- and post-multiplying by $diag\{1, 1, Q_1\}$.

C. Stabilization and optimization

For simplicity, assume here a nominal value of: α_k, u_{k-h_1} and u_{k-1-h_1}. In next subsection (18)–(19) will be considered as uncertain inside a convex polytope. Condition b) of Problem 1 can be formulated in terms of Linear Matrix Inequalties (LMIs) [10]. Fulfillment of condition (20) is looked for.

Define $P \triangleq \begin{bmatrix} P_1 & P_2 \\ P_2 & 0 \end{bmatrix}$, being P_2 Hermitian. Consider as Lyapunov-Krasovskii candidate

$$V_k = V_{1,k} + V_{2,k} + V_{3,k}, \quad (26)$$

being

$$V_{1,k} = \bar{x}_k^T EPE\bar{x}_k, \quad P_1 > 0 \quad (27)$$
$$V_{2,k} = \sum_{n=1}^{h} \sum_{i=k-n}^{k-1} y_i^T R y_i, \quad R > 0 \quad (28)$$
$$V_{3,k} = \sum_{i=k-h}^{k-1} x_i^T S x_i, \quad S > 0, \quad (29)$$

where $V_{1,k}$ guarantees asymptotic stability of system (21) without delays. Delay-dependent as well as delay-independent criteria are considered in $V_{2,k}$ and $V_{3,k}$, respectively [10], [11].

Next, a sufficient condition for asymptotic stability and minimization of a performance index that, among other considerations, limites high current peaks, is derived.

Theorem 1: Consider system (15)–(17) with nominal value of: α_k, u_{k-h_1} and u_{k-1-h_1}. $h > 0 \in \mathbb{N}$ is a

known constant delay and $K, G \in \mathbb{R}^{1\times 2}$. If there exist $\mathcal{Q}, \mathcal{R}, S, R, P_1 > 0 \in \mathbb{R}^2$ and $c, \mu > 0$ such that

$$\begin{aligned}
\min_K \quad & \mu \\
& P_1 > 0 && (30)\\
& \Gamma < 0 && (31)\\
& \begin{bmatrix} -\mu I_2 & 0_2 & I_2 & 0_2 \\ * & -\mu I_2 & 0_2 & I_2 \\ * & * & -P_1 - S & S \\ * & * & * & -hR - S \end{bmatrix} < 0, && (32)\\
& \Lambda > 0 && (33)
\end{aligned}$$

where Γ is defined in Eq. (34), found at the top of next page, then the equilibrium of the closed-loop system (15)–(17) is asymptotically stable and the current peaks are limited.

Proof: The goal is to satisfy $V_{k+1} - V_k + J_k < 0$ for system (21).

Lyapunov-Krasovskii method yields:

$$\begin{aligned}
& V_{1,k+1} - V_{1,k} = \bar{x}_{k+1}^T EPE\bar{x}_{k+1} - \bar{x}_k^T EPE\bar{x}_k \\
& = \left\{ \bar{x}_k^T \bar{A}^T - \psi_k^T [0 \quad \alpha_k K^T B^T + (1-\alpha_k) G^T B^T] \right\} \\
& \quad P \left\{ \bar{A}\bar{x}_k - \begin{bmatrix} 0 \\ \alpha_k BK + (1-\alpha_k) BG \end{bmatrix} \psi_k \right\} - \bar{x}_k^T EPE\bar{x}_k \\
& = \bar{x}_k^T [\bar{A}^T P \bar{A} - P_1] \bar{x}_k - \bar{x}_k^T \bar{A} P \begin{bmatrix} 0 \\ \alpha_k BK + (1-\alpha_k) BG \end{bmatrix} \psi_k \\
& - \psi_k^T [0 \quad \alpha_k K^T B^T + (1-\alpha_k) G^T B^T] P \bar{A} \bar{x}_k.
\end{aligned}$$

From (28) and Jensen Inequality [22]:

$$\begin{aligned}
V_{2,k+1} - V_{2,k} &= h y_k^T R y_k - \sum_{n=1}^{h} y_{k-n}^T R y_{k-n} \\
&\leq \bar{x}_k^T \begin{bmatrix} 0 & 0 \\ 0 & hR \end{bmatrix} \bar{x}_k - \frac{1}{h} \psi_k^T R \psi_k
\end{aligned}$$

Finally,

$$\begin{aligned}
V_{3,k+1} - V_{3,k} &= x_k^T S x_k - x_{k-h}^T S x_{k-h} \\
&= x_k^T S \psi_k + \psi_k^T S x_k - \psi_k^T S \psi_k
\end{aligned}$$

These developed expressions and Eq. (8) are applied to inequality (20), in such a way that the LMIs (31) are obtained.

On the other side, summing (20) from $n = 0$ to ∞, it is obtained

$$\sum_{k=0}^{\infty} (V_{k+1} - V_k + J_k) = V_\infty - V_0 + \sum_{k=0}^{\infty} J_k = -V_0 + \sum_{k=0}^{\infty} J_k < 0.$$

Thus, $\sum_{k=0}^{\infty} J_k < V_0 < [\bar{x}_0 \quad \psi_0] \mathcal{M} [\bar{x}_0 \quad \psi_0]^T$, where $\mathcal{M} \triangleq \begin{bmatrix} P_1 + S & -S \\ -S & hR + S \end{bmatrix}$. To minimize the trace of $\mathcal{M}$ means to minimize any $\mu > 0$, such that, $\mathcal{M} < \mu I_4$, [23]. From this inequality and applying the Schur's complement LMI (32) is obtained. ∎

D. Control design

Now, consider uncertain parameters given in Section III and (18)–(19). For this purpose, Theorem 1 is extended in the case of polytopic uncertainties.

Denote

$$\Omega \triangleq [A \quad BK \quad \alpha_k \quad u_{k-h_1} \quad u_{k-1-h_1}]$$

and assume that $\Omega \in \mathcal{C}o\{\Omega_j, \quad j = 1, ..., 64\}$, namely

$$\Omega = \sum_{j=1}^{n} \lambda_j \Omega_j, \quad \text{for} \quad \text{all}, \quad 0 \leq \lambda_j \leq 1, \quad \sum_{j=1}^{n} \lambda_j = 1$$

and being the vertices of the polytope described by $\Omega_j = [A^{(j)} \quad B^{(j)}K \quad \alpha_k^{(j)} \quad u_{k-h_1}^{(j)} \quad u_{k-1-h_1}^{(j)}]$ for $j = 1, 2, ..., 64$.

Pre- and post-multiplying LMI (31) by $Q = \text{diag}\{Q_1, Q_1, Q_1\}$ and apply the Schur' complement. Pre- and post-multiplying LMI (32) by $Q = \text{diag}\{I_2, I_2, Q_1, Q_1\}$ and taking $Q_1 = P_2^{-1} > 0$ and $\bar{P}_1 = Q_1 P_1 Q_1$, $\bar{R} = Q_1 R Q_1$, $\bar{S} = Q_1 S Q_1$, the following sufficient condition is achieved.

Theorem 2: Consider system (15)–(17) with $h \geq 0 \in \mathbb{N}$ is a known constant delay and $K, G \in \mathbb{R}^{1\times 2}$. If there exist $T, Y \in \mathbb{R}^{2\times 1}$ and $Q_1 \in \mathbb{R}^2$ with $K = TQ_1^{-1}$, $G = YQ_1^{-1}$, $\mathcal{Q}, \mathcal{R}, \bar{R}, \bar{P}_1, \bar{S} > 0 \in \mathbb{R}^2$ for $j = 1, ..., 64$ and $c, \mu > 0$ such that

$$\begin{aligned}
\min_K \quad & \mu \\
& \bar{P}_1 > 0 && (35)\\
& \bar{\Gamma}^{(j)} < 0 \quad j = 1, ..., 64, && (36)\\
& \begin{bmatrix} -\mu I_2 & 0_2 & I_2 & 0_2 \\ * & -\mu I_2 & 0_2 & I_2 \\ * & * & -Q_1 - \bar{S} & \bar{S} \\ * & * & * & -h\bar{R} - \bar{S} \end{bmatrix} < 0, && (37)\\
& \Lambda > 0 && (38)
\end{aligned}$$

being $\bar{\Gamma}^{(j)}$ defined in (39), found at the top of next page, are satisfied. Then, in the vertices j, the equilibrium is asymptotically stable as well as the current peaks are limited in the entire polytope.

Proof: This is an extension of Theorem 1 for polytopic uncertainties with some mathematical manipulations. Therefore, this theorem proof follows Theorem 1 proof. ∎

Remark 2: This robust control tuning method is conservative due to the definition of the matrix P, as well as, the attraction domain, $\mathfrak{X}$.

Corollary 1: Gain K, obtained from T and Q_1 in Theorem 2, fulfills Theorem 1 and consequently guarantees both robust stability and minimization of the current peaks for a fixed delay.

As future work an optimization of the ellipsoid $\mathfrak{X}$ will be interesting to perform.

V. Robust control result

In this section, the robust control gains for Control (7) are computed by employing the approach above. The Vdd-Hopping circuit parameters given in [8] and the load model parameter given in [14] are reported. Therefore, $N = 24$ is taken as the total number of PMOS transistors. The voltage supply is $V_h = 1.2V$. The reference signal, v_r, is a step between the low voltage level $V_{c_l} = 0.8V - \epsilon_h$ and the high voltage level $V_{c_h} = 1.2 - \epsilon_h$, being $\epsilon_h = 0.06V$ and

$$\Gamma \triangleq \begin{bmatrix} \bar{A}^T P \bar{A} - EPE + \text{diag}\{\mathcal{Q} + \Xi, hR\} & -\bar{A}^T P \begin{bmatrix} 0 \\ B(\alpha_k K + (1-\alpha_k)G) \end{bmatrix} + \begin{bmatrix} S - \Xi \\ 0 \end{bmatrix} \\ * & -\frac{1}{h}R - S + \Xi \end{bmatrix} \tag{34}$$

$$\Xi = (\alpha_k K + (1-\alpha_k)G)\mathcal{R}(\alpha_k K^T + (1-\alpha_k)G^T)$$

$$\bar{\Gamma}^{(j)} \triangleq \begin{bmatrix} \bar{\Gamma}_1^{(j)} & \bar{\Gamma}_2^{(j)} & -\alpha_k^{(j)} B^{(j)} T - (1-\alpha_k^{(j)}) B^{(j)} Y + \bar{S} & Q_1 \mathcal{Q} & \bar{\Xi}\mathcal{R} & 0 \\ * & \bar{P}_1 - 2Q_1 + h\bar{R} & 0 & 0 & 0 & 0 \\ * & * & -\frac{\bar{R}}{h} - \bar{S} & 0 & 0 & \bar{\Xi}\mathcal{R} \\ * & * & * & -\mathcal{Q} & 0 & 0 \\ * & * & * & * & -\mathcal{R} & \mathcal{R} \\ * & * & * & * & * & -\mathcal{R} \end{bmatrix}, \quad j = 1, ..., 64 \tag{39}$$

where

$$\bar{\Xi}^{(j)} \triangleq (\alpha_k^{(j)} T + (1-\alpha_k^{(j)}) Y)$$
$$\bar{\Gamma}_1^{(j)} \triangleq Q_1 {A^{(j)}}^T + A^{(j)} Q_1 - 2Q_1 + \alpha_k^{(j)} T^T {B^{(j)}}^T + (1-\alpha_k^{(j)}) Y^T {B^{(j)}}^T + \alpha_k^{(j)} B^{(j)} T + (1-\alpha_k^{(j)}) B^{(j)} Y$$
$$\bar{\Gamma}_2^{(j)} \triangleq \bar{P}_1 + Q_1 {A^{(j)}}^T - 2Q_1 + \alpha_k^{(j)} T^T {B^{(j)}}^T + (1-\alpha_k^{(j)}) Y^T {B^{(j)}}^T,$$

$\epsilon_l = 0.01$ ($V_{c_l} \approx V_l$). These parameters comes from the equilibrium of Eq. (3). The system resistances are $R_L = 27.7\Omega$ and $R_0 = 31.41\Omega$, the capacitance is $C = 9nF$, while $I_{leak} = 1.67 \cdot 10^{-3}$. The clock frequency is taken $f_{clk} = 200MHz$ and $T_s = 1.67ns$. This introduces an one-sample-period delay ($h_1 = 1$) in the control block output due to a power-performance trade-off. Likewise $h_2 = 2$, thus $h = 3$.

The uncertain parameters take the following ranges:

- transistor characteristic, R_0, from 25Ω to 38Ω,
- load dynamic resistance, R_L, from 55.53Ω to 72.46Ω,
- load capacitance, C, from $1pF$ to $1nF$.

And, $\mathcal{Q} = \text{diag}\{10, \quad 10\}$, $\mathcal{R} = \text{diag}\{1000, \quad 1000\}$.

Then, optimization problem is resolved, obtaining

$$K_1 = -0.49, \quad K_2 = 0.72.$$

This was obtained for $c = 1.1'$, $\mu = 4.6 \cdot 10^{10}$, $G = \begin{bmatrix} -0.15 & 0.82 \end{bmatrix}$ and $P_1 = \begin{bmatrix} 0.0001 & 0.0002 \\ 0.0002 & 2.8574 \end{bmatrix} \cdot 10^6$. Note that even if the control constant tuning is conservative, there is a feasible solution.

VI. Simulation Results.

Some simulations show the robustness of the optimal saturated control law proposed for the Vdd-Hopping circuit. Likewise, a comparison between the performance achieved with the control gains obtained in this paper with respect to another control gains obtained in [15] is performed. These simulations are done by using the parameter values given in Section above.

A. Uncertain PMOS resistance

In this kind of systems, the electrical characteristic of the PMOS can suffer changes due to temperature changes.

In Fig. 3 the simulation is performed increasing the value of the PMOS resistance by 20%. The system in the low voltage level converges to $0.78V$, which is inside the interval given by (9), $\mathcal{I}_l = [0.74V, \quad 0.86V]$. Likewise, the high voltage level converges to $1.133V$, which is inside the interval given by (10), $\mathcal{I}_h = [1.132V, \quad 1.155V]$. These tests show that the equilibrium is robust with respect to parameter uncertainties and delays. And, the current peaks are small.

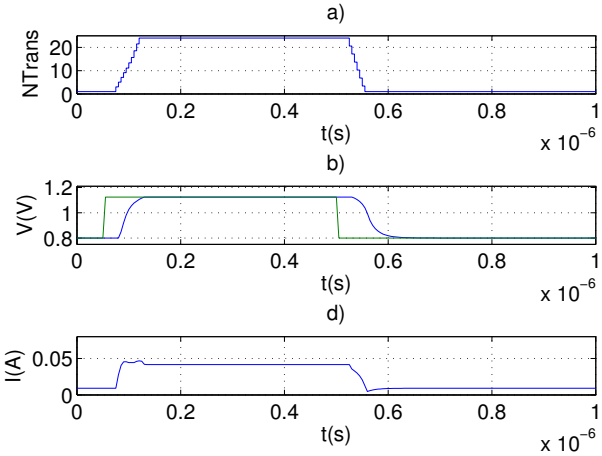

Fig. 3: $R_0 = 31.41\Omega \rightarrow R_0 = 37.7\Omega$, $K_1 = -0.47$, $K_2 = 0.68$. Evolution of the: a) number of transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

B. Uncertain load parameter

Another example shows that system performance is sensitive to the values of K_1 and K_2.

The capacitance employed during the control design and the previous simulations has been $C = 1nF$. In the following, it is desired to validate the system robustness when $C = 1pF$, i.e., 1000 times smaller. The lack of knowledge of the load in the real applications of these

systems may imply this change of three order of magnitude. Some simulations are shown using the robust control gains computed in this paper (Fig. 4) and the control gains computed in [15] (Fig. 5), which are $K_1 = -19.3$ and $K_2 = 39.27$. These gains were computed linearizing the closed-loop system around the set point. $K = [\bar{K}_1, \bar{K}_2]$ are defined by ensuring that $A + BK$ is Hurwitz and placing the poles by trial and error, in such a way, that the nonlinear system presents a suited behaviour. Note that, in Fig 5, the system does not respond to voltage variation. However, in Fig. 4 the system performance is satisfactory. This example shows the great robustness of the system when the robust control tuning is employed.

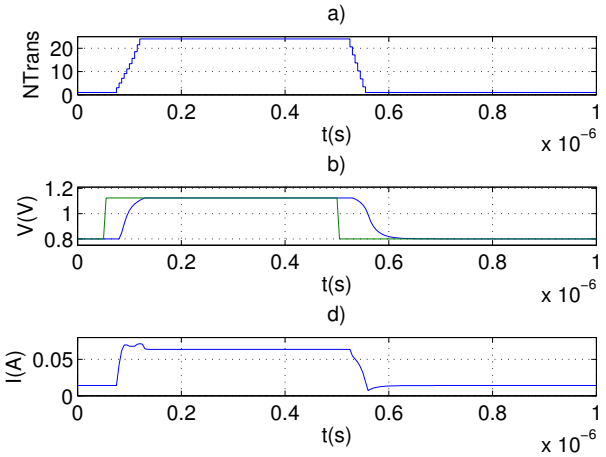

Fig. 4: $C = 1nF \rightarrow C = 1pF$ and $K_1 = -0.47$, $K_2 = 0.68$. Evolution of the: a) number of transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

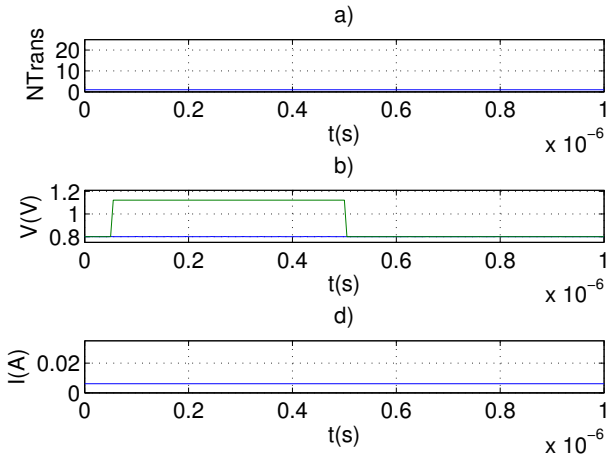

Fig. 5: $C = 1nF \rightarrow C = 1pF$ and $K_1 = -19.3$, $K_2 = 39.27$. Evolution of the: a) number of transistors switched on, b) v_r (dashed) and v_c (solid), c) current I_l.

VII. Comparison with the 'intuitive' controller of [8]

A comparison is performed between the controller presented here and the 'intuitive' controller proposed in [8]:

$$u_k = \text{sat}_1^N\{u_{k-1} + sign(e_k)\}. \tag{40}$$

A. Voltage and current performance

Control (40) switches on or off one transistor according to the sign of the error voltage signal. Therefore, this controller has the limitation that one only transistor can be switched on or off at every sampling time. On the other side, v_r follows a linear time evolution between $V_l = 0.8V$ and $V_{c_h} = 1.12V$ with a slope specified in [8] equal to $1.015106V/s$. A simulation of this controller is performed by using the parameter values given in Section VI. This simulation is shown in Fig. 6,. Note that, the performance presents an oscillatory behavior, with important current peaks. In addition, transient periods are slower and occurs significant current peaks in comparison with Control (4).

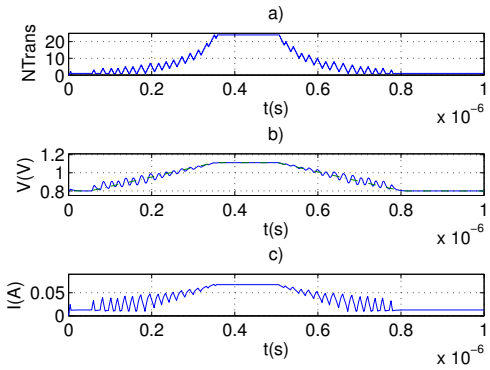

Fig. 6: 'Intuitive' control. Evolution of: a) number of PMOS transistors switched on, b) v_r (dashed) and v_c (solid), c) current. I_l.

B. Energy evaluation

In the set of PMOS, the dissipated energy in the transient period depends on the kind of control law employed, i.e., on the switching sequence. The purpose here is to evaluate the energy cost associated with the set of PMOS transistors during the rising transient period using Control (4) and the 'intuitive' controller proposed in [8] (assume that the falling transient period is similar). An estimation of the PMOS transistors during the transient period is

$$E_d = \int_{t_0}^{t_f} (V_h - v_c) I_l dt,$$

where t_0 is the initial time and t_f is the final time in such transient period.

Figure 7 shows the dissipated energy during the rising transient period. Note that the energy consumption is much higher using the controller proposed in [8] than using Control (4). More precisely, this energy consumption has

been reduced from $7.2\mu J$ to $0.34\mu J$, i.e., 95% reduction. Notice that a nonsmooth behavior of the current transient and a larger transient period may result in a higher energy consumption.

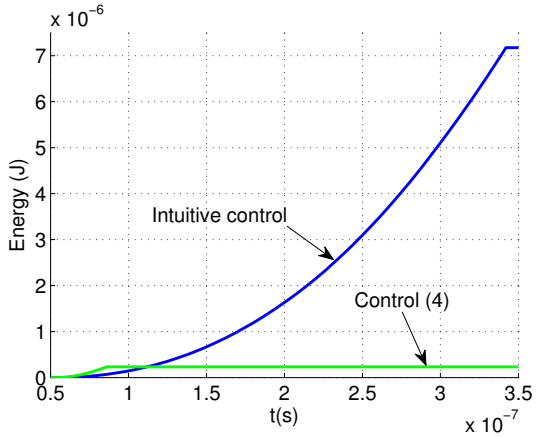

Fig. 7: Energy dissipated during the rising transient period.

VIII. Conclusions

In this paper an optimal and robust saturated controller was designed for the time-delay Vdd-hopping circuit. This optimal controller minimizes a performance index that, among other considerations, limites high current peaks. As side effect, this controller improves the dissipated energy and it achieves fast transient periods. The system is rewritten in a suited state-space representation, such that, an optimal and robust problem can be formulated to tune the control gains. This problem is dealt with Lyapunov Krasovskii theory, which provides some stability conditions through Linear Matrix Inequalities (LMIs). Consequently, a robust equilibrium stability as well as a robust disturbance rejection under parameter uncertainties are ensured for the time-delay system. The method also takes into account the control saturation estimating an attraction domain.

The closed-loop system robustness is shown by means of some simulations. Likewise, a comparison of the obtained control tuning design with respect to an 'intuitive' controller presented in [8] is performed. The robust control tuning design leads to higher controller gains but they are valid with respect to the saturation limits.

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References

[1] A. Chandrakasan and R. Brodersen, *Low power digital CMOS design*. Kluwer Academic Pub, 1995.

[2] T. Burd and R. Brodersen, "Design issues for dynamic voltage scaling," in *in Proc International Symposium on Low Power Electronics and Design*. ACM, 2000, pp. 9–14.

[3] G. Wei and M. Horowitz, "A fully digital, energy-efficient, adaptive power-supply regulator," *IEEE Trans. on Solid-State Circuits*, vol. 34, no. 4, pp. 520–528, 1999.

[4] G. Patounakis, Y. Li, and K. Shepard, "A fully integrated on-chip DC-DC conversion and power management system," *IEEE Trans. on Solid-State Circuits*, vol. 39, no. 3, pp. 443–451, 2004.

[5] A. Dancy, R. Amirtharajah, and A. Chandrakasan, "High-efficiency multiple-output DC-DC conversion for low-voltage systems," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 3, pp. 252–263, 2000.

[6] V. Gutnik and A. Chandrakasan, "Embedded power supply for low-power DSP," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 5, no. 4, pp. 425–435, 1997.

[7] S. Lee and T. Sakurai, "Run-time voltage hopping for low-power real-time systems," in *Proc. Annual Design Automation Conference*. ACM, 2000, pp. 806–809.

[8] S. Miermont, P. Vivet, and M. Renaudin, "A Power Supply Selector for Energy-and Area-Efficient Local Dynamic Voltage Scaling," *Lectures Notes in Computer Science*, vol. 4644, p. 556, 2007.

[9] M. Klein, J. Lehoczky, and R. Rajkumar, "Rate-monotonic analysis for real-time industrial computing," *IEEE Computer*, vol. 27, no. 1, pp. 24–33, 1994.

[10] E. Fridman and U. Shaked, "Delay-dependent H_{inf} control of uncertain discrete delay systems," *European Journal of Control*, vol. 11, no. 1, pp. 29–39, 2005.

[11] K. Gu and S. Niculescu, "Stability Analysis of Time-Delay Systems: A Lyapunov Approach," *Advanced Topics in Control Systems Theory, Lecture Notes from FAP*, pp. 139–170, 2005.

[12] E. Fridman, A. Seuret, and J. Richard, "Robust sampled-data stabilization of linear systems: an input delay approach," *Automatica*, vol. 40, no. 8, pp. 1441–1446, 2004.

[13] Y. Cao, Z. Lin, and T. Hu, "Stability analysis of linear time-delay systems subject to input saturation," *IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 2, pp. 233–240, 2002.

[14] S. Miermont, "Contrôle distribué de la tension d'alimentation dans les architectures gals et proposition d'un sélecteur dynamique d'alimentation," Ph.D. dissertation, Institute National Polytechnique de Grenoble, December 2008.

[15] C. Albea, C. Canudas-de Wit, and F. Gordillo, "Control and stability analysis for the Vdd-hopping mechanism," *In Proc. IEEE Conference on Control Applications (CCA)*, 2009.

[16] C. Albea and C. Canudas-de Wit, "Dispositif de commande numérique pour un tableau de transistors pmos en parallele," *Patent Number:08/07342*.

[17] C. Albea, F. Gordillo, and C. Canudas de Wit, "High performance control design for dynamic voltage scaling devices," *IEEE Trans. on Circuits and Systems I: Regular Paper*, no. 99, pp. 1–1.

[18] T. Hu and Z. Lin, *Control systems with actuator saturation: analysis and design*. Birkhauser, 2001.

[19] E. Fridman and U. Shaked, "A Descriptor System Approach to H_∞ Control of Linear Time-Delay Systems," *IEEE Trans. on Automatic Control*, vol. 47, no. 2, pp. 253–270, 2002.

[20] ——, "An LMI approach to stability of discrete delay systems," *In Proc. of the European Control Conference*, 2003.

[21] E. Fridman, A. Pila, and U. Shaked, "Regional stabilization and H_∞ control of time-delay systems with saturating actuators," *International Journal of Robust and Nonlinear Control*, vol. 13, no. 9, pp. 885–907, 2003.

[22] K. Gu, V. Kharitonov, and J. Chen, *Stability of time-delay systems*. Birkhauser, 2003.

[23] P. Millan, L. Orihuela, C. Vivas, and F. Rubio, "An optimal control L_2-gain disturbance rejection design for networked control systems," in *Proc. IEEE American Control Conference (ACC), 2010*. IEEE, 2010, pp. 1344–1349.