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Guidelines for MOSFET Device Optimization accounting for L-dependent Mobility Degradation

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Abstract
This paper reports a new methodology to monitor L-dependent mobility degradation based on empirical modeling of experimental results. This method allows benchmarking the impact on mobility degradation of different technological modules, thus giving some guidelines for device optimization.

Introduction
As channel length L of MOSFETs is scaling down, carriers’ mobility μ is degraded by additional scattering mechanisms with a dramatic impact below 100nm. As reported by Andrieu et al. [1] and by Cros et al. [2] (Fig.1), this mobility crisis affects both electrons and holes. Moreover, this degradation has been measured for both poly-Si gate and metal gate [3], for both high-K and SiO2 [4], for strained and unstrained devices [1,3], for doped and undoped channel [2,4] and also whatever the device architecture: Bulk [1], SOI [4,5], Gate-All-Around [2] or FinFET [6]. This μ(L) degradation was confirmed whatever the extraction method, i.e. Y-function, Split-CV or magneto-resistance [7], and cannot be solely explained by ballistic effects [8,9]. Unfortunately, mobility falls is a sign of a poor quality of the transport in the channel keeping us away from the ballistic regime. Whatever the conduction regime (ballistic or drift-diffusion), the on-state current will be limited by a maximum velocity that can be expressed as \( v_{\text{max}} = \min(v_{\text{sat}}, v_{\text{inh}}) \) [10]. As shown in Fig.2, strong mobility degradation on short devices prevents from reaching the velocity limit, i.e. maximum on-current. Some authors [7,11] have identified those additional scattering mechanisms as impurity Coulomb scattering while neutral defects have been suggested by others [2,4]. This statement gives ground for a systematic examination of \( \mu(L) \) degradation in order to establish guidelines for device optimization even if the precise origin of those additional scattering mechanisms is still not fully understood.

Experiment Methodology & μ-Degradation Modeling
A handy tool for extracting the mobility and monitoring its length dependence is the low field mobility \( \mu_0 = \frac{1}{L_{\text{eff}}} \frac{1}{W_{\text{eff}}} \frac{1}{C_{\text{ox}}} V_{\text{DS}} \). At low \( V_{\text{DS}} \) (<V₉₀₉), \( Y(\mu_0)=\frac{1}{2} \frac{L_{\text{eff}}}{W_{\text{eff}}} \frac{1}{C_{\text{ox}}} V_{\text{DS}} \) is extracted from the Y-function [12] while effective channel length and width (resp. \( L_{\text{eff}} \) and \( W_{\text{eff}} \)) and gate oxide capacitance \( C_{\text{ox}} \) are obtained independently from gate-to-channel \( C_{\text{ox}} \) measurements [13]. The notion of \( \mu_0 \) is illustrated by Fig.3. It is also worth noticing that classical Coulomb scattering and surface roughness terms do not significantly alter \( \mu_0 \) under strongly inversion conditions (species, energy, dose). Results in Fig. 10 are demonstrating that S/D architecture optimization is possible even when reducing the RTP temperature.

Mobility boosters: After having examined some possible causes of degradation, we have now investigating the effects of mobility boosters on mobility degradation. Local process induced stress (PIS) engineering by using eSiGe stressors is studied in Fig.11, while surface orientation is considered in Fig.12. Even if both strategies have an impact on holes’ \( \mu_{\text{max}} \) only local PIS which is also L-dependent [18] significantly improves \( \mu_0 \).

Discussion & Guidelines
Seeing the strong degradation of the mobility, one could think that any mobility improvement is not relevant since all strategies will finally have the same mobility at very short gate length. Using our model, we have extrapolated from the measurements the resulting mobility at \( L_{\text{eff}}=10\text{nm} \) in Fig.13. We can see that mobility improvement is still possible even at 10nm if well optimized. We have also investigated a possible link between \( \mu_{\text{max}} \) and \( \mu_0 \) in Fig.14: no clear correlation was found between the two parameters meaning that they are needed to monitor the mobility degradation. Thus we have introduced a new figure of merit \( \eta = \frac{\mu_{\text{max}}}{\mu_0} \). Higher \( \eta \) is, higher the short channel mobility will be and closer to its limiting velocity the device will operate. Finally, we give some guidelines, based on this work in Fig.15 in order to limit \( \mu(L) \) degradation.

Conclusion
Using a new monitoring method based on empirical modeling of \( \mu(L) \) degradation, we have systematically examined the impact on \( \mu(L) \) of the gate stack, channel doping, junction architecture and mobility boosters. It has been found that this degradation is not ineluctable and that working on key technological modules would help us to get closer to the ballistic regime.

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for both electrons and holes. Fig. 1: Literature data from [1] & [2] clearly showing length dependent mobility degradation for both electrons and holes.

![Graph showing mobility as a function of channel length](image1)

Fig. 2: Strong mobility degradation on short devices prevents from reaching the velocity limit, i.e. maximum on-current. Fig. 5: \( \mu_{\text{eff}} \) measurements for different \( L_{\text{eff}} \). \( \theta_1 \) and \( \theta_2 \) are kept constant for all channel lengths. Inset: \( L_{\text{eff}} \) definition. Fig. 6: Length dependent mobility degradation model introducing mobility degradation factor \( \alpha_\mu \).

\[
\alpha_\mu = 0, \quad \mu_{\text{Effective}}(L_{\text{eff}}) = C \cdot \text{Cte}
\]

![Graph showing mobility as a function of channel length](image2)

Fig. 3: Illustration of low field mobility \( \mu_0 \) vs. \( Q_{\text{inv}} \) measured by Y-function @\( Q_{\text{inv}} \approx 0 \). Coulomb scattering & surface roughness scattering are negligible. Fig. 7: Comparison of electron mobility between two SiON gate oxide thicknesses. Thinner 12Å oxide is more degraded than 17Å.

![Graph showing mobility as a function of channel length](image3)

Fig. 4: Series resistance \( R_{\text{SD}} \) correction which is critical on short devices is intrinsically taken into account when using Y-function.

![Graph showing mobility as a function of channel length](image4)

Fig. 8: Comparison of electron mobility between different metal gate materials. Nitrided metals are more degraded than not nitrided.

![Graph showing mobility as a function of channel length](image5)

Fig. 9: Comparison of electron mobility between undoped & doped ultra thin body (UTB) with high-K/metal gate stack. Fig. 10: Comparison of electron mobility between two S/D architectures while keeping the same Poly/SiON gate stack.

![Graph showing mobility as a function of channel length](image6)

Fig. 11: Comparison of hole mobility between unstrained reference and locally strained device with eSiGe S/D stressors.

![Graph showing mobility as a function of channel length](image7)

Fig. 12: Comparison of hole mobility between (100)\textsuperscript{<110>} device and (110)\textsuperscript{<110>} device with same poly/SiON gate stack.

![Graph showing mobility as a function of channel length](image8)

Fig. 13: Sub-100nm electron mobility with extrapolation at \( L_{\text{eff}} = 10 \text{nm} \) using our model.

![Graph showing mobility as a function of channel length](image9)

Fig. 14: \( \alpha_\mu \) as a function of \( \mu_{\text{max}} \) clearly showing no universal correlation between \( \alpha_\mu \) & \( \mu_{\text{max}} \).

![Graph showing mobility as a function of channel length](image10)

Fig. 15: Guidelines for short channel mobility optimization based on the figure of merit \( \eta = \frac{\mu_{\text{max}}}{\alpha_\mu} \).

References