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STATISTICAL ANALYSIS OF IMPLANT ANGLES EFFECTS ON ASYMMETRICAL NMOSFETS CHARACTERISTICS AND RELIABILITY

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Résumé: - L'analyse statistique de la dissymétrie des caractéristiques électriques des transistors NMOS LDD traduit l'influence des angles d'implantation sur la variation du non recouvrement grille-drain (ou grille-source) observé sur les dispositifs réalisés sur une même plaque et sur les différentes plaques d'un même lot de fabrication. La conséquence de cette dispersion sur le vieillissement des structures montre l'importance du suivi de ce paramètre pour la fiabilité des transistors et la prudence nécessaire pour l'interprétation des résultats de stress électrique effectué sur les transistors.

Abstract: - Statistical analysis of asymmetry in LDD NMOSFETS electrical characteristics shows the influence of implantation angles on non-overlap variation observed on devices realized on a 100 mm wafer and within the wafers of a batch. The study of the consequence of this dispersion on the aging behaviour illustrates the importance of this parameter for reliability and the necessity to take it in account for accurate analysis of stress results.

INTRODUCTION:

The development of short channel NMOSFETS needed the design of new structures in order to decrease the peak value of the Electric field near the Drain edge. Several ways have been investigated (eg. LDD, DDD architecture) which have given good results in reducing hot carriers degradation. On the other hand, those devices are known to be sensitive to process parameters like implantation angles (Tilt and electrostatic scanning), gate etching profiles ..., which have a strong influence on the asymmetry of NMOS devices, depending on the position of the device with respect to the ion beam [1,2].

The asymmetry of transistors (due to the shadowing effect of the gate edge on lightly doped implants) is shown to play an important role on the aging behaviour of the devices.

EXPERIMENTAL

In order to analyse the consequences of tilt and electrostatic scanning angles on devices, we have designed a test structure including two perpendicular typical NMOSFETS (50 x 1 µm²). LDD devices are fabricated through a 1 µm N-well CMOS process using a sidewall spacer technique, with a gate oxide thickness of 25 nm. The lightly doped junction implant is done through an arsenic implant dose of 10¹³ cm⁻², with 7° off-axis. Initial electrical test measurements are made on an automatic test line in order to analyse the differences in bulk and drain currents at a given voltage condition (Vd=7 V, Vg=3.5 V) for both perpendicular structures in the forward and reverse mode (inverting the role of drain and source). This work is carried out for all the wafers (Φ=100 mm) in a batch, in several positions per wafer (20 or 60 depending on the process) (see fig.1).

Electrical stresses are performed on those devices, in order to show the consequences of the asymmetrical behaviour of devices on the reliability, along a diameter of a 100 mm wafer. Transistors are stressed, at room temperature, for 10 hours. The stress conditions are: Vd=7 Volts, Vg=3.5 Volts.

RESULTS

1. INFLUENCE OF ELECTROSTATIC SCANNING

We analysed the differences in bulk or drain current for the two perpendicular devices with the test made in a given order (from chip 1 to 20). We defined the difference in drain currents by

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\[ \text{Diff} = 2 \times \frac{(I_{df} - I_{dr})}{(I_{df} + I_{dr})} \]

\[ I_{df} = I_{d} \text{ in forward mode (} V_d = 7\text{V}, V_g = 3.5\text{V)} \]

\[ I_{dr} = I_{d} \text{ reverse mode} \]

The same work was made for bulk currents and gave similar results.

To illustrate the influence of the two electrostatic scanning angles, we plot the differences in two directions (see fig. 1):

a. Along the direction parallel to the primary flat (see fig. 2a), the gradient is evident for devices with the channel parallel to the flat, with a difference between the upper and the lower device of about 6%.

b. Along the direction perpendicular to the primary flat (see fig. 2b), the gradient is significant only for the devices with the channel perpendicular to the flat. The dispersion between the upper and the lower device is about 4%.

\[ \text{fig 2. Gradient of drain current asymmetry along the direction parallel (2a.) and perpendicular (2b.) to the primary flat} \]

\[ \text{for channel parallel to primary flat , + for channel perpendicular to primary flat} \]

The two different behaviours are explained by the influences of the electrostatic scanning angles of the implantor on a whole wafer. The differences in the two directions are due to the different scanning angles along the two directions in our implantor. It means that, even with a 0 off-axis implant angle, we find some devices with a non-overlap drain structure.

\[ \text{2-INFLUENCE OF THE TILT ANGLE} \]

For avoiding the channeling effect during the implant, the wafers are implanted with a tilt angle of 7 degrees. That tilt angle gives different results on wafers depending on the position of the wafer during the operation (see fig 3). If we plot the differences in currents for the two perpendicular directions (see fig 4a.), the points are distributed along a circle.

That circle is due to the fact the tilt angle has a complementary effect on the perpendicular transistors. The values measured on a whole wafer (illustrated by the same number) are centered around a median position depending on the random position of the wafer during the low dose implant. If the analysis is done in only one direction, it is possible to locate symmetrical devices that give the best results in stress measurements. However, this case means the worst case for perpendicular devices.

The diameter of the circle shows the process sensitivity to the tilt angle (see fig 4a. and fig 4b.).

\[ \text{fig 3. Drain current asymmetry on different wafers of the same batch (60 points per wafer)} \]
fig4. Influence of the technology on bulk current asymmetry

3-CONSEQUENCES ON DEVICES RELIABILITY
Asymmetrical devices are known to be very sensitive to electrical stresses performed in the non-overlap region [3]. In order to show the consequence of the dispersion of electrical characteristics over a wafer, we analysed one with a central value of Diffid = 0. In that case, transistors structures change from a drain overlap to a non-overlap situation along a diameter. The results of the stress show only a slight degradation of the transconductance ($dGm/G_{m0} < 5\%$ for 10 hours of stress) until we reach the non-overlap condition, which gives the worst results (see fig 6). A factor of 4 in $G_m$ degradation is observed between the two extreme cases, after 10 hours of stress.

CONCLUSION
Such an analysis, with only a few complementary measurements, gives an accurate idea of the process sensitivity to implant angles and provides a predictive tool for aging behaviour of advanced CMOS structures.

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