Ultra-Low Power RFIC Solutions for Wireless Sensor Networks

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Ultra-Low Power RFIC Solutions for Wireless Sensor Networks

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to my parents...

to my dear father...

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Abstract

[**EN**] Since their emergence, Wireless Sensor Networks (WSN) have been growing continually becoming a key player in many applications such as military tracking, remote monitoring, bio-sensing and home automation. These networks are based on IEEE 802.15.4 standard which is dedicated to low rate wireless personal area networks (LR-WPANs) in the unlicensed radio band (868 MHz/915 MHz/2.4 GHz). Low power consumption, low cost of implementation and high level of integration are the main challenges of these systems. As radio frequency transceiver is one of the most power hungry block in wireless sensor node, power consumption of radio frequency front-end (RFFE) must be reduced. To deal with, several approaches are possible, either at circuit level by investigating operating modes of transistors and merging functionalities or at system level by searching novel demodulating architectures. This thesis explores the specific requirements and challenges for the design of a very-low power 2.4 GHz down conversion mixer operating in moderate inversion region and consuming 330 µW. A second circuit merging the local oscillator and the mixer was designed and implemented in 65 nm CMOS technology. The self-oscillating mixer (SOM) operates at a radio frequency of 2.4 GHz and consumes 600 µW from a 1 V supply. Finally, a compact demodulator implemented in 65 nm CMOS technology was proposed. It uses a novel architecture to demodulate all analog modulations while consuming just 120 µW from a 0.5 V supply and achieving a sensitivity less than −30 dBm in the case of AM modulation.

[**FR**] Depuis leur apparition, les réseaux de capteurs sans fil (WSN) n'ont cessé de se développer pour devenir un acteur clé dans de nombreuses applications telles que le suivi militaires, la surveillance à distance, la bio-détection ou la domotique. Ces réseaux basés principalement sur la norme IEEE 802.15.4 qui est consacrée aux réseaux sans fil personnels à faible débit et à faible portée (LR-WPAN) dans la bande de fréquences radio sans licence ISM (868 MHz/915 MHz/2.4 GHz). La faible consommation d'énergie, le faible coût de mise en œuvre et le niveau d'intégration élevé sont les principaux défis de ces systèmes. Le module radio est le bloc le plus gourmand en énergie dans un nœud capteur, sa consommation de puissance doit donc être réduite. Pour ce faire, plusieurs approches sont possibles, soit au niveau circuit en exploitant les modes de fonctionnement du transistor ou en fusionnant les fonctionnalités des blocs qui constituent un front-end radiofréquence. Soit au niveau système en examinant de nouvelles architectures de démodulation. Cette thèse explore les exigences et les défis spécifiques pour la réalisation d'un mélangeur à très faible consommation fonctionnant en zone d'inversion modérée et consommant 330 µW. Un second circuit combinant l'oscillateur local et le mélangeur a été conçu et réalisé en technologie CMOS 65 nm. Le "Self-Oscillating Mixer" (SOM) fonctionne à une fréquence radio de 2.4 GHz et consomme 600 µW sous une tension d'alimentation de 1 V. Enfin, un démodulateur compact a été réalisé en technologie CMOS 65 nm. Il utilise une nouvelle architecture pour démoduler toutes les modulations analogiques, cette approche se base sur la théorie de synchronisation des oscillateurs. Le système proposé consomme uniquement 120 µW sous une alimentation de 0.5 V et permet d'atteindre une sensibilité inférieure à −30 dBm dans le cas d'une modulation AM.

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Finally, I want to dedicate this modest work to my home country, Tunisia, to all the people who started the revolution at the end of 2010 and who continue to struggle for a better future. Living this event while being far away was really hard. Special thanks to all my friends there for their constant and helpful support.

Last but of course not least, I thank my parents and my family for their permanent support and especially for their sacrifices which has allowed me to continue my studies. I am really grateful to them. I dedicate this thesis to my dear father that I would have loved to share this moment with him but unfortunately life decided otherwise. He taught me how to stay strong in tough times, I love you Dad.

Chapter 1

Introduction

In recent years, a trend toward a world in which people will be surrounded by networked devices that are sensitive and adaptive to their needs can be foreseen. This trend has been expressed in a vision called Ambient Intelligence (AmI). It is possible to partition this world into three different classes of devices called "Watt nodes", "milli-Watt nodes" and "micro-Watt nodes" [8]. The "Watt nodes" and the "milli-Watt nodes" demand a further improvement in technology scaling to meet the low-power target. In contrast, the design of a "micro-Watt" node requires meeting the limit of miniaturization, cost reduction and power consumption. Therefore, the complexity of this task is not in the number of transistors but in the capability to optimally combine technologies, circuit and protocol innovation to obtain the utmost simplicity of the wireless node. One implementation of these "micro-Watt nodes" can be achieved through wireless sensor networks (WSN). Since their emergence, they keep on growing up, becoming a key player in most industrial applications. Thanks to their ease of implementation and very low cost, these networks are extensively used in wireless personal or body area networks (WPAN or WBAN) enabling a wide variety of compelling applications. As an example, WSN are used to survey the environment or to monitor energy consumption in residential buildings. The use of WSN enables real-time pricing and adaptive

energy usage without user intervention. Several applications require low datarate, very low power consumption and a long lifetime for the battery. In this case the easier management of the wireless nodes has allowed discarding the star-mesh in favor of a more flexible peer-to-peer architecture. Within this evolving scenario, the ZigBee [9] and the other wireless sensor networks standards represent an additional step towards an even more flexible system able to reshape itself dynamically. Due to their nature, these systems do not require any base-station, since they are formed by autonomous short-range wireless nodes, which monitor and control the environment defining the working area by their spatial distribution. Since the high density of units makes the system more flexible and relaxes the sensitivity of the single receiver, in ZigBee compliant networks the performance is exchanged with the possibility of having long-lasting and cheap devices [2]-[10]. However there is a trade-off between efficiency and cost which settles the density of nodes in a WSN. One of the most critical components making up an efficient sensor node is the wireless transceiver, which transmits and receives data packets in order to provide the communication link between distributed nodes. The goal of this research activity through MIRANDELA project is to comprehensively address the challenges in implementing ultra-low power CMOS RFIC solutions for WSN.

1.1 System Requirements

The implementation of wireless sensor networks involve a hardware optimization in order to make dense node deployment possible in practical scenarios, each node must be physically and economically unobtrusive. In order to make these networks a reality, the wireless node should be optimized for three metrics:

- **Low cost**: The utility of the network depends on high density and ubiquity, which means a large numbers of nodes. In order to make large-scale deployments

economically feasible, nodes must be very low cost.

- **Small size**: Embedding the components into the existing infrastructure of daily environments (walls, furniture, lighting, etc.) requires a very small form factor of the entire sensor node. Typically, node volumes less than $1\,cm^3$ (much smaller than a AA battery) are necessary. A very high level of integration is mandatory if such small dimensions are to be achieved.

- **Low power**: For large networks with many nodes, battery replacement is difficult, expensive, or even impossible. Nodes must be able to function for long periods, ideally up to 10 years, without running out of power.

Each of these three factors are somewhat intertwined. For example, electronic components are already so small that overall module size is limited by power supply or energy storage requirements. For this reason, reducing power consumption of the electronics is an effective way to shrink size as well. Another example is that highly integrated circuits with few external components can simultaneously reduce both size and cost. One of the most compelling reasons to reduce power consumption is to enable the use of new power supply technologies like energy harvesting [11] and low cost printable batteries [12]. These early-stage developing technologies cannot supply much power, so any means of reducing power requirements will hasten the adoption of next-generation power supplies. A successful implementation of wireless sensor networks require improvements in several disciplines: networking, low power RF and digital IC design, MEMS techniques, energy scavenging, and packaging. Figure 1.1 shows the various specialized blocks of a sensor node. In the implementation of extremely small sensor nodes, each of these blocks becomes crucial. However, among all the functions, the wireless communication component is the most power consuming one and the most challenging issue in implementing a wireless node is the integration of ultra-low power RF transceiver. Therefore, the main target of this research is to reduce the energy dedicated to communication in wireless sensor nodes. In order to reach this goal, it is important to understand the needs of RF transceivers in WSN.

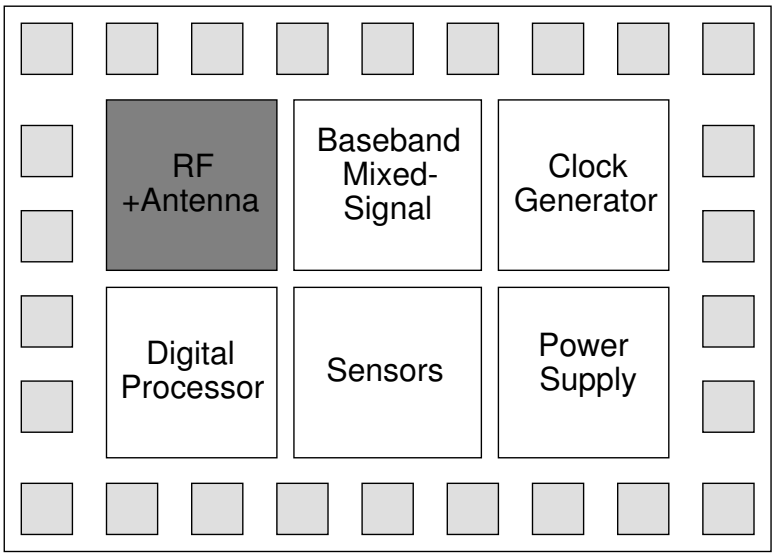


Figure 1.1: Hardware blocks for wireless sensor network implementations

1.2 RF Transceiver Requirements

This section describes the transceiver requirements [13] that are unique to sensor node communications. It is further demonstrated, the radio requirements are very different from traditional low power transceivers (pager receivers, RFID tags, Bluetooth-specification radios, keyless-entry).

1.2.1 Power Consumption

In the design of prototype sensor nodes, the wireless interface consumes the largest fraction of the power and size budget of the node. While the demands of the sensing and digital processing components cannot be ignored, their duty cycle is typically very low. A combination of advanced sleep, power down, and leakage reduction techniques allows to make their average power dissipation virtually negligible [14]. Thus, the wireless interface for sensor networks is the dominant source of power consumption. Whereas optical communication approaches offer the potential of very low power and small size, line-of-sight and directivity considerations make them less attractive [15].

1.2.2 Datarate

As mentioned, the requirements of a transceiver for wireless sensor networks differ dramatically from a traditional wireless link. Thus, common performance metrics such as energy/bit and bits/s/Hz should be applied with the realization that other factors prevail. For example, a modified metric such as energy/useful-bit is relevant if all sources of power and overhead (for example: synchronization, the impact on energy storage) are included. First we will examine the typical operation mode of the sensor node. An investigation of the traffic patterns and data payloads reveal that the transceiver operation is fundamentally different than a wireless LAN or Bluetooth-specification radio. Data packets in sensor networks tend to be relatively rare and unpredictable events. In most application scenarios, each node in the network sees only a few packets/second. In addition, the packets are relatively short (typically less than 200 bits/packet). This is expected as the payloads normally represent slowly varying and highly correlated environmental data measurements. Combined, this means that the average data rate of a single node rarely exceeds 1 kbit/s.

1.2.3 Range

In this discussion, we will assume that the nodes in the network are placed relatively closely (the average distance between nodes is less than or equal to 10 m). For a given sensitivity, scaling the node to larger ranges would require additional transmit power or increased coding gain (longer transmit times). As the transmitted power increases in low power transmitters, the global transmitter efficiency increases. Thus, in short-distance links, rising the transmitted power is the preferred approach over increased coding gain. As the transmitted power increases, a linear enhance in the link budget is obtained for a sub-linear increase in the transmitter power consumption. Improving the link budget through coding gain would involve linear or super-linear increases in the receive power consumption due to increased packet length and/or higher received bandwidths. Indeed, at transmitted power levels of −10 dBm and below, a majority of the transmit mode power is dissipated in the circuitry and not radiated by the antenna. However, at high

transmit levels (over 0 dBm), the active current draw of the transmitter is high. It is difficult to source high active currents with micro-scale energy scavengers and batteries. Convenient and efficient transmit power levels for sensor node applications are roughly in the range of -10 to 3 dBm.

1.2.4 Sensitivity

Figure 1.2 plots the theoretical range for a radio with a -70 dBm sensitivity for various RF propagation models at 2 GHz. As shown, the range varies greatly depending on the radio environment. For free space (where the path loss appropriate is R^2), a range of 37 m is achieved with a 0 dBm transmit power. However, in indoor environments, a higher exponent (R^3 or R^4) is more suited. In that regime, a transmit power of at least 0 dBm is required for a 10 m range. To add a margin for deep fading, the receiver sensitivity for a 0 dBm transmit signal and a 10 m range should be greater than -75 dBm. Thus, for this application, a receiver sensitivity of better than -75 dBm is imposed. Higher sensitivities will allow lower transmitted power levels, subject to the constraints in the previous section.

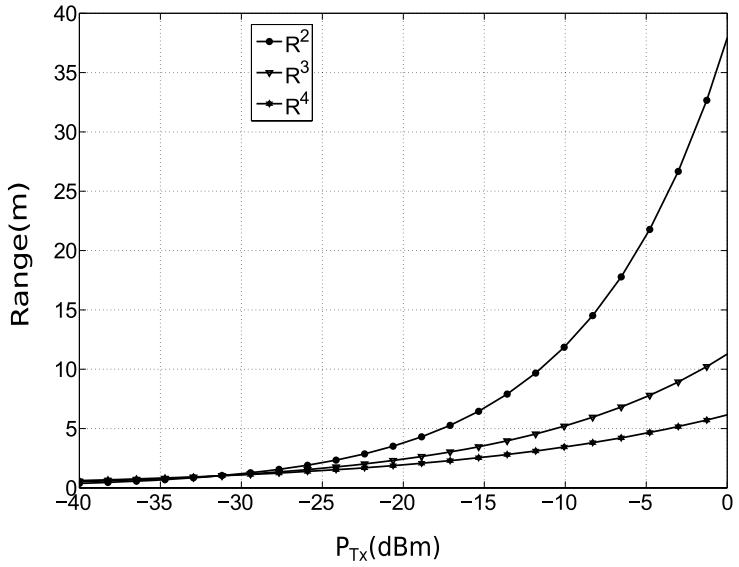


Figure 1.2: Radio range for receiver with a -70 dBm sensitivity

1.2.5 Turn-On Time

In an environment in which the radio is in idle or off mode most of the time, and in which data communications are rare and packets short, it is essential that the radio start up very quickly. For instance, a typical 1 Mbps Bluetooth specification radio with a 500 µs turn-on time would be poorly suited for the transmission of short packets. The on-time to send a 200 bit packet would be only 200 µs. Start-up and acquisition represent an overhead that is larger than the actual payload cost, and could easily dominate the power budget (given that channel acquisition is typically the most power-hungry operation). Thus, fast start-up and acquisition is essential to minimize this overhead. An agile radio architecture that allows for a quick and efficient channel acquisition and synchronization is desirable. Complex wireless transceivers tend to use sophisticated algorithms such as interference cancellation and large constellation modulation schemes to improve bandwidth efficiency. These techniques translate into complex and lengthy synchronization procedures and may require accurate channel estimations. Packets are spaced almost seconds apart, which is beyond the coherence time of the channel. This means that these procedures have to be repeated for every packet, resulting in major overhead unsuitable in a low-power environment. Simple modulation and communication schemes are hence the desirable solution if agility is a prime requirement.

1.2.6 Integration/Power Tradeoff

Achieving the goal of a very low power/low cost RF design is complicated by a well documented power/integration (cost) tradeoff. For example, the use of high performance SiGe processes, while offering the designer high f_T operation and low bias current levels, eliminates the possibility of integration with low power digital systems. A multi-chip solution would prohibitively increase the cost and area for sensor network applications. Another common strategy for CMOS RF designers trying to reduce power consumption is to use high quality passive surface mount components [16]. This solution also prohibitively increases cost and board area, as each surface mount inductor is larger than the entire transceiver chip. Recently published "fully integrated" transceivers typically refer to a

transceiver that has simply eliminated the need for external ceramic or surface acoustic wave (SAW) filters. They still, however, require an off-chip quartz crystal and various passive components. To meet the cost and form-factor requirements of this application, a truly fully integrated transceiver is mandatory. In addition to increasing the size, off-chip passives add more complexity and cost to the board manufacturing and package design. Furthermore, these macro-fabricated components increase the manufactured performance distributions of the radio by adding completely uncorrelated component variations. One method that can be used to achieve a high level of integration is the use of a relatively high carrier frequency. Currently available simple low power radios, as used in control applications, typically operate at low carrier frequencies between 100 and 800 MHz. A high carrier frequency has the distinct advantage of reducing the required values of the passive components, making integration easier. For example, a 2.53 µH inductance is needed to tune out a 1 pF capacitor in a narrow-band system at 100 MHz, requiring a surface mount inductor. For a 2 GHz carrier frequency, the inductance needed is only 6.33 nH, which can easily be integrated on-chip using interconnect metallization layers. In addition, the critical antenna physical dimensions are linearly related to the carrier frequency. For a given antenna radiation pattern and efficiency, a higher carrier frequency allows a much smaller antenna. A quarter-wavelength monopole antenna at 100 MHz would be 0.75 m long. At 2 GHz, the size shrinks to 37.5 mm, allowing very efficient and inexpensive board-trace antenna. However, the drive to higher carrier frequencies in the interest of high integration is in direct conflict with the need for low power consumption. As the carrier frequency increases, the active devices in the RF signal path must be biased at higher cutoff frequencies, increasing the bias current and decreasing the transconductance-to-current gm/Id ratio. The result is an increased power dissipation at higher carrier frequencies. Thus, an inherent tradeoff exists between integration and power consumption that must be addressed through architectural decisions and the use of new technologies.

1.3 Challenges

In order to meet the RF transceiver requirements of wireless sensor networks, several challenges have emerged addressing both physical and protocol layer issues. The energy scavenging problem for example is an important technological key issue in wireless sensor networks. In fact, offering a wireless node the possibility to harvest the energy from his environment is an ideal solution to improve the lifetime of the wireless sensor and to avoid costly battery replacement. However, the power efficiency of these energy scavenging sources is sometimes limited and must be enhanced to provide necessary power to the node. Another attractive challenge is the duty-cycle control of radio communication module. This latter is most of time in idle state and large amount of energy could be saved by choosing a proper duty-cycle control.

1.3.1 Energy Constraints

In order to reduce the implementation cost and to allow a flexible method of deployment, the node's battery lifetime must be enhanced. In fact, in many applications, the maintenance cost considerations render frequent replacement of the energy source deterrent. Thus, the node has to scavenge its energy from the environment. The energy storage capability is limited by the storage medium (battery or capacitor) and the size constraints. Single-time charge could work for applications with life cycles below one year, replacing the energy supply could be constraining for some applications and using energy scavenging is often a necessity. The finite power density of state-of-the-art energy sources is illustrated in Table 1.1 [7].

The average power dissipation of the node is severely constrained by the energy scavenging volume of the node. These sources can be broadly grouped into two categories: energy scavenging sources and energy storage sources. From a volume of $1\,cm^3$, an average continuous output power of $100\,\mu W$ could be supplied by one or a combination of these power sources. If a one year lifetime were acceptable, either a lithium battery or fuel cell would suffice. However, micro fuel cell technology is still in the early

Table 1.1: Average power density of various energy storage and scavenging devices [7]

Power Source	Power Density $\mu W\,cm^{-3}$	Lifetime
Lithium Battery	100	1 year
Micro Fuel Cell	110	1 year
Solar Cell	10-15000	$\propto$
Vibrational Converter	375	$\propto$
Air Flow	380	$\propto$
Temperature Gradients	50	$\propto$

stages of research, and is prohibitively complex and expensive. Another active area of research is the thin-film battery technology, which will yield large benefits for sensor node implementations. For desired node lifetimes greater than one year, however, $1\,cm^3$ does not provide ample storage for the node's 3110 J/year energy requirements. Typical node deployment scenarios would demand a 10 years lifetime (31 kJ). This is a prohibitively large amount of energy to store in a $1\,cm^3$ volume, requiring the harvesting of energy from the environment. Solar power is a proven and universal method of collecting ambient energy. For outdoor or high-light conditions, this is the obvious solution. However, in dim lighting conditions, the power output drops dramatically. In these environments, an additional energy source is needed. Vibrational converters, air flow generators, and temperature gradient generators all produce 50-400 $\mu W\,cm^{-3}$, as listed in Table 1.1. Of the three, vibrational converters are the simplest and they have the most potential for wafer-scale fabrication. In conclusion, a $1\,cm^3$ sensor node can support an average power draw of 100 µW. A combination of solar or vibrational energy scavenging and battery energy storage is likely to yield the most robust and inexpensive solution. In addition to limitations on average power dissipation, the available peak current levels that can be supplied to the electronics are also limited. In fact, the current consumption form is an important metric in wireless sensor networks and it is not surprising that wireless

sensor communication components score well on power consumption and utilization of wake-up/sleep modes for duty cycling. However, power consumption is only part of the solution. Four other factors must also be addressed in order to achieve low power in wireless sensor applications [17]. These are peak current, graceful power failure, low-power mesh routing and sleep current.

Peak current

The plot in Figure 1.3 [17] depicts the current consumption in three typical wireless sensor node states for a commonly used wireless sensor platform. In state one, the microprocessor and transceiver are in sleep mode (10 µA). In state two, the microprocessor is switched on while the transceiver is asleep (10 mA). In state three, both the transceiver and the microprocessor are awake (27 mA). These current draws can be sustained with

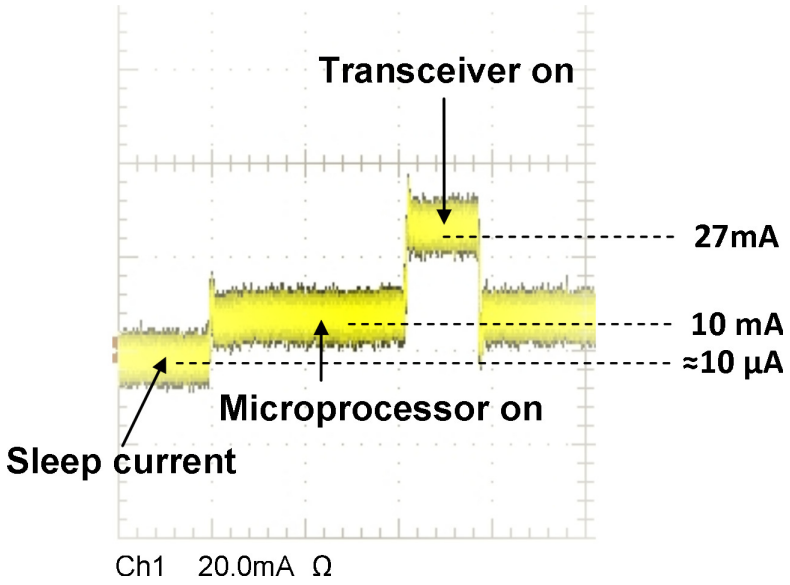


Figure 1.3: Three current consumption states in a wireless sensor node

high-power batteries such as alkaline cells, but they typically exceed the tight energy budgets available with small batteries or energy harvested sources. These energy sources share an important feature; they have a hard time generating the peak current needed to awaken the electronics, even if they can cope with the average current consumption

throughout the wake-up/sleep cycles. A coin cell battery, for example, has a typical maximum output power of 15 milliamps, far below the peak value that most wireless communication systems require. In addition, since most microscale energy scavenging and storage devices provide a naturally high impedance, the peak current drive capability is small (less than a few mA). Providing high drive current would require excessively large storage capacitors and complex voltage regulators. The RF datalink circuit design must address this issue by presenting a low peak active current draw.

Graceful power failure

When an energy source has dried out, the electronics cannot communicate and are dead. This unexpected situation can arise and must be taken into account, either as a normal event, solar cell at midnight as instance or as an exceptional condition (depleted battery). In both case, the power problem is expected to be forecasted before the energy source has completely dried out. During this last breath, the device should perform a number of actions to inform its environment of the situation, transmit some critical data and put itself in a state that allows fast recovery when the power is restored. To accommodate failing low-power energy sources such as batteries and solar cells, devices must employ a technique known as "graceful power failure". During normal operation, the devices carefully monitor the state of the power circuits. As they encounter declining power levels, they raise different levels of alarms ranging from early warning to near-death. The alarms are escalated and communicated to other parts of the system, thereby enabling the system to be placed in a state consistent with the alarm condition.

Low-power mesh routing

One of the most important differences between wireless sensor communication technology and other well-known wireless technologies is the ability of sensor nodes to forward messages from another one located further down in the communication chain. This technique, known as mesh routing or multi-hop networking, provides an effective and reliable means of spanning large infrastructures, beyond the range of what a single

wireless link can do. However, to forward a message received from a neighboring node, the concerned node needs to be in an awake and receiving mode when the original wireless message arrives. Unfortunately, the receiving mode requires so much power that it can drain batteries in a matter of a few days. The most straightforward solution, as specified by most industry standards, is to limit the multi-hop capability to the nodes that are permanently connected to the main power. In such a framework, low-power devices, which are assumed to be in a power-down mode most of the time, are not capable of retransmitting messages from other devices. These low-power devices, known as end-devices, are located at the end or beginning of the communication chain. This framework, which combines mains-powered mesh routing devices and low-power end-devices, works for some applications. Take, for example, an office lighting application utilizing interconnected wireless luminaires and light switches. The luminaires, which are connected to the main power source, house the mesh routing communication nodes. The switches, which are not mains powered, are a natural place for the end-devices. Many other applications do not fit well in such a framework. Think of gas detection, fire detection, access control, precision farming, battlefield monitoring, perimeter surveillance and warehouse temperature monitoring. In these applications, mains power is not readily available or even present. Running a power cable in these applications would be cost prohibitive, offsetting the benefit of wireless communication. To address this class of applications, which has been found to be more prevalent than mains-powered, multi-hop applications require a totally different framework. In this framework, known as low-power multi-hop networking or low-power routing, all of the nodes, including the mesh routing nodes, operate in low-power mode. The key to this approach, referred in the literature as "synchronized wake-up", is to coordinate receiving activity in a way that eliminates the need for the mesh routing nodes to continually operate in receive mode, thereby significantly reducing power consumption. Figure 1.4 depicts how low-power routing works when Node A wants to send a message to Node C, through Node B. All nodes in the picture are low-power nodes, sleeping most of the time. The breakthrough lies in synchronizing the sleep/wake-up cycles of the nodes to each other. Nodes wake up when

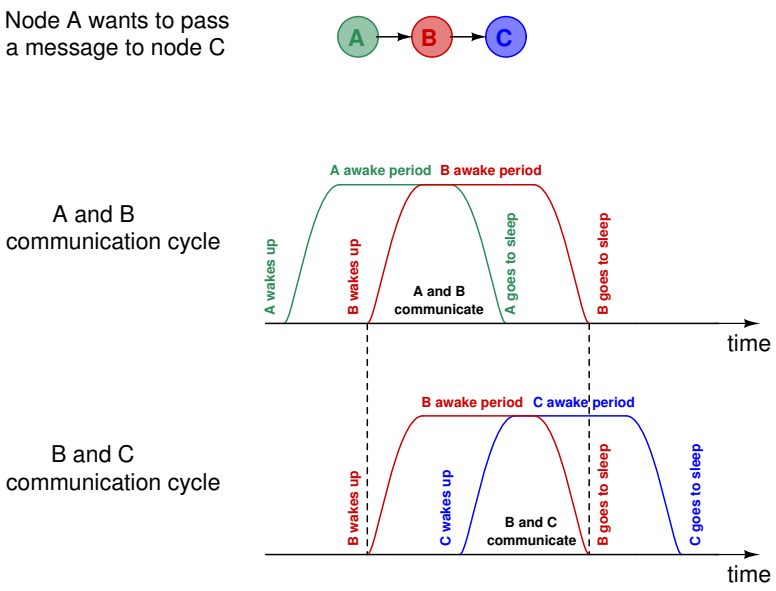


Figure 1.4: Synchronizing "awake" period among nodes

they expect a message from a neighboring node. This enables the routing nodes to operate in a nearly powerless sleeping state most of the time, thereby achieving ultra-low-power operation. Clearly, more wake-ups will occur than strictly required to carry the data, as neighboring nodes will not always have data to transmit. However, the additional power required for periodic wake-ups and synchronizations is more than offset by the power saved by eliminating the need for continuous receive mode operation.

sleep current

Wireless chips are usually specified according to their power consumption in receive and transmit mode. Remember, however, that in order to achieve low power, the devices must be duty cycled, moving between alternate sleep and awake states. The longer the required battery life, the longer the device sleeps between wake-up periods. Unfortunately, electronic circuits never really "sleep". Although the powered-down circuits don't yield anything meaningful from a functional standpoint, a small leakage current flows through the transistors. This leakage can amount to several tens of microamps. Sleep current is not usually considered as an important design factor, but it becomes extremely important

when designing a circuit that must live for five years or more on a battery, sleeping most of its life. If the design is not optimized for low leakage current, the majority of the power will be spent on sleeping.

1.3.2 Duty-cycle Control in Sensor Networks

Several methods can be used to address the duty-cycle control issue. Most of them can be described as protocol-based. In synchronous networks, a global reference clock is maintained on each node throughout the network. With a global clock, the protocol can assign communication timeslots to each node. The drawback of this solution is that it may be difficult to maintain and distribute the clock in an ad-hoc network where nodes may be joining and leaving the network. In addition, the energy used to distribute and maintain synchronization can be significant. Another type of protocol-based duty-cycle control, which avoids a global time reference, is pseudo-asynchronous "rendezvous". Depending on the protocol, communication may be initiated by either the transmitting node or the receiving one [18]. Figure 1.5 shows an example of a transmitter-initiated protocol. A timer is used to activate the receiver periodically in order to monitor the channel for communication. If no signal is received, the node returns to sleep mode. When the transmitting node wants to initiate communication it repeatedly sends requests, or beacons, until the receiver wakes up and hears the request, at this time data can be exchanged. Although this method avoids the need for time synchronization between the two nodes, significant energy may be expended both by the receiver (monitoring) and the transmitter (beaconing). More importantly, there is an inherent trade-off between average power consumption and network latency. In order to reduce latency, the protocol must be adjusted for the receiving node to monitor the channel more often, increasing duty-cycle and average power. An alternative to protocol-based duty-cycle control is based on asynchronous wake-up. This method adds an auxiliary receiver called a wake-up receiver (WuRx) to each node. Its only job is to continuously monitor the channel for communication requests or wake-up signals. As shown in Figure 1.6, the WuRx now effectively controls the duty-cycle based on actual communication requests, taking the

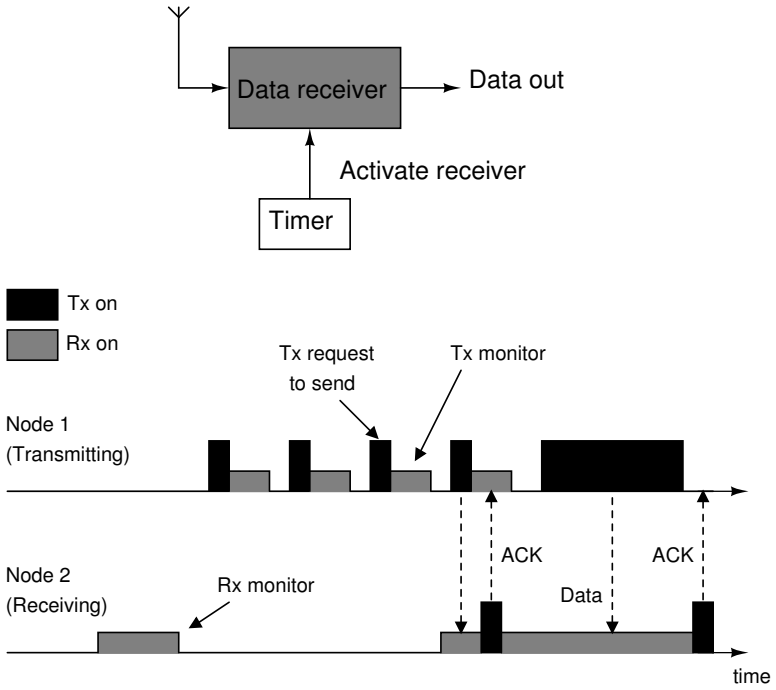


Figure 1.5: Protocol-based duty-cycle control: transmitter initiated

place of the timer used in protocol-based methods. The use of a wake-up receiver breaks the trade-off between latency and average power consumption described earlier. The WuRx can respond immediately to requests and so latency is effectively eliminated. The energy that was previously dedicated to repeated beaconing on the transmit side and periodic monitoring on the receive side is replaced by the power consumption of the WuRx. Because of the continuously monitoring of the channel by the WuRx, its active power consumption must be very low. Duty-cycle control based on asynchronous wake-up is an attractive alternative to protocol-based methods for many network scenarios, particularly those with low latency requirements. However, very few published wake-up receiver implementations exist in the literature. In [19], the authors extend the battery life of a personal digital assistant (PDA) by activating it only when an incoming request is received. An IEEE 802.11b wireless LAN transceiver is used for data communications in this prototype, while the wake-up receiver is implemented with a commercial off-the-shelf receiver module consuming about 7 mW in receive mode.

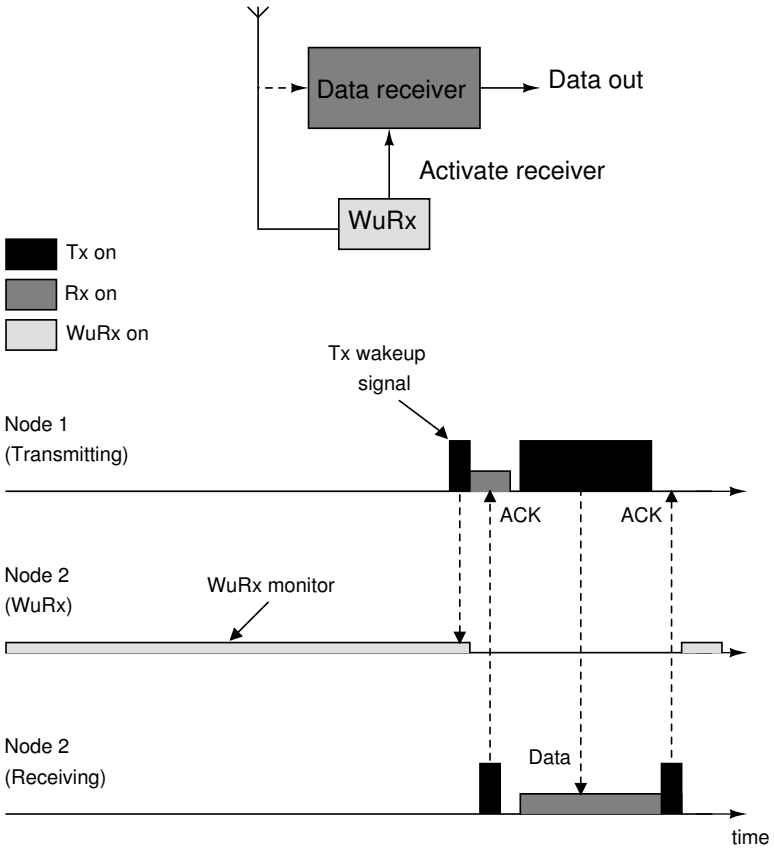


Figure 1.6: Duty-cycle control with wake-up receiver

1.3.3 Low-power Design Strategies

Battery life-time is an important performance metric for many wireless networks. In WSN applications for example, there is a growing need to extend the life-time of the network and, as discussed before, energy scavenging techniques and duty-cycle control help to reach this goal. However, this is one part of the solution and a deep investigation on radio communication module (*cf.* section 1.1) of sensor nodes is mandatory to see where we can attack the power consumption problem. A proper architectural choice is crucial to obtain good levels of performance, costs and power dissipation. Nevertheless, it is only the first step towards the design optimization, which can be reached only by proper choices down to transistor level. Within communication module's blocks, radio-frequency ones are the most promising for power and area saving since they are more expensive and

power-hungry than low-frequency parts. Therefore, much effort in optimization process is paid to RF blocks. In this section several design approaches are discussed, in order to find the most effective area and power minimizing strategies proposed in the litterature. To illustrate this purpose some selected examples from the state-of-the-art are reported and described in this section. The proposed architectures specifically highlight the tradeoff between silicon saving and the optimization of power consumption. Figure 1.7 shows a direct conversion receiver architecture proposed in [1]. Since the frequency synthesizer is the most power-hungry block in a receiver front-end, reducing its power consumption results in a large saving on the whole receiver power dissipation. Therefore, the proposed solution reduces the working frequency to save power. In a conventional direct conversion

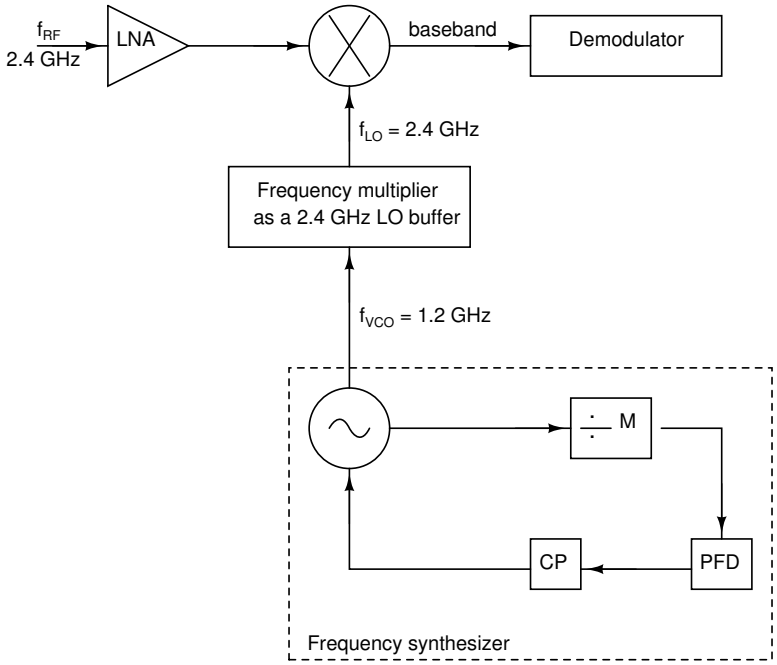


Figure 1.7: Direct conversion receiver proposed in [1]

receiver, the RF input signal and LO frequencies are equal, which allows the translation of the input to DC. In this architecture, the generated LO frequency is halved respect to the RF signal; the frequency synthesizer is then processed by a frequency multiplier to generate the desired RF frequency for direct conversion. Thus, both voltage controlled

oscillator (VCO) and the frequency divider work at 1.2 GHz instead of 2.4 GHz, resulting in power saving. This is obtained at the cost of a phase noise worsening, which is anyway maintained in an acceptable range for the application. Power reduction is also obtained thanks to the buffering effect of the frequency multiplier avoiding the need to introduce power-hungry buffers. In this solution, the power optimization is obtained by increasing costs, since two integrated coils are required to generate the desired LO frequency. Another way to minimize power consumption is to reduce both, bias current and voltage supply. The approach proposed in [2] focuses mainly on voltage supply minimization. The architecture reported in Figure 1.8 is based on a passive and differential front-end in order to increase the available voltage swing and to have a good noise figure (NF) and linearity at minimum power. In order to reduce the number of inductors and therefore

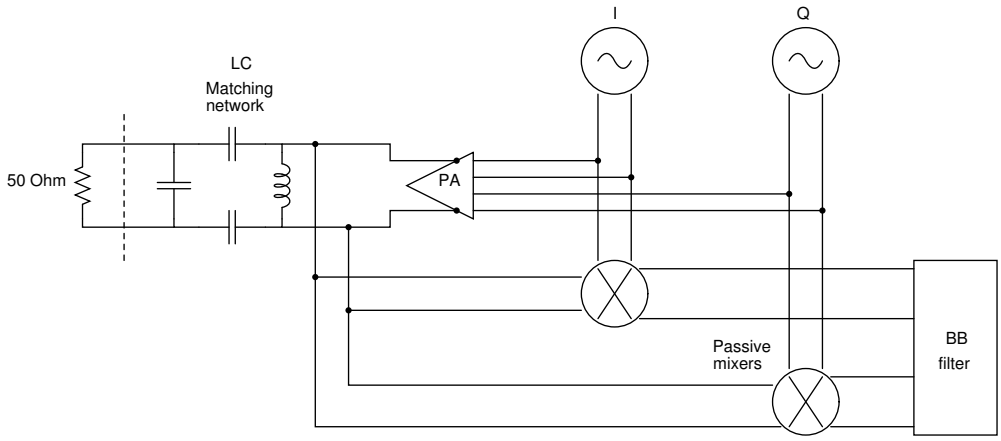


Figure 1.8: Block diagram of the proposed transceiver in [2]

the silicon area, the antenna matching network is shared between the transmitter and the receiver. This network, which introduces a passive gain, replaces the traditional LNA, resulting in power saving. Quadrature generation is provided by a back-gate quadrature VCO. This technique reduces power consumption in comparison with the conventional cross-coupling quadrature generation [20]. In transmit mode, the PA and mixer are driven from the high quality factor LC tank of the VCO without buffering and the whole differential VCO output swing is amplified. This design choice helps to reduce power consumption and to improve performances. Avoiding quadrature generation at LO path

is an efficient approach to reduce at the same time power dissipation and cost. Exploiting this design technique, [3] proposes a low-IF architecture with direct VCO modulation transmitter. The block diagram of the transceiver is depicted in Figure 1.9. The proposed

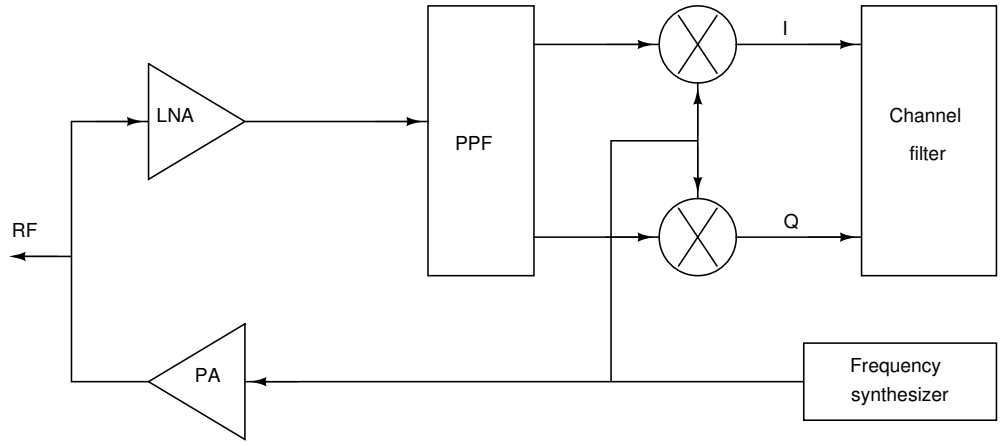


Figure 1.9: Proposed transceiver in [3]

architecture utilizes a single oscillator signal and generates the quadrature signals in RF path, where the low-noise amplified signal is split into I and Q components using a passive 2 stage poly-phase-filter (PPF). The down-conversion mixer can be implemented as a passive switching device, lowering not only the power consumption but also the flicker noise in comparison with a Gilbert cell. Thus, the only power consuming element of the receiver front-end is the LNA, which has also to compensate losses introduced by the poly-phase-filter and mixer. The proposed LNA is composed by two stacked stages, sharing the bias current and boosting the gain. Concerning the transmitter, the VCO frequency modulation is performed within the loop. This allows to amplify the modulated signal without any mixing and low-pass filtering needed, which helps to reduce power consumption. In addition, the constant envelope frequency modulation allows to maximize the PA efficiency. In this design strategy, power minimization is reached by using a single VCO and generation quandrature in the RF path. This choice requires a careful design of the LNA, where power consumption can be minimized exploiting the bias sharing technique. In conclusion, even if the power and area minimization require

a careful choice of the transceiver architecture, they can be reached only by combining this choice with proper design strategies. As shown in the state of the art overview, cost minimization requires to reduce the number of integrated coils and external components. This can be obtained by *e.g.* sharing the matching network and the oscillator between the transmitter and the receiver. Nevertheless, the most promising solution to save power consumption seems to be bias and device sharing. A careful choice of the operating region for transistors is necessary in order to capture both RF performances and current effieciency [21]. Another promising approach to further reduce power consumption is to merge functionalities in RF building blocks [22]. This attractive way helps to maximize the power saving while maintaining a good flexibility, which can be exploited to optimize the design and reach a good trade-off between power dissipation and system performances. Since the RF transceiver requirements in WSN are quite relaxed in comparison with other wireless networks, they can be satisfied by designing mere circuits and systems. The need for complex architectures, to demodulate the RF signal, is no longer necessary and new topologies could be imagined to directly extract the useful information. One can imagine the early times of radio receivers with envelope detection module to demodulate AM signals. These systems could be implemented in wireless sensor networks thanks to their simplicity. This approach will be further detailed and discussed in chapter 3.

1.4 Thesis organization

This chapter proposes a brief on wireless sensor networks backgrounds. Requirements on system and radio-frequency transceivers are presented with a special focus on power consumption of radio communication module. Challenges related to energy constraints and duty-cycle control in sensor networks are discussed. The main goal of this research is to present solutions at circuit and system levels which help the design and implementation of an ultra-low power receiver for WSN. Chapter 2 introduces some design methodologies dedicated to reduce the power consumption at building block level. Two circuits a mixer and a mixer-VCO, namely Self-Oscillating Mixer (SOM), are presented to illustrate the techniques. Chapter 3 describes the design and implementation of a receiver demodulator

using a novel architecture to extract useful information from a RF signal. This system level solution is compatible with basic modulation schemes namely phase modulation, frequency modulation and amplitude modulation. Finally, Chapter 4 concludes with a brief summary of results and discussion of future research directions.

Chapter 2

Circuit Approach

This chapter introduces design methodologies to reduce power consumption in RF circuits. First, techniques to reduce power consumption are discussed. Since they do not correspond all the time to low voltage operation, approaches for lowering supply voltage are also proposed. In order to implement these techniques, a mixer and a self-oscillating mixer were carried out in a 130 nm *and* 65 nm *CMOS process respectively.*

2.1 Analog Techniques for low power/low supply voltage RF design

Standard CMOS technology has become prevalent in analog and RF circuit design mainly due to the low production cost and potential for integration with accompanying digital circuits. As outlined in chapter 1, cost and integration are two essential considerations in the design of circuits for wireless sensor networks. Thus, scaled sub-micron CMOS technology is a natural choice for implementation of these circuits. In addition, deep sub-micron CMOS opens up new frontiers in low voltage and current circuit design. In this section, design techniques are outlined to fully explore the advantages of modern CMOS devices and achieve minimal power consumption for RF circuits.

2.1.1 Circuit Configurations

Although CMOS scaling has been extremely beneficial for digital circuits, analog circuits have often been hindered by these advances. One of the most difficult problems is the constantly diminishing supply voltage for modern CMOS processes, causing reduced voltage headroom and dynamic range for analog and RF applications. Figure 2.1 shows projected trends in CMOS supply voltage scaling over the next 6 years, as predicted by the International Technology Roadmap for Semiconductors (ITRS) [23]. Scaling trends are shown for three different digital technology targets. The low power operation digital roadmap is the most aggressive, since supply voltage scaling is one of the main strategies for reducing power consumption in digital circuits [24]. Trends for high performance and low standby power designs lag by several generations, but are also expected to experience supply voltage scaling below 1 V in the next six years. These digital roadmaps are an important indicator for the state of future analog designs because digital performance drives technology scaling. In order to reap the cost benefits of integration, analog and RF designs must conform to the specifications of digital technologies. One common strategy for dealing with reduced voltage in analog designs is to use special analog process options or high voltage I/O devices for the analog portions of the design. Though effective, this solution raises cost and increases power usage of the analog block. It is clear that future analog and RF designs will be subjected to ever more stringent supply voltage constraints. In many cases, however, it may be feasible to embrace this trend and reduce the supply voltage as low as possible as a means of achieving minimum power consumption. For low power designs, the minimum bias current is usually determined by the required circuit performances and cannot be arbitrarily reduced. On the other hand, the supply voltage is usually set at a standard value that may not be optimal for the design. If the current levels are optimized, the technique of reducing the supply voltage may result in additional power savings. In the following, possible opportunities for low voltage RF design are discussed.

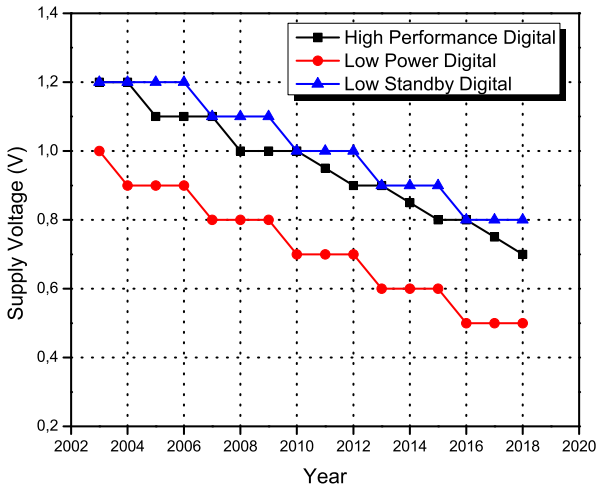


Figure 2.1: ITRS projections for CMOS supply voltage scaling

The Cascode and Folded Topologies

The cascode configuration is widely used in the design of CMOS RFICs thanks to its reasonable high-frequency characteristics in terms of gain, output impedance and reverse isolation. Figure 2.2 shows a simplified illustration of a cascode stage with its principles of operation in dc and ac conditions [25]. With a stacked architecture, the dc bias current is shared by the two active devices of the same type, which is advantageous as far as power consumption is concerned. However, if both of the metal-oxide-semiconductor (MOS) transistors are operating in saturation, a supply voltage of at least twice of the transistor's overdrive (V_{GS} - V_{TH}) is required. Typically, the RF performance of a cascode stage degrades significantly as the supply voltage decreases, making it less attractive for low-voltage circuit operations. To alleviate the stringent limitations on the supply voltage, a folded cascode configuration in classical analog circuit design has been adopted by many RF designers. The idea of folded cascade is to decouple the ac and dc paths of the circuit. A simplified illustration is depicted in Figure 2.3 where a decoupling capacitor and two RF chokes are employed. As the equivalent impedance provided by the RF chokes is sufficiently large and the decoupling capacitor is considered as a short circuit at

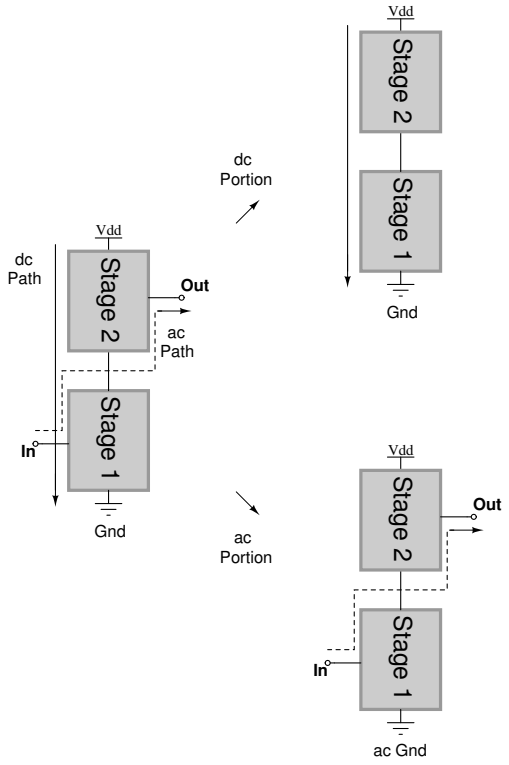


Figure 2.2: A conceptual illustration of the cascode architecture

the frequencies of interest, the ac signal path of the folded cascode stage is identical to that of a conventional one. On the other hand, as indicated in Figure 2.3, the dc voltages and bias currents of the two stages are virtually independent. Therefore, the required supply voltage can be effectively reduced at the cost of higher current consumption while maintaining the desirable performance of the RFICs.

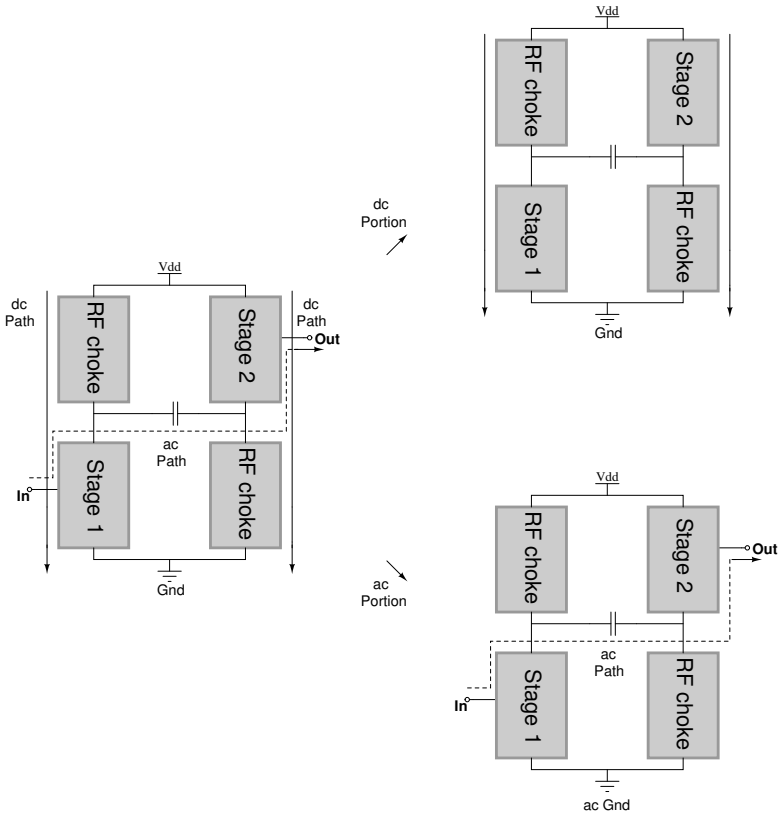


Figure 2.3: A conceptual illustration of the folded cascode architecture

Complementary Current Reuse Technique

As indicated in the previous section, the folded cascode topology trades dc power for supply voltage. To achieve low-voltage and low-power circuit operations at the same time, a complementary current-reuse technique is proposed in [26] with circuit example and design guidelines for down-conversion mixers. A conceptual illustration of a down-conversion mixer using the current-reuse technique is shown in Figure 2.4, where the

transconductance stage M_N performs the voltage-to-current conversion of the RF input signal, small-signal current is then directed to the source of the PMOS differential pair through capacitor C_1. The commutating stage (M_{P1}, M_{P2}) provides frequency down-conversion since it is driven by local oscillator (LO) with sufficient swings. Resistor R_1 is employed to provide a bypass current path such that large load resistance R_L can be used to boost the conversion gain without introducing excessive voltage drop.

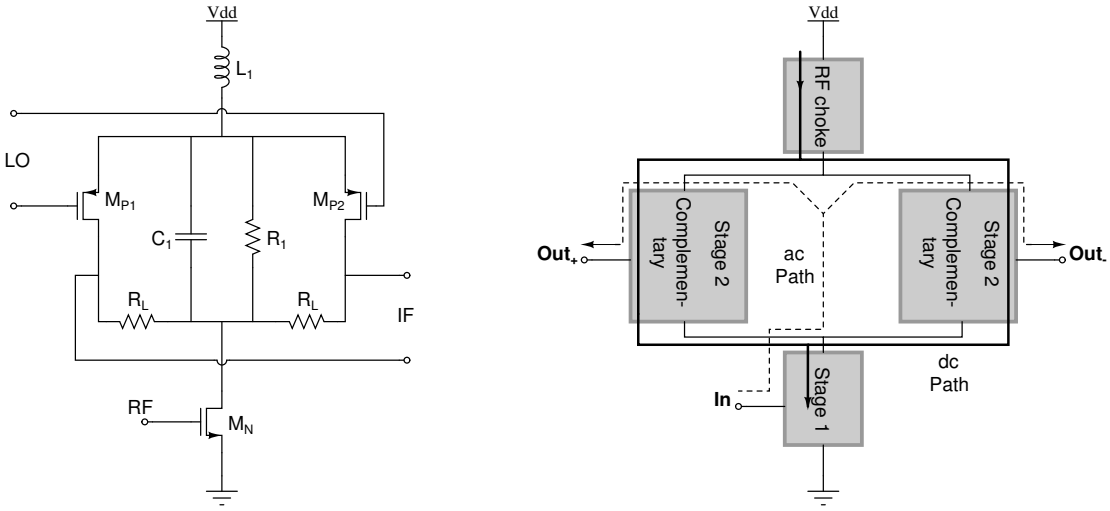


Figure 2.4: The complementary current-reused mixer with a current-bleeding technique

2.1.2 Transistor Biasing

Forward-body Bias Technique

In the design of CMOS RFICs for low-voltage operations, the threshold voltage of the MOSFETs is considered one of the fundamental limitations for the supply voltage. For circuits in which the active devices are always on, it is desirable to have transistors with a reduced threshold voltage. For the CMOS process technology, the option of multiple threshold voltages is typically realized by adjusting the thickness of the gate oxide or the doping profile in the channel. However, this complicates the fabrication process and requires higher implementation cost. Alternatively, the threshold voltage can be manipulated by the bias voltage at the body terminal. Taking the n-channel MOSFET

as an example, the threshold voltage is given by:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \tag{2.1}$$

Where V_{SB} is the source-to-body voltage, V_{TH0} is the threshold voltage for $V_{SB} = 0$, γ is a process-dependent parameter, and ϕ_F is a semiconductor parameter with a typical value in the range of 0.3-0.4 V. In a triple-well CMOS technology, the simplified cross-sectional view of a NMOS device is given in Figure 2.5 to demonstrate the forward-body bias technique (FBB). By raising the dc voltage V_B at the body terminal, the value of V_{SB} becomes negative, leading to a decrease in the effective threshold voltage and therefore a control on the transistor current as it is shown on Figure 2.6.

As forward body bias is directly applied to p-n junction between the source and the

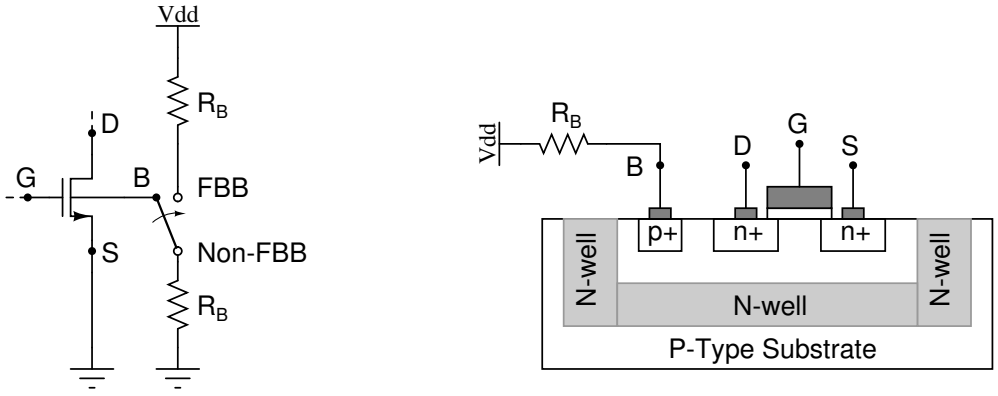


Figure 2.5: Forward-body bias technique

body, a current-limiting resistance R_B is typically included in the series path to prevent excessive current conduction, which may cause latch-up failure in CMOS circuitry. A special care must also be taken into account regarding the applied amount of V_{SB}, since a large source to bulk voltage may trigger CMOS latch up. The FBB is limited by the subthreshold leakage current and the forward biasing of the drain-bulk junction. According to [27] and [28], the upper limit of the FBB voltage for latch-up free operation, in 65 nm CMOS technology with V_{DD} ranges from 0.9 to 1.2 V, is 0.6 V.

Figure 2.7 shows the threshold voltage versus back-gate forward bias for NMOS transistor in 65 nm CMOS process. It can be clearly seen that an increase in the back-

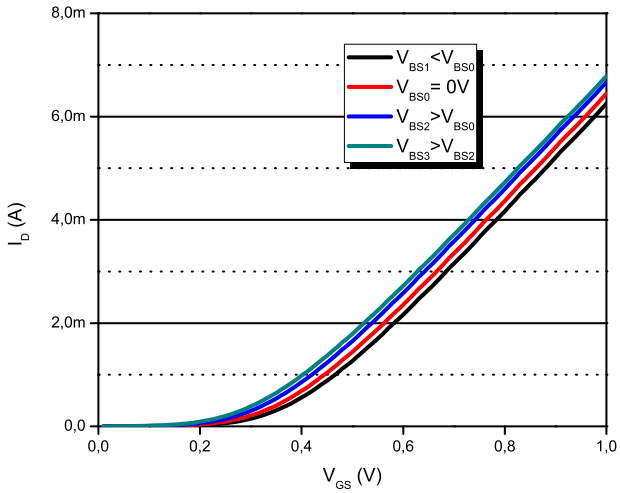


Figure 2.6: Transistor drain current for different bulk-source voltages, 130 nm CMOS process

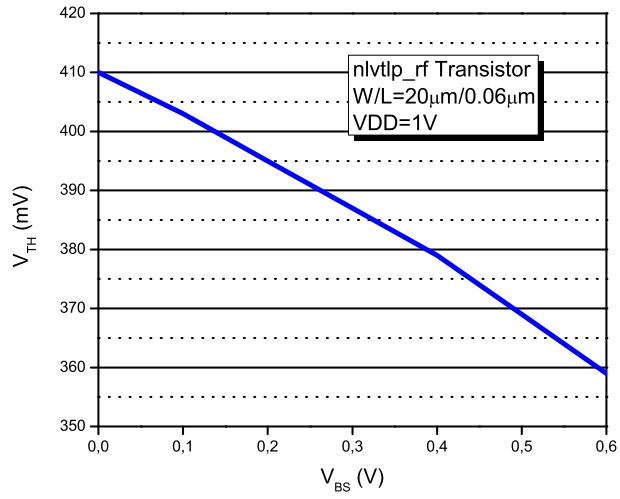


Figure 2.7: Threshold voltage versus V_{BS} for NMOS transistor in 65nm process

gate forward bias from 0 V to 0.6 V can lower the threshold voltage from 0.41 V to 0.36 V, which correspond to a reduction of 12 %. Therefore, the circuit power supply voltage could be lowered by the same proportion.

Subthreshold Operation

The main interest in transistor effect is the transconductance operation, which converts an input AC voltage into an output AC current. Hence, the transconductance g_m is the first and most important analog parameter of a transistor. The transconductance efficiency, rating the g_m to the drain current, is a figure of merit exploited in the design of low power analog circuits. Its maximum occurs in subthreshold operation of MOS device as depicted in Figure 2.8. In RF domain, the performances of a circuit are often correlated to the maximum of the cutoff frequency, f_T, defined as:

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.2}$$

where g_m is the small-signal transconductance and C_{gs} and C_{gd} represent the gate-source and gate-drain capacitances, respectively. Figure 2.8 figures out that the f_T is maximum when the transistor operates in strong inversion region (SI), which in turn corresponds to a weak transconductance efficiency.

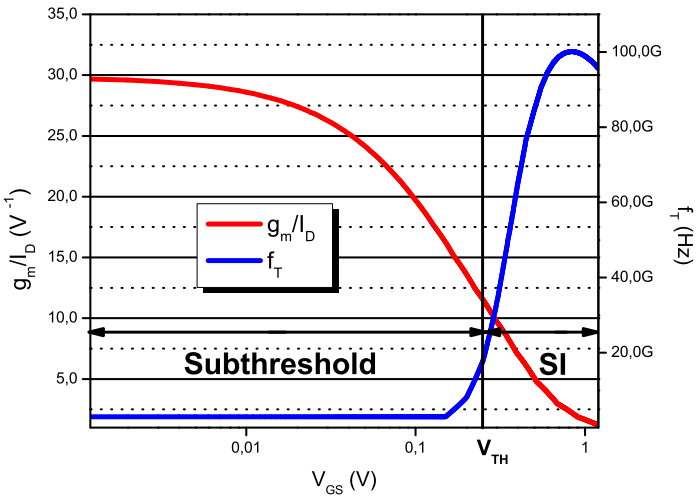


Figure 2.8: g_m/I_D and f_T for a modern CMOS 130 nm process

Technology Scaling

It is clear that MOS device exhibits a maximum of f_T in strong inversion region which is more suitable for high frequency applications. Operating in weak inversion region increases the transconductance efficiency but it comes at the expense of lower device f_T. However, with scaling down technology, cutoff frequency is increased for all regions of operation and it is no longer necessary to bias devices for the highest possible f_T. This trend is depicted in Figure 2.9 which represents the cutoff frequency of 3 different CMOS generations: 130 nm, 65 nm and 28 nm. For a zero overdrive bias (V_{GS}-V_{TH}=0 V), the 130 nm process achieves a f_T of 32 GHz, whereas the 65 nm and 28 nm nodes achieve respectively 50 GHz and 90 GHz of f_T. Hence the increased bandwidth induced

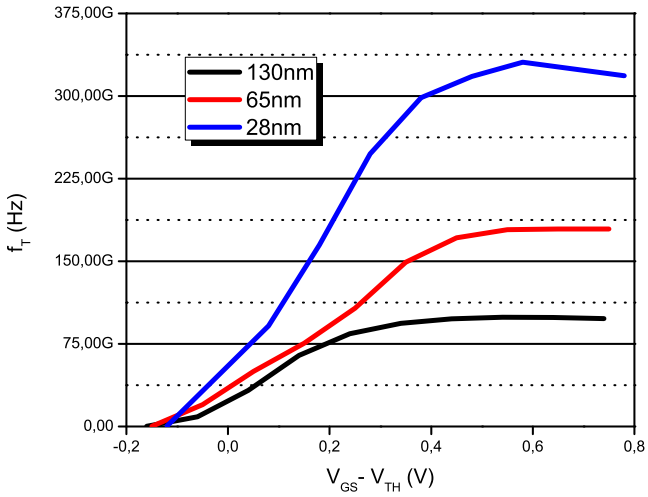


Figure 2.9: Comparison of f_T with technology scaling

by technology scaling will alleviate the problem of low f_T in subthreshold region. As consequences more and more RF circuits would operate with transistors biased in WI and MI modes experiencing technology scaling.

Transistor Metrics for Low Power RF

One of the main limitations in the Ultra-Low Power CMOS RFIC design is the low value of transistor's transconductance, g_m, due to the low bias current. As discussed previously, an effective way of minimizing power consumption is to bias the transistor in weak inversion region where the transistor achieves a maximum value of g_m/I_D, however, it exhibits a minimum cutoff frequency f_T. This approach is extensively used in analog circuit design whose the operating frequency is far from f_T. In RFIC design the effect of parasitic, such as C_{gs} in a MOS transistor, is of major importance. This phenomenon represented by f_T plays a key role in the optimization of RF building blocks. To capture both RF performances and DC power consumption of a MOS transistor in any region of operation, [21] introduces a new figure of merit (FoM), the $g_m f_T$-to-current ratio ($g_m f_T/I_D$). By taking into account both g_m and f_T, maximizing the $g_m f_T/I_D$ for a fixed bias current leads to the maximum achievable gain-bandwidth-product (GBW). This unique attribute makes the $g_m f_T/I_D$ a proper objective function for the optimization of the ULP RF and analog circuits. As shown in Figure 2.10, this new figure of merit

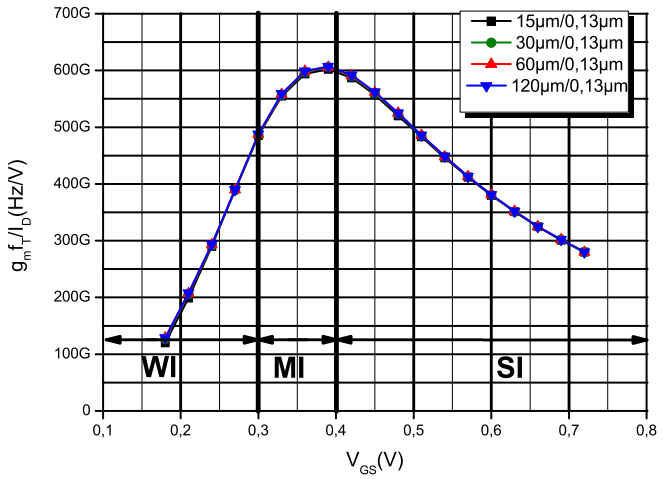


Figure 2.10: $g_m f_T/I_D$ for various transistor sizes for a modern CMOS 130 nm process

reaches its maximum in moderate inversion (MI) region, a transition area between weak inversion (WI) region, maximum of g_m/I_D, and strong inversion (SI) region, maximum

of f_T. It can also be noticed that the $g_m f_T/I_D$ ratio is independent of the transistor size for a given technology node. We will further reference the regions of MOS operation according to Table 2.1. U_t representing the thermal voltage (kT/q).

Table 2.1: Operating regions of the MOS transistor

Region of operation	Voltage
Strong Inversion (SI)	$V_{GS}>V_{TH}+4U_t$
Moderate Inversion (MI)	V_{TH}-$4U_t<V_{GS}<V_{TH}+4U_t$
Weak Inversion (WI)	$V_{GS}<V_{TH}$-$4U_t$

After investigating the advantages and disadvantages of subthreshold operation in this section, it appears that moderate inversion is an attractive compromise between the speed of strong inversion and the transconductance efficiency of weak inversion. In current technologies, moderate inversion is a realistic target for the realization of RF circuits. Moderate inversion also benefits from lower electric fields in the device, avoiding high field effects that degrade performance and reliability [29]. In this section, design approaches exploiting low supply voltage/low power techniques and subthreshold biasing were presented and motivated. First, circuit configurations aspects were discussed. Folded topology is suitable for low supply voltage operation, however, to achieve low-voltage and low power circuits at the same time, current reuse technique is more attractive. To further reduce power consumption, transistor biasing was also investigated to choose the optimized region of operation. So, in order to obtain RF performances and low power consumption, a new figure of merit was introduced, this latter includes the transconductance efficiency and cutoff frequency as $g_m f_T$-to-current ratio ($g_m f_T/I_D$) and it reaches a maximum in moderate inversion region. Therefore, a moderately inverted transistor seems to be an obvious choice for ultra low power circuits. Finally, equipped with these low power design methods; a mixer and a self-oscillating mixer are designed in the next sections to investigate these techniques.

2.2 Ultra-Low Power 2.4 GHz Down Conversion Mixer

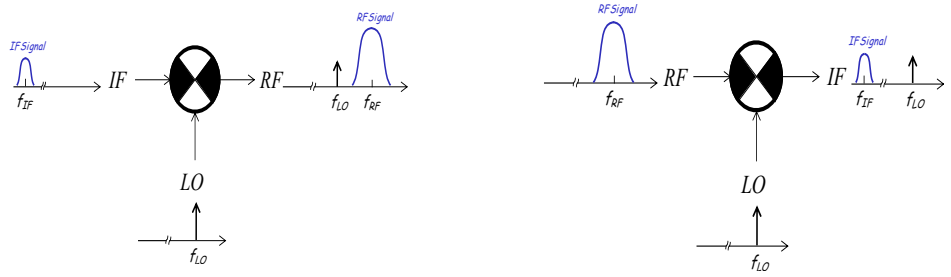
In this section we will detail the first approach of this thesis, the optimized biasing approach. The technique is applied to a mixer to further reduce its power consumption. First, mixer backgrounds are detailed. Then, the design of the circuit is discussed and finally, post-layout simulations are presented.

2.2.1 CMOS Mixer Fundamentals

The mixer is an essential building block in RF front-ends since it generates the frequency shift:

- In emitters, it upconverts a baseband signal to a useful signal at high frequencies, to take advantage of favorable propagation condition [30]. In this case, they are called up-conversion mixers, Figure 2.11a.
- In receivers, it translates an incoming RF signal to an Intermediate Frequency (IF), namely the down-conversion operation, for efficient demodulation [30]. Figure 2.11b.

  Conversion process in time domain is performed by multiplying the RF signal by local oscillator (LO) signal.



(a) Up conversion

(b) Down conversion

Figure 2.11: Mixer principle

Active and Passive Mixers

There are two classes of mixers: active and passive mixers. Active architectures, providing a voltage gain, are preferred in Rx architectures. They contribute to

improve the sensitivity of the system by lowering the noise contribution of the baseband stage. In Tx part, the high linearity and low 1/f noise of a passive mixer make it a good alternative. The power gain is then reported to the Power Amplifier (PA).

Performance Metrics of Mixers

- **Conversion Gain**: The "voltage conversion gain" of a mixer is defined as the ratio of the rms voltage of the IF signal to the rms voltage of the RF signal. The "power conversion gain" of a mixer is defined as the IF power delivered to the load divided by the available RF power from the source (Eq 2.3). If the input impedance and the load impedance of the mixer are both equal to the source impedance, for example, $50\,\Omega$ as instance, then the voltage conversion gain (Eq 2.4) and power conversion gain of the mixer are equal when expressed in decibels.

$$CG_{power} = \frac{\text{Output power at IF}}{\text{RF available input power}} = \frac{V_{IF}^2/R_L}{V_{RF}^2/R_S} \tag{2.3}$$

$$CG_{voltage} = \frac{\text{IF output voltage (rms)}}{\text{RF input voltage (rms)}} \tag{2.4}$$

- **Noise Figure**: The noise figure is defined as the signal-to-noise ratio (SNR) at the input (RF) port divided by the SNR at the output (IF) port Eq 2.12.

$$NF_{dB} = 10\log(\frac{SNR_{RF}}{SNR_{IF}}) \tag{2.5}$$

  In a typical mixer, there are actually two frequencies that will generate a given intermediate frequency. One is the desired RF signal and the other is called the image signal as shown in Figure 2.12. The reason that two such frequencies exist is that the IF is simply the magnitude of the difference between the RF and LO frequencies. Hence, both signals above and below ω_{LO} at $(\omega_{LO} \pm \omega_{IF})$ will produce outputs at the same frequency ω_{IF}. The two input frequencies are therefore separated by $2\omega_{IF}$. In a heterodyne architecture, $f_{in} \neq f_{LO}$, the

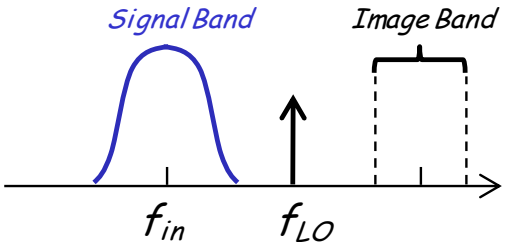


Figure 2.12: Image band

SNR_{out} is half of the SNR_{in} because the noise originating in both the desired and image frequencies are added in IF signal according to the illustration of Figure 2.13. In such a case, the NF is referred as Single Side Band (SSB). In a homodyne architecture, f_{in}=f_{LO}, there is no image frequency and the SNR_{in} is kept the same at IF. This situation is referenced as Double Side Band (DSB). In a mixer, the noise is also replicated and translated by each harmonic of

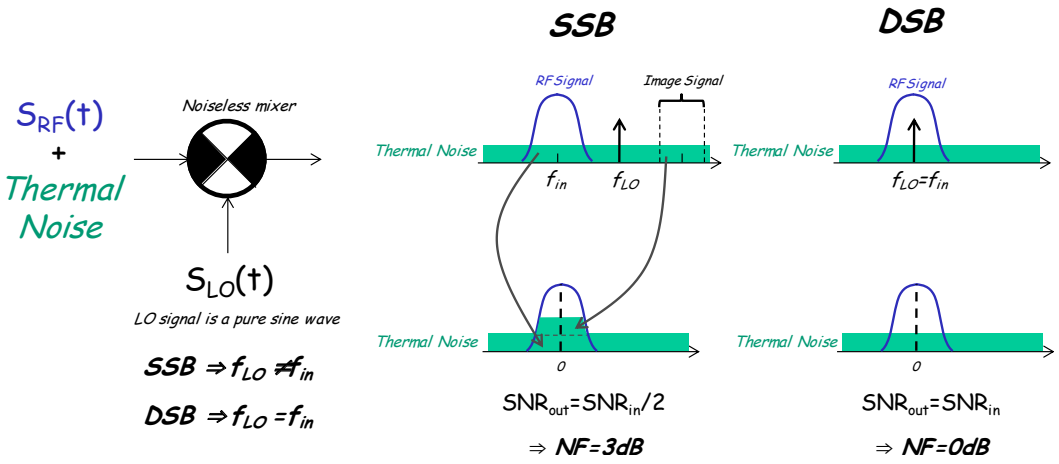


Figure 2.13: SSB and DSB noise figure

the LO, this mechanism is called "noise folding". Larger gain and lower noise contribution are produced by square LO signal [31]. Unfortunately, this latter generates harmonics and so "noise folding" as depicted in Figure 2.14.

– **Port-to-Port Isolation**: The principle of frequency shift which is a typical non linear operation makes the port to port isolation a critical parameter

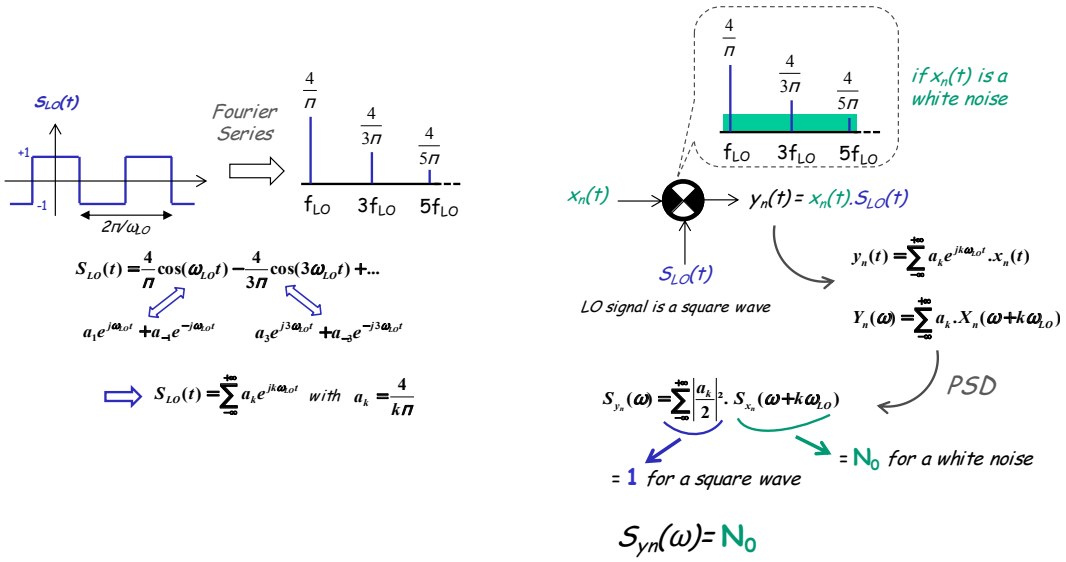


Figure 2.14: Noise folding mechanism

of RF mixers. The LO-RF feedthrough results in LO leakage to the LNA and eventually the antenna, whereas the RF-LO feedthrough allows strong interferers in the RF path to interact with the local oscillator driving the mixer. The LO-IF feedthrough allows substantial LO signal existing at the IF output which can desensitize the following stages and so the receiver. Finally, the RF-IF isolation determines what fraction of the signal in the RF path directly appears in the IF one, a critical issue with respect to the even-order distortion problem in homodyne receivers. The different port-to-port isolation are shown in Figure 2.15 and defined by the following equation:

$$Isolation_{i->j} = \frac{Power_i \mid_{@\ jport}}{Power_j \mid_{@\ iport}} \tag{2.6}$$

– **Mixer Linearity**: Mixer is inherently a nonlinear device. Whereas desired nonlinearities are necessary to produce the mixed signal, undesired nonlinearities may corrupt the desired IF signal. Ideally, we would like IF output to be proportional to the RF input signal amplitude. However, real mixers have some limit beyond which the output has a sublinear dependence on the

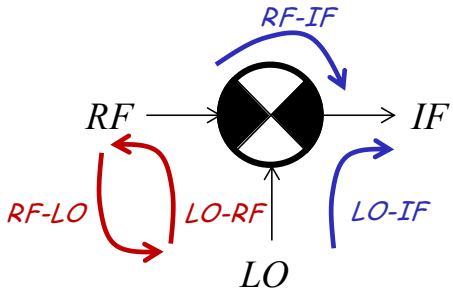


Figure 2.15: Different mixer isolations

input, 1 dB compression point ($P_{1\,\mathrm{dB}}$) is a way to measure this limit. Input $P_{1\,\mathrm{dB}}$ is the input power level that causes the mixer output to decrease from its linear magnitude response by 1 dB. In general, a mixer generates various cross-products of the RF and LO signal and their harmonics. The frequency of the resulting components can be expressed as $|m\omega_{RF} \pm n\omega_{LO}|$, where m and n are integers. A difficult task in receiver design is to ensure that, except for $|\omega_{LO} \pm \omega_{RF}|$, such components do not fall in the IF band. Owing to nonlinearities in the RF path, it is possible that harmonics of the interferers beat with harmonics of the LO thus corrupting the downconverted signal. The two-tone second-order and third-order intercept are used to characterize mixer linearity. A two-tone intermodulation (IM) test is a relevant way to evaluate mixer performance because it mimics the real-world scenario in which both a desired signal and a potential interferer (perhaps at a frequency just one channel away) feed a mixer input. The third-order intercept point is the extrapolated point where the fundamental and third-order intermodulation products (IM3) intersect each other. Figure 2.16 summarizes the different linearity performances of the mixer.

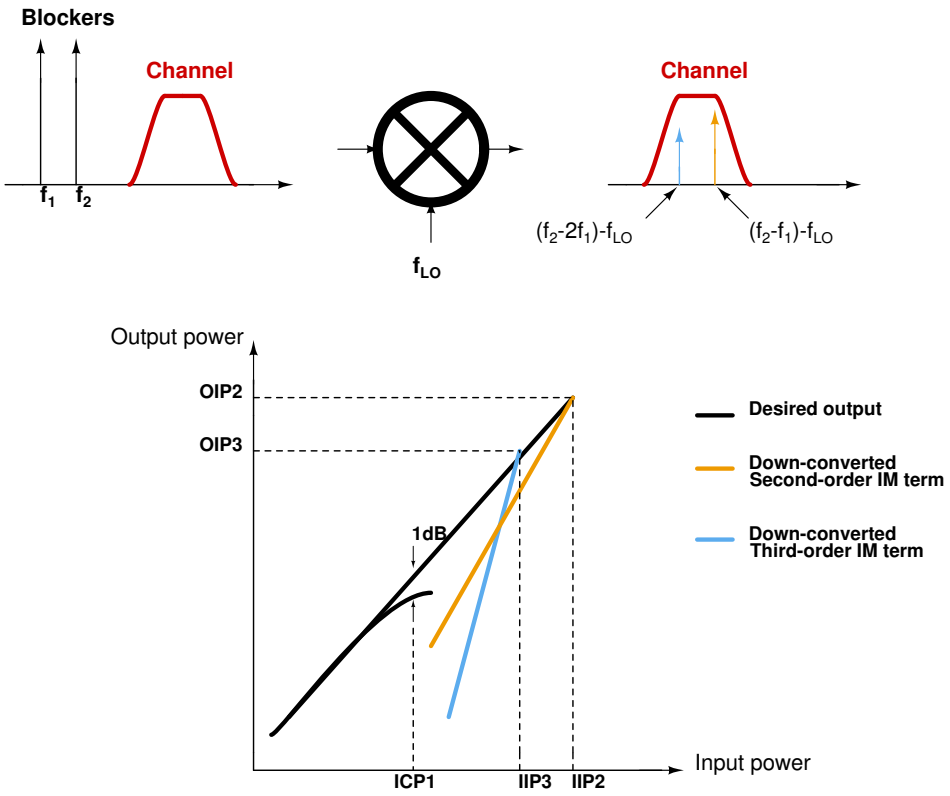


Figure 2.16: Mixer linearity mechanism

Single-balanced and Double-balanced Mixers

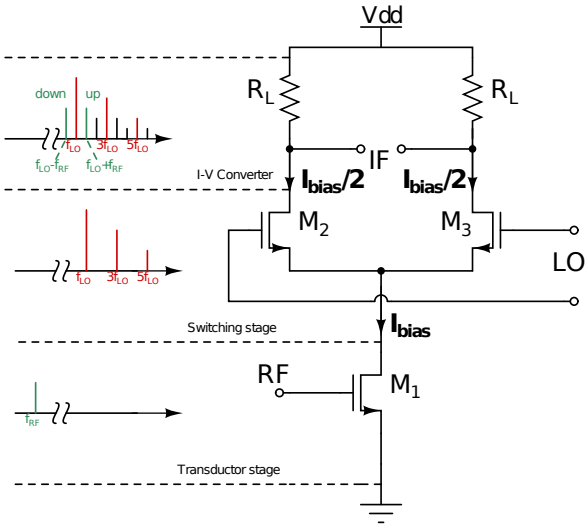
Due to the nonlinearity of mixing operation, many spurious can appear at the mixer output. As matter of consequences the topology choice is very important to attenuate this phenomenon. In Figure 2.17a, the single balanced topology -*i.e.* single RF with differential LO- exhibits some harmonics at f_{LO} in the IF spectrum. In Rx mode, these LO harmonics desensitize the receiver and so must be filtered. Its fully differential or fully balanced counterpart, Figure 2.17b, introduced by Barrie Gilbert [32], theoretically cancels both the LO and RF even order harmonics at the output. In practice, since the RF signal processed by the LNA (and possibly the image-reject filter) is usually single ended, one of the input terminals of the double-balanced mixer is simply connected to a bias voltage. This in turn creates different propagation times -*i.e.* phase shifts- for the two signal phases amplified by M_1 and M_2, leading to finite even-order distortion [33]. Conversion gain and noise figure for these two architectures are expressed in equations Eq 2.7, Eq 2.8 and Eq 2.9.

$$CG \approx \frac{2}{\pi} g_{m1,2} R_L \tag{2.7}$$

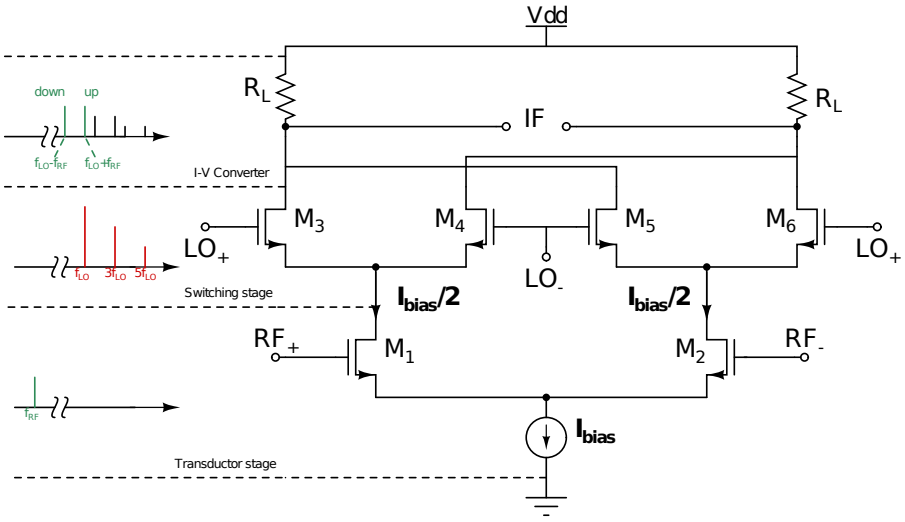
$$NF_{SB} \approx \frac{\pi^2}{4}\{1 + \frac{\gamma_1 g_{d01}}{g_{m1}^2 R_S} + \frac{2}{g_{m1}^2 R_L R_S}\} \tag{2.8}$$

$$NF_{DB} \approx \frac{\pi^2}{4}\{1 + \frac{2\gamma_1 g_{d01}}{g_{m1,2}^2 R_S} + \frac{2}{g_{m1}^2 R_L R_S}\} \tag{2.9}$$

where γ: Channel noise factor, g_{d0}: Open channel conductance and R_S=50 Ω. For a fixed power consumption, the two configurations achieve equal conversion gain but the single balanced architecture exhibits a lower input-referred noise. Double balanced architecture provides good isolation and do not suffer from LO-to-IF feedthrough, however, it requires a balun to perform its differential input. This, degrades the noise figure of the front-end and adds more complexity. Therefore, a single balanced topology seems to be more suitable for an ultra-low power system.



(a) Single-balanced mixer

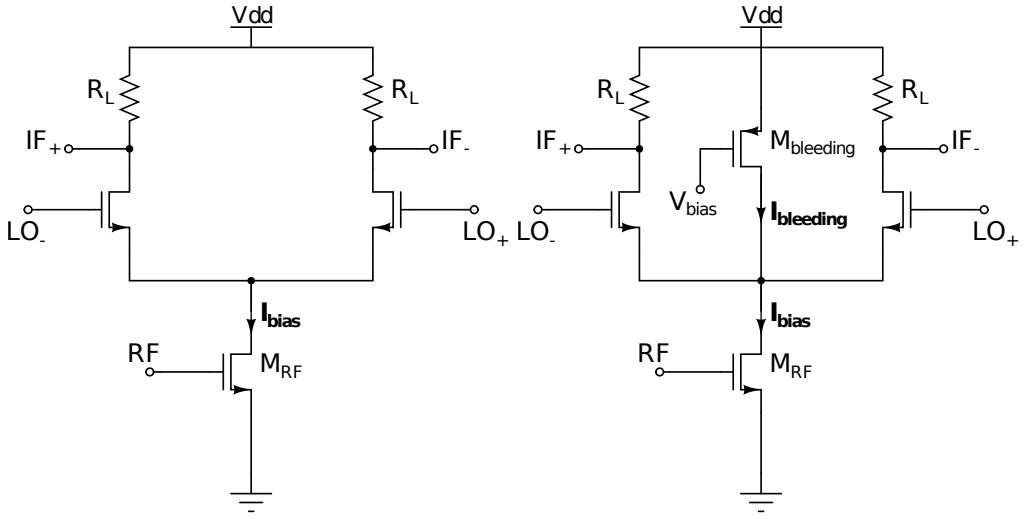


(b) Double-balanced mixer

Figure 2.17: Single-balanced and double-balanced mixers

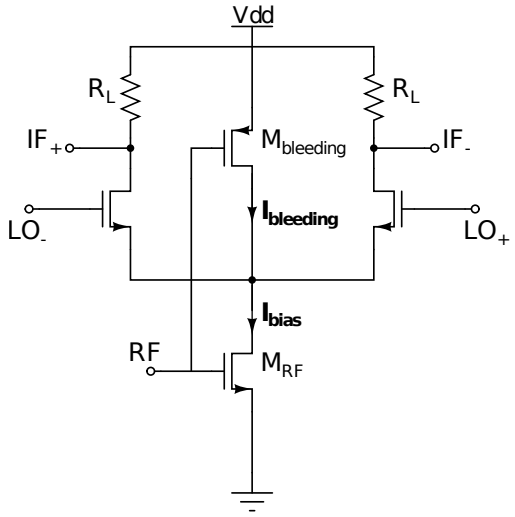
2.2.2 Topology Choice

Focusing on the design of a very low power down converter, the mixer topology is of single balanced type with differential output port. The current-reuse bleeding technique is exploited to further lower the noise figure and enhance the conversion gain of the mixer. An investigation of this technique is first presented in Figure 2.18 and then discussed.



(a) Current commuting mixer

(b) Bleeding mixer



(c) Current-reuse bleeding mixer

Figure 2.18: Various configurations of active mixers

The first configuration presented in Figure 2.18a is based on the conventional single balanced current-commuting mixer. In such structure, both the gain (Eq 2.10) and the linearity (Eq 2.11) are directly proportional to the amount of current flowing through the transconductance stage, I_{bias}. On the other hand, the noise figure (Eq 2.12) increases with I_{bias} for a fixed transconductance g_{mRF} [31] because of the noise induced by the switching pair and represented by the third term in Eq 2.12 according to [34].

$$VCG \approx \frac{2}{\pi} R_L \sqrt{K_n I_{bias}} \tag{2.10}$$

$$IIP_3 \approx 4\sqrt{\frac{2}{3}\frac{I_{bias}}{K_n}} \tag{2.11}$$

$$NF \approx 1 + \frac{\pi^2}{2g_{mRF}^2 R_L R_S} + \frac{\pi\gamma I_{bias}}{A g_{mRF}^2 R_S} + \frac{\gamma\pi^2}{4 g_{mRF} R_S} \tag{2.12}$$

where $K_n = \mu_n C_{ox}$(W/L) and A: LO amplitude. Hence, the transductor current (I_{bias}) needs to be enhanced without varying the switching current to improve the gain, the linearity and lower the noise figure in a conventional current commuting mixer. It is completed by the circuit of Figure 2.18b [35]. The principle is based on an additional current source, the bleeding transistor ($M_{bleeding}$), which steers the current pulled into the RF stage. By means, the DC current flowing into the switching pair is no longer controlled by the transductor stage. As well the tradeoff relying on the biasing current of the RF transistor is completely relaxed. The configuration of Figure 2.18b, can evolve to the topology of Figure 2.18c, which takes advantages of both bleeding and current-reuse techniques. The p-channel transistor ($M_{bleeding}$) is used as a bleeding current source and also contributes to the transconduction of the input signal. For a fixed current I_{bias}, the overall transconductance of the RF stage is no longer "g_{mRF}" but "$g_{mRF} + g_{mbleeding}$", with $g_{mbleeding}$ the transconductance of the transistor ($M_{bleeding}$). The first circuit developed in this thesis is based on this current-reuse bleeding configuration.

2.2.3 Circuit Design

The complete circuit design consists of both the mixer core and two buffers to drive the signal off-chip. It is implemented in a 130 nm CMOS technology from ST Microelectronics. The design of the down converting part and the buffer stage are reported in this section.

Mixer Core

The mixer core is based on current-reuse bleeding configuration as shown in Figure 2.19. The capacitor C_f is used to decouple the biasing of M_1 and M_4. Both transistors operate in moderate inversion region to maximize the $g_m f_T$ to drain current ratio.

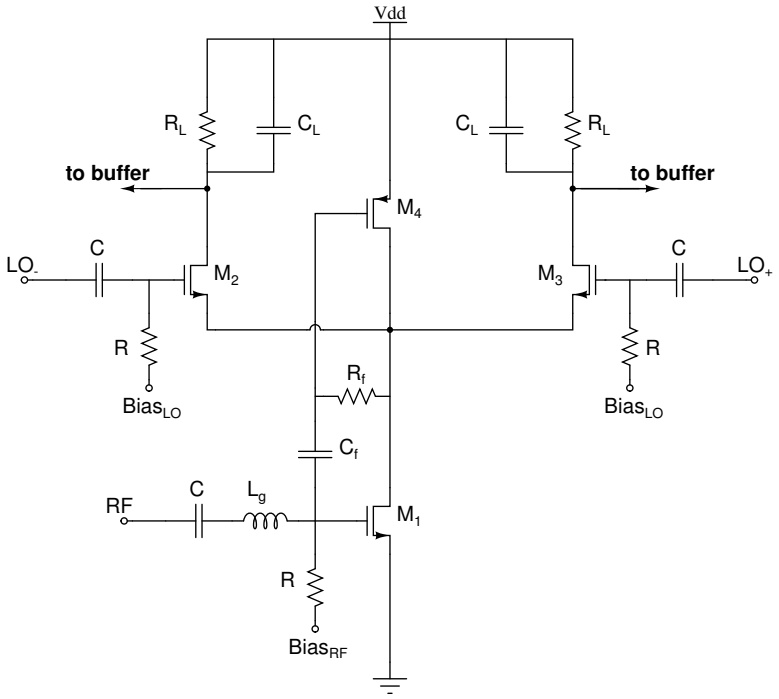


Figure 2.19: Circuitry of mixer core

The supply voltage V_{DD} is fixed to 0.8 V for a nominal operation. The core bias current is controlled by an external voltage, $Bias_{RF}$, applied to the gate

of M_1. At the mixer output, a low-pass filter (R_L, C_L) allows for a rejection of high frequency harmonics -*i.e.* RF and LO signals. The analytic expression of the noise figure, the input impedance and the voltage conversion gain are derived in Eq 2.13, Eq 2.14 and Eq 2.15.

$$NF \approx \frac{\pi^2}{4}\{1 + \frac{\gamma_1 g_{d01}}{g_{m1}^2 R_S} + \frac{\gamma_4 g_{d04}}{g_{m4}^2 R_S} + \frac{2}{g_{mT}^2 R_L R_S} + \frac{R_S}{R_f}\} \tag{2.13}$$

$$Z_{in} \approx \frac{C_0 R_f}{C_{gsT} + C_0} + j\{L_g\omega - \frac{g_{mT} R_f C_0}{(C_{gsT} + C_0)^2 \omega}\} \tag{2.14}$$

$$VCG \approx 2 g_{mT} \frac{R_L}{R_S} \sqrt{\frac{L_g}{C_{gs1}}} \tag{2.15}$$

with $g_{mT} = g_{m1}+g_{m4}$; $C_{gsT} = C_{gs1}+C_{gs4}$ and R_S=50 Ω.

The same current flows into M_1 and M_4, it is the bleeding technique, thus allowing the switching stage to act as a pure passive mixer. As a matter of consequences, the noise contribution of (M_2, M_3) can be neglected. The NF only accounts for the RF stage (M_1, M_4), resistive load R_L and the feedback resistor R_f in Eq 2.13. The resistor R_f, fifth term in Eq 2.13, needs to be as large as possible, with respect to the input matching conditions defined in Eq 2.14, to lower its noise contribution. C_0 models the capacitive loading effect of the switching stage (M_2, M_3) connected to the transductor stage (M_1, M_4). The imaginary part of the input impedance Z_{in} is cancelled by tuning L_g in Eq 2.14. R_f, in combination with C_{gsT} and C_0 adjusts the real part of Z_{in} to 50 Ω.

Output Buffer

Output buffers are necessary for measurement in order to drive instrumentation whose impedances are standardized to 50 Ω. An NMOS source follower topology (M_5, M_6) with current source (M_7, M_8) was chosen due its simplicity of output matching and wide frequency range of gain response. A schematic

of the output buffer is depicted in Figure 2.20. The transconductance of $M_{5,6}$ is close to 20 mS to ensure a low output return loss at IF frequency.

$$50\,\Omega = \frac{1}{g_{m5,6}} \Rightarrow g_{m5,6} = 20\,\text{mS} \tag{2.16}$$

The low-pass filter (R,C) reduces the noise contribution of the current mirror.

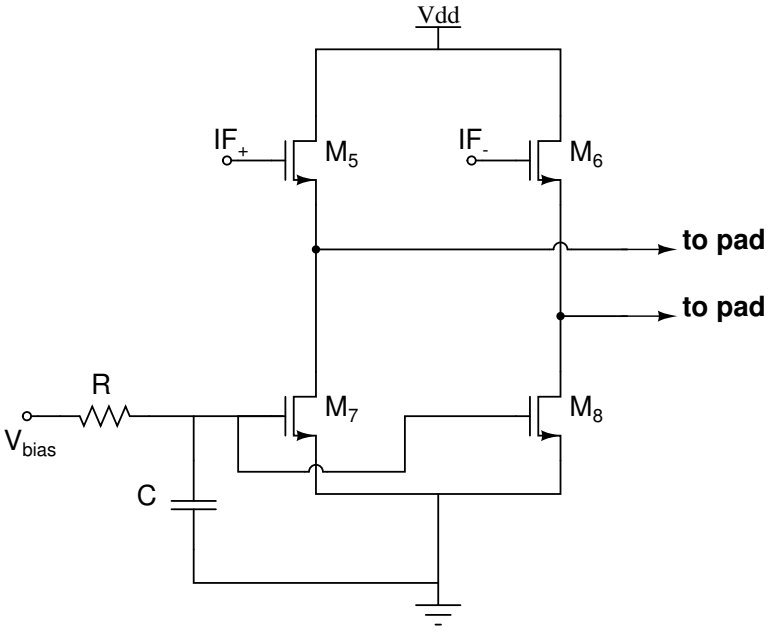


Figure 2.20: Schematic of the source followers

The buffer stage operates from a 0.8 V supply and consumes a total current of 2 mA. The final device types and aspect ratios are summarized in Table 2.2.

2.2.4 Layout and Post-layout Simulations

The final design has been realized in a 130 nm standard CMOS process with 6 metal layers from STMicroelectronics. In this design, the most sensitive parts are the switching pair (M_2, M_3) and the input matching path. The switching part is laid out in a common centroide configuration to make it immune from cross-chip gradients and the extracted parasitic are embedded in the input matching synthesis. The complete chip layout is shown in Figure 2.21. The

Table 2.2: Sizes of mixer devices

Device	Size	Device	Size
M_1(W/L)	14 µm/0.13 µm	C_f	10 pF
$M_{2,3}$(W/L)	6 µm/0.13 µm	C_L	2 pF
M_4(W/L)	24 µm/0.13 µm	L_g	12 nH
$M_{5,6}$(W/L)	120 µm/0.13 µm	R_L	2 KΩ
$M_{7,8}$(W/L)	30 µm/0.13 µm	R_f	5 KΩ
C	10 pF	R	5 KΩ

chip size is 0.745 mm^2 including all the pads. Empty space of the chip are filled by decoupling capacitors to filter out the variation of supply voltage. The proposed ULP mixer operates in 2.4 GHz ISM Band. The frequency

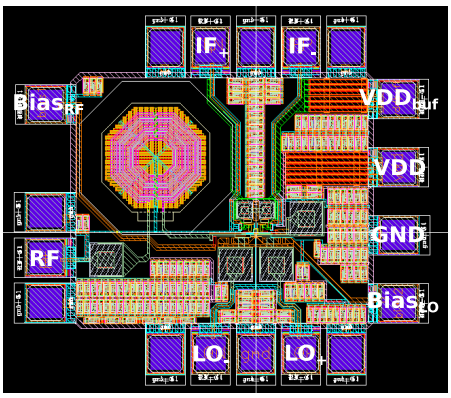


Figure 2.21: Snapshot of the mixer layout

plan used for simulations is: a 2.4 GHz RF signal, a 2.41 GHz LO signal and a 10 MHz IF intermediate frequency. The mixer core consumes 330 µW under 0.8 V supply voltage. $Bias_{RF}$ is set to 360 mV allowing transistor M_1 to operate in moderate inversion region. $Bias_{LO}$ sets the overdrive voltage (V_{GS}-V_{TH}) of the switching pair (M_2, M_3) to zero for an ideal switch. DC current flowing through M_1 and M_4 is 410 µA. Figure 2.22 shows the voltage

conversion gain and noise figure for various values of the feedback resistance R_f. Both characteristics improve with increasing R_f. The feedback resistance

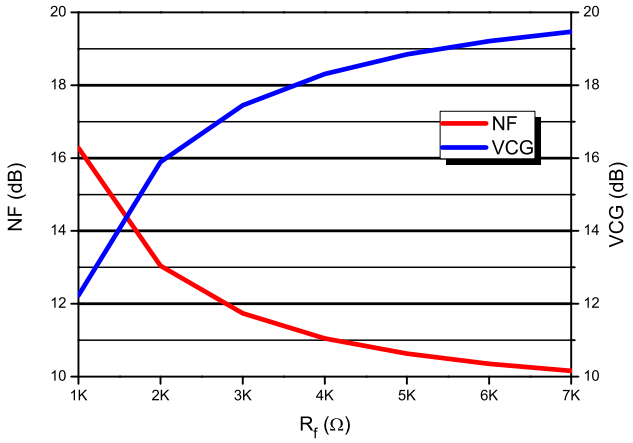


Figure 2.22: Simulated voltage conversion gain and SSB noise figure versus R_f at 10 MHz IF. LO power is -1 dBm

also contributes to tune the input matching of the mixer (Eq 2.14). Figure 2.23 illustrates the input return loss, S_{11}, versus R_f. A tradeoff has to be found between a good input matching (Figure 2.23), a large conversion gain (CG) and a low noise figure (NF) (Figure 2.22). Hence, R_f has been set to 5 KΩ in the implemented circuit. The voltage conversion gain (VCG) and the single side band noise figure (SSB NF) are reported versus LO power in Figure 2.24. Their optimum values obtained at a LO power of 5 dBm are 22.7 dB and 9.3 dB respectively. Considering a constrained power budget to address ultra low power applications, it is better suited to account for an LO power which does not exceed 0 dBm, typically -1 dBm. Under these conditions, VCG and SSB NF are 18.7 dB and 11.5 dB respectively.

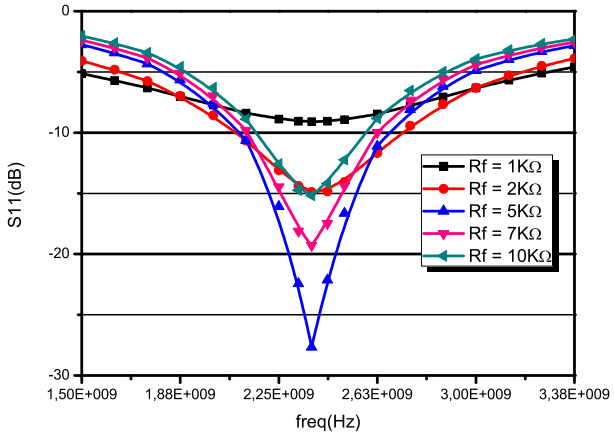


Figure 2.23: Input return loss S_{11} for various R_f

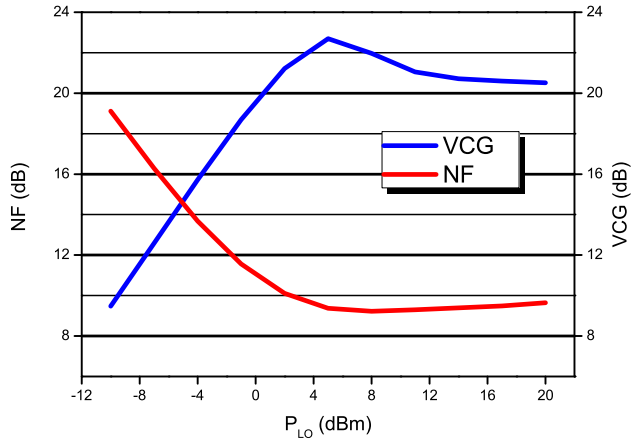


Figure 2.24: Simulated voltage conversion gain and SSB noise figure versus P_{LO} at 10 MHz IF

The single-tone 1 dB compression point and intermodulations are shown in Figure 2.25. The input referred 1 dB compression point (ICP1) is −21 dBm. The third-order intercept point (IIP3), −14.9 dBm, was tested by applying a two-tone large signal at 2.4 GHz and 2.401 GHz.

Table 2.3 summarizes the performances of the proposed circuit and various low

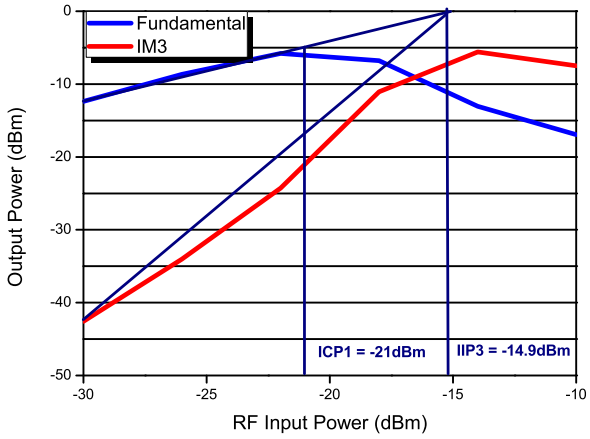


Figure 2.25: IIP3 and ICP1 of Mixer at 330 µW power consumption

power RF CMOS mixers from the literature. To compare them, we use the common figure of merit (FOM_{Mixer}) (Eq 2.17), which includes the conversion gain (Gain), noise figure (F), linearity (IIP3) and DC power consumption (P_{DC}):

$$FOM_{Mixer,linear} = \frac{Gain \times IIP3}{(F-1) \times P_{DC}(\text{mW})} \tag{2.17}$$

Table 2.3: Performance summary and comparison to other CMOS mixers

Ref.	Techology CMOS[nm]	RF [GHz]	IF [MHz]	P_{LO} [dBm]	VDD [V]	P_{DC} [mW]	Gain [dB]	NF [dB]	IP1dB [dBm]	IIP3 [dBm]	LO-RF [dB]	LO-IF [dB]	FOM [dB]
This work	**130**	**2.4**	**10**	**-1**	**0.8**	**0.33**	**18.7**	**11.5**	**-21**	**-14.9**	**28**	**43**	**-12.2**
[36]	130	2.4	60	-9	1	0.5	15.7	18.3	-28	-9	33	22	-16.3
[37]	130	2.5	10	-1	0.6	1.6	5.4	14.8	-9.2	-2.8	70.9	54.2	-16.8
[37]	130	2.5	10	-1	0.8	7.8	15	8.8	-16.9	-9.5	71.1	54.2	-19.1
[38]	180	2.4	1	-2	1	3.2	11.9	13.9	-	-3	-	-	-15.8
[39]	180	2.4	30	-2	1.8	1	32	8.5*	-	-14.5	60.5	-	-9.6
[40]	180	2.4	10	0	0.8	2	14.5	17.1	-22	-11	-	-	-23

*Double Side Band

It is not worthy the 3 best FOMMixer: this work, [38] and [39] bias the transistor in moderate inversion or close to the subthreshold voltage (V_{th}). This point figures out the interest in operating devices out of the Strong Inversion

(SI) mode, typically in WI or MI, to address very low power applications in advanced CMOS technologies. Considering a comparison between our post-layout simulations and the measurements of [38] and [39], the current reuse bleeding topology achieves the second best FOM with −12.2 dB and the lowest power consumption, under 330 µW.

2.3 Ultra-Low Power 2.4 GHz Self-Oscillating Mixer (SOM)

As discussed in the previous chapter, this section introduces the second approach of the thesis. To deal with wireless sensor networks requirements and further reduce the power consumption of RF front-end, the approach consists in merging the RF building blocks functionalities. Several options are possible, either combining the LNA and the mixer or merging the mixer and the local oscillator. [41], for example, combines the LNA and the mixer yielding to a Low Noise Converter (LNC). Compared with traditional cascaded LNA and mixer, this approach reduces the power consumption by removing the DC current path flowing into the LNA. Nevertheless, applying the RF signal to the mixer input with a low amplification, results in a low gain and a high NF which degrades the entire receiver performance. So, in this section we will focus on the study and design of Self-Oscillating Mixer (SOM). This option seems to be attractive since in an RF front-end, the local oscillator is the most power hungry building block.

2.3.1 CMOS LC Oscillators Background

Mixer basics have been already developed in section 2.2.1. We need now to introduce some fundamental elements about LC oscillators before investigating the design of the self-oscillating mixer. Figure 2.26 shows a parallel ideal lossless LC tank. If the capacitor (or the inductor) is initially charged, when

the switch closes the voltage across the resonator is sinusoidal with a constant amplitude (determined by the initial condition and the values of L and C). The nominal frequency of oscillation is determined by the tank parameters

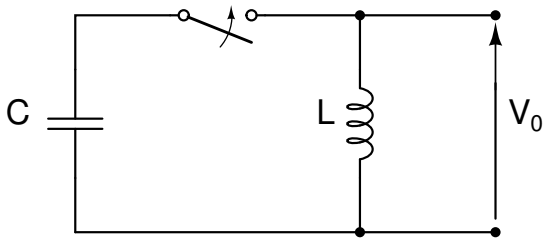


Figure 2.26: Ideal inductor capacitor resonator

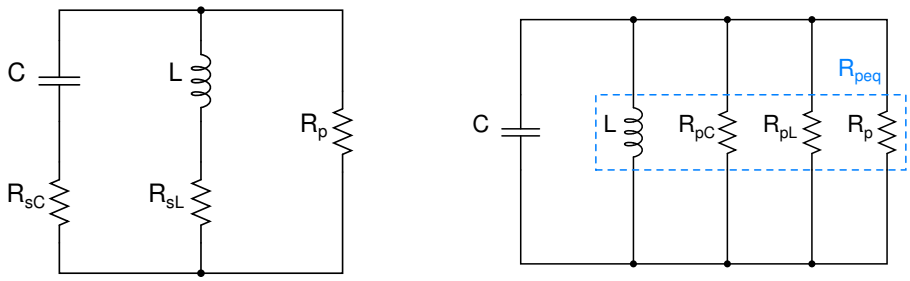
according to Eq 2.18:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.18}$$

Under the hypothesis of lossless components, the inductor and capacitor continue to exchange the stored energy in each other and the output voltage will never be attenuated. In practice, the hypothesis of lossless component does not hold on. Figure 2.27 shows a real case of LC resonator which includes series losses for all components (R_{sL}, R_{sC}) and a parallel loss (R_p). The loss associated with the reactive components is identified by the quality factors:

$$Q_L = \frac{\omega L}{R_{sL}} \tag{2.19}$$

$$Q_C = \frac{1}{\omega C R_{sC}} \tag{2.20}$$



(a) Serie losses

(b) Parallel losses

Figure 2.27: Tank serie and parallel losses

For sufficiently large Q_L and Q_C, the tank can be represented (near the resonant frequency) by the circuit of Figure 2.27b with:

$$R_{pL} = Q_L \omega L \tag{2.21}$$

$$R_{pC} = \frac{Q_C}{\omega C} \tag{2.22}$$

The characteristic impedance Z_0 and the quality factor of the complete tank circuit Q_T are defined as follows:

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{1}{\omega_0 C} = \omega_0 L \tag{2.23}$$

$$R_{peq} = R_p // R_{pC} // R_{pL} \tag{2.24}$$

$$Q_T = \frac{R_{peq}}{Z_0} = \frac{R_{peq}}{\omega_0 L} = \omega_0 C R_{peq} \tag{2.25}$$

$$\frac{1}{Q_T} = \frac{Z_0}{R_p} + \frac{1}{Q_L} + \frac{1}{Q_C} \tag{2.26}$$

The total tank quality Q_T is dominated by the lowest quality factor component. Due to the presence of the tank losses (represented by R_{peq}) the oscillation vanishes, because part of the energy exchanged in each cycle from the inductor to the capacitor and vice versa is dissipated by R_{peq}. In order to maintain the oscillations, a negative conductance must be added in parallel to the resonator to compensate the tank losses. Negative conductance (or resistance) can be obtained with active circuits providing energy to the LC resonator, at least

equal to the energy dissipated by the tank losses in each cycle. The minimum needed negative conductance g_{mc} must be at least equal to the total loss conductance ($1/R_{peq}$):

$$|g_{mc}| \geq \frac{1}{R_{peq}} = \frac{1}{Q_T Z_0} \tag{2.27}$$

To guarantee oscillations start-up under Process-Voltage-Temperature (PVT) variations the negative conductance is designed with a factor of 1.5 to 3 times larger than the required minimum. There are several circuits able to provide negative conductance (or resistance), leading to a wide variety of oscillator topologies [30][33]. Among them, the widely used circuit topology of a CMOS LC tank oscillator is depicted in Figure 2.28. It is commonly preferred for several reasons:

* It requires a minimal number of active (and noisy) components, resulting in low phase noise
* It requires a minimal number of passive components, and thus low silicon area
* It is very easy to insert variable capacitors to tune the output frequency
* It is a differential topology providing two anti-phase (180° shifted) output signals. Differential topology is inherently less sensitive to common-mode noise, such as supply voltage variation and substrate noise, it also intrinsically remove even order distortions.

  The differential resonator of the Figure 2.28 is composed by two LC tanks where the parallel losses are represented by R_{peq}. When the tail transistor is biased in saturation region the circuit gives the differential negative conductance to compensate the tank losses. The small signal differential conductance is given by: g_{mc} = -g_m/2 where g_m is the transconductance of the transistor $M_{2,3}$. To guarantee the oscillation start-up the following equation must be satisfied:

$$|g_{mc}| = \frac{g_m}{2} \geq \frac{1}{2R_{peq}} \tag{2.28}$$

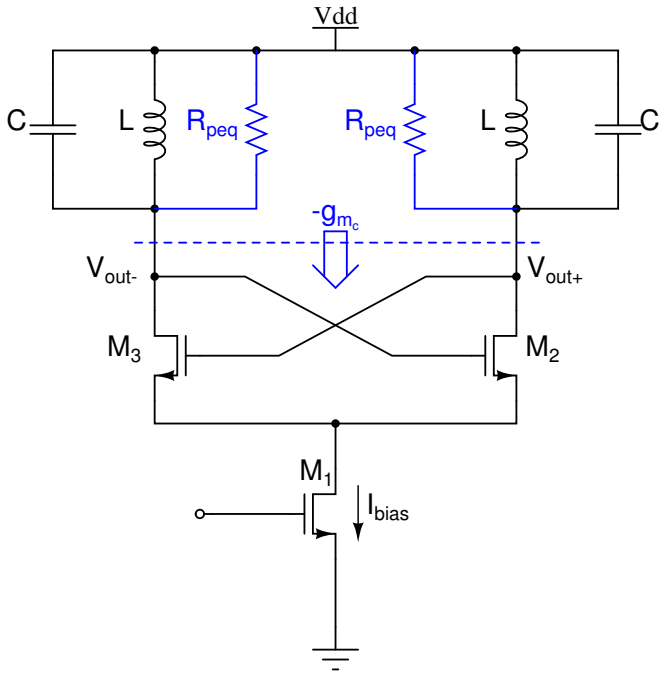


Figure 2.28: Circuit schematic of negative resistance LC CMOS Oscillator

where $2R_{peq}$ is the total differential resistance seen across the two LC tanks. The transconductance of each cross coupled transistor must be higher than the corresponding LC tank loss [42].

Oscillation Amplitude

If we assume that the differential current entering into the resonator is a squarewave ranging from -$I_{bias}/2$ to $I_{bias}/2$, at the frequency of resonance, higher harmonics of this input current are strongly attenuated by the LC tank and only its fundamental component (I_0=$2I_{bias}/\pi$) is converted into a differential voltage by the equivalent impedance at resonance $2R_{peq}$= $2Q_T Z_0$. At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain. In such cases, the tank amplitude can be better approximated as:

$$V_{out_{diff}} = \frac{4}{\pi} I_{bias} Z_0 Q_T = \frac{4}{\pi} I_{bias} \omega_0 L Q_T \tag{2.29}$$

We can observe the linear dependence between the oscillation amplitude and I_{bias}, Q_T, and Z_0. So to increase the output voltage swing, it is sensible to increase either the tail current or LQ_T product. However, increasing the tail current increases power consumption. Therefore, there has been constant research on improving inductor quality factor. High Q inductor also implies a lower g_m to start oscillations.

This analysis is true in the current-limited region of the oscillator. However, there is a point where a further enhance in current does not lead to an increase in output voltage swing. This is the voltage-limited region where the output swing is limited by the DC voltage supply. The output voltage saturates to a value close to two times the voltage supply V_{DD}. The bias current at which the oscillator saturates is $I_{bias_{sat}}$:

$$V_{sat} = 2\alpha V_{DD} = \frac{4}{\pi} I_{bias_{sat}} Z_0 Q_T \tag{2.30}$$

Therefore,

$$I_{bias_{sat}} = \frac{\pi}{2} \frac{\alpha V_{DD}}{Q_T Z_0} = \frac{\alpha V_{DD}}{\omega_0 L Q_T} \tag{2.31}$$

with $\alpha < 1$

Phase Noise

Another design challenge in voltage controlled oscillators is the phase noise. Phase noise arises from thermal noise and flicker noise of the cross-coupled pair, MOS varactors, tail transistor, and the LC tank. The injected noise affects the amplitude and phase of the oscillator. Figure 2.29 shows the spectrum of an ideal and a real oscillator. An ideal oscillator only oscillates at the designed frequency and its frequency spectrum is just an impulse at f_{LO}, whereas the real oscillator has a spread-out spectrum due to the bandpass nature of the LC tank. In the time-domain, phase noise produces jitter and amplitude variation.

Figure 2.29: Ideal and real oscillator spectrum

The effect of phase noise in a downconverting system can be explained by Figure 2.30. After downconversion, the desired signal and interferer overlap each other. The finite power of the interferer appears as noise power that corrupts the desired signal and affect the selectivity of the system. Hence lowering the phase noise is one of the important design goals in oscillator design in order to meet a specific standard.

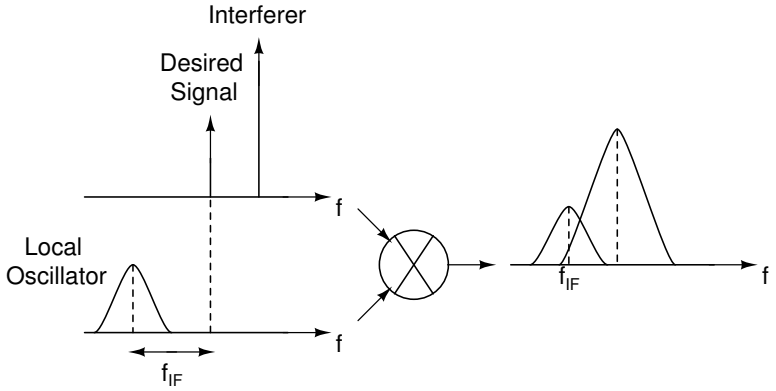


Figure 2.30: Effect of phase noise in a downconverting system

Leeson in [43] proposes an analytic expression of phase noise based on a Linear Time Invariant (LTI) model. The phase noise $\mathcal{L}(\Delta\omega)$ is specified at an offset frequency ($\Delta\omega$) from the carrier (ω_0) according to Eq 2.32:

$$\mathcal{L}(\Delta\omega) = 2kTR_{peq}\frac{F}{V_0^2}\{\frac{\omega_0}{Q_T\Delta\omega}\}^2 \tag{2.32}$$

where k is the Boltzmann's constant, T is the absolute temperature, R_{peq} is the equivalent tank parallel resistance, V_0 is the peak oscillation

amplitude, Q_T is the tank quality factor. F, the noise factor, is given by [44]:

$$F = 2 + \frac{8\gamma R_{peq} I_{bias}}{\pi V_0} + \frac{8}{9} g_{m_{bias}} R_{peq} \tag{2.33}$$

where γ is the device white noise coefficient and $g_{m_{bias}}$ is the current source transconductance. As previously seen, at low bias current, when the amplitude of oscillation is smaller than the power supply, the differential pair acts as a simple current switch driving the resonators and V_{out} is expressed by Eq 2.29. For higher currents, the output voltage saturates close to two times the supply voltage. Combining Eq 2.32 and Eq 2.33, we can obtain:

$$\mathcal{L}_{current-limited}(\Delta\omega) = (2 + 2\gamma)\frac{\pi^2 kT}{16\omega_0 L Q_T I_{bias}^2}\{\frac{\omega_0^2}{Q_T \Delta\omega}\}^2 \tag{2.34}$$

$$\mathcal{L}_{voltage-limited}(\Delta\omega) = \{2 + \frac{4\gamma\omega_0 L Q_T I_{bias}}{\pi\alpha V_{DD}}\}\frac{kT\omega_0 L Q_T}{4(\alpha V_{DD})^2}\{\frac{\omega_0^2}{Q_T \Delta\omega}\}^2 \tag{2.35}$$

Eq 2.34 and Eq 2.35 show that the phase noise decreases with I_{bias} in the current-limited region and increases in the voltage-limited region. Therefore, minimum phase noise is achieved at the transition of the two regions, when $V_{out} = V_{sat} = 2\alpha V_{DD}$ and can be expressed as referenced in Eq 2.36:

$$\mathcal{L}_{min}(\Delta\omega) = (2 + 2\gamma)\frac{kT\omega_0 L Q_T}{4(\alpha V_{DD})^2}\{\frac{\omega_0^2}{Q_T \Delta\omega}\}^2 \tag{2.36}$$

For a given technology, V_{DD} and γ are fixed. The tank quality factor Q_T can be maximized by an optimum choice of inductor and varactor. To reduce the minimum achievable phase noise of an oscillator, the inductor should be reduced, and the current consumption equally increased (according to Eq 2.31) to fall in the optimum region of operation [42].

2.3.2 Self-Oscillating Mixer State-of-the-art

To combine both a mixer and an oscillator, many techniques have emerged in the literature. Self-oscillating mixer presented in [4] (Figure 2.31)

achieves the oscillation and mixing functions by stacking an LC-tank on a double balanced current-commuting mixer. Since the mixer output is fully differential, two cross-coupled pairs connected in parallel act as loads for the switching stage. As matter of consequences, the LO signal can easily end up at the mixer output. Another double-balanced oscillator

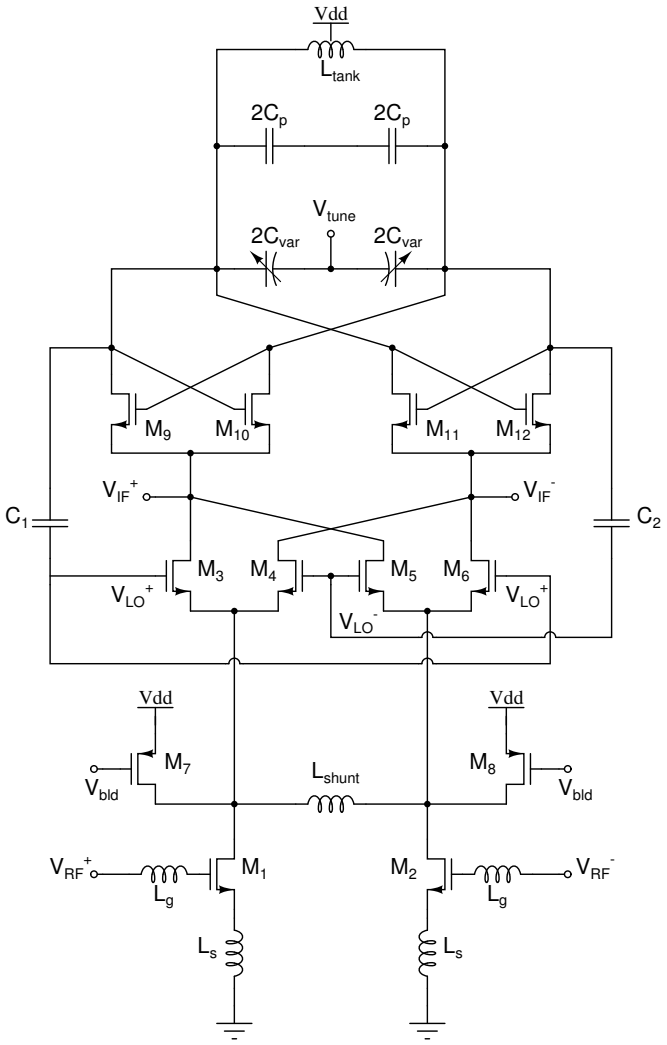


Figure 2.31: Schematic of the self-oscillating mixer proposed in [4]

mixer implemented in a 180 nm CMOS technology is reported in [5] (Figure 2.32). In such configuration, the LO output signal is generated

by a nMOS differential VCO which is directly fed into the source of a switching pair. This topology can operate under very low voltage supply, the V_{DD} is 1 V.

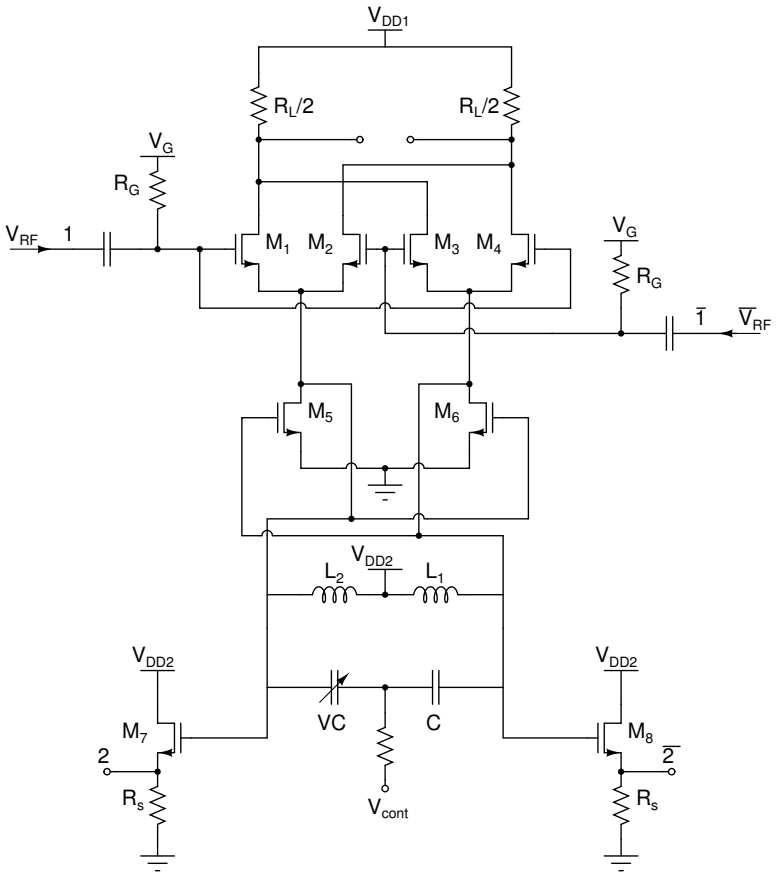


Figure 2.32: Low-power oscillator mixer from [5]

Through a specific approach of the transconductor stage, some SOM topologies exhibit a low noise amplification. There are referenced as LMV for LNA-Mixer-VCO. In [22], the LMV cell (Figure 2.33) exploits the intrinsic mixing functionality of a LC-tank oscillator to provide a compact solution. Sensing the downconverted signal at the output of the VCO unavoidably degrades the oscillator phase noise, so, a capacitor C_{diff} is introduced to sense the IF signal at the sources of transistors (M_1,

M_2). It closes the loop at RF while presenting a high impedance at IF. A design trade-off between LNA and VCO must be undertaken in the choice of the aspect ratio of transistor M_0, which is, at the same time, the VCO bias generator and the core of the low-noise amplifier. This means that the flicker noise injected by M_0 degrades the VCO phase noise. Therefore, to avoid this trade-off, a low-frequency degeneration circuit must be introduced, attenuating the 1/f noise injected by the LNA core into the VCO. To reduce losses in the IF path, The LMV cell operates in current mode (*i.e.* introducing a virtual ground as IF output load). It boosts the overall down-conversion gain to 36 dB. Unfortunately, this technique dramatically increases the power consumption to 5.6 mW.

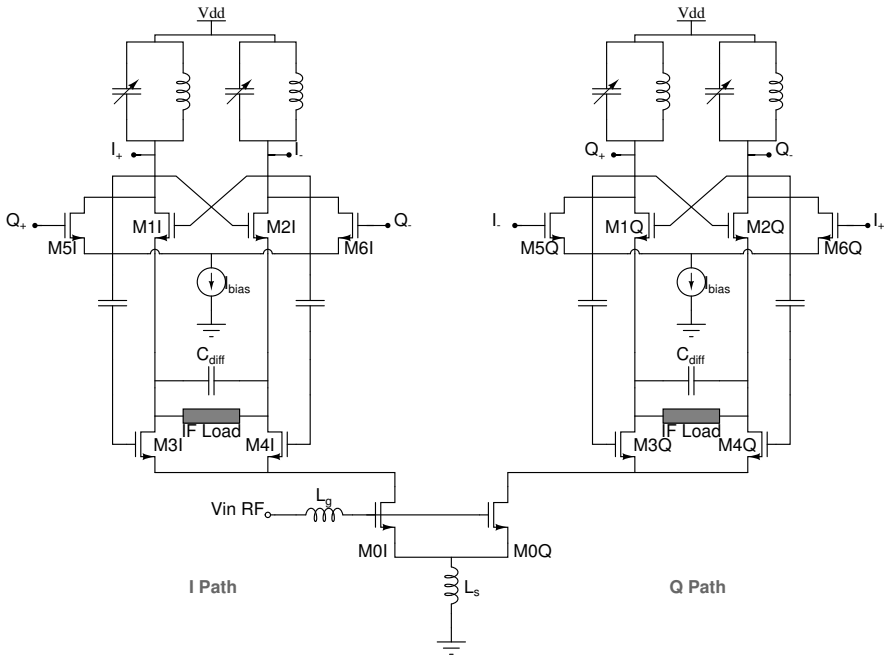


Figure 2.33: Low-power oscillator mixer from [5]

The self-oscillating mixer proposed in this thesis is inspired from the work reported in [4]. A LC-tank is stacked on a single balanced mixer through two cross-coupled pairs in a current-reuse configuration. To take

advantages of subthreshold operation, the transconductor stage is biased in moderate inversion and some efforts have been undertaken to further enhance the LO-IF isolation. Indeed, since the tank is stacked on the top of the switching pair, LO signal can easily ends at the mixer output. So, capacitors C_p are introduced to degenerate the cross-coupled pair at high frequencies and reduce LO feedthrough from the tank. A block diagram of the proposed ultra-low power SOM is depicted in Figure 2.34.

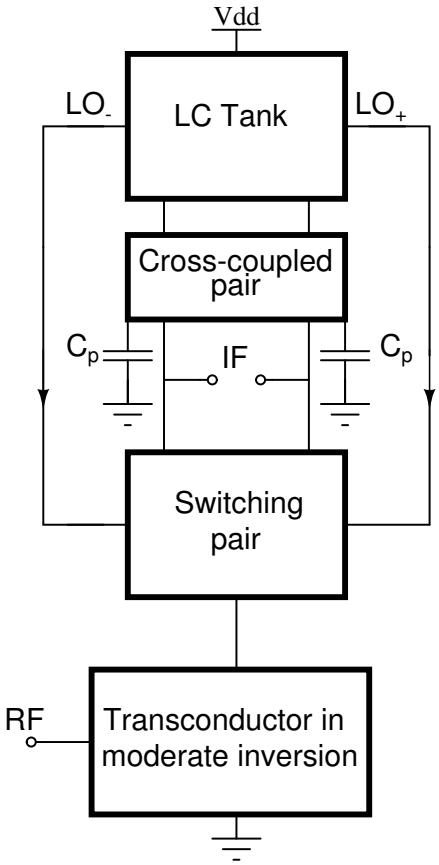


Figure 2.34: Block diagram of the proposed self-oscillating mixer

2.3.3 Circuit Design

In this section, a design analysis of the major blocks in the proposed self-oscillating mixer is detailed. First SOM core is described, transistor

models are also investigated. Then, the buffer circuit is briefly described.

SOM Core

Before proceeding to the design of the self-oscillating mixer, two transistor types from the design kit are compared according to the figure of merit $g_m f_T/I_D$. Figure 2.35 shows the $g_m f_T$-to current ratio for the two transistor types, Low Power (LP) and General Purpose (GP), and this for various sizes.

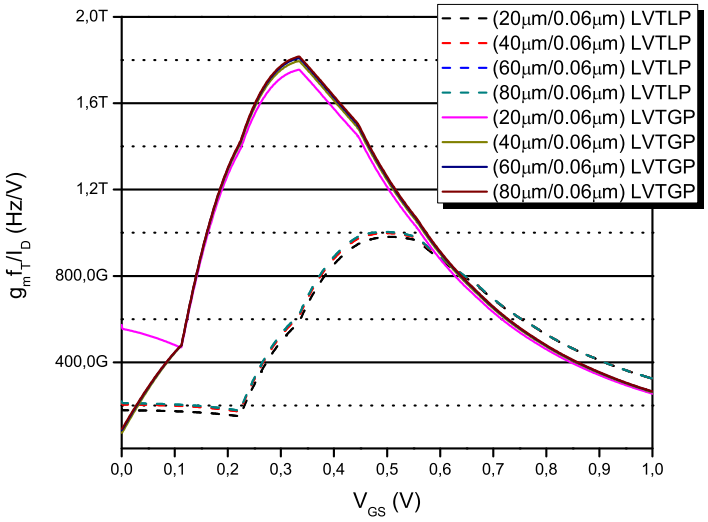


Figure 2.35: $g_m f_T/I_D$ versus V_{GS} for LP and GP transistors

The maximum of $g_m f_T/I_D$ is reached at a gate-source voltage of 330 mV and 500 mV for the transistors GP and LP respectively. Thus, the amount of current consumed by GP model is less than the LP one. So, we have chosen the GP model since our main design goal is ultra-low power. For the following, the gate-source voltage of the transconductor stage of the SOM will be fixed to 330 mV. The circuitry of the proposed self-oscillating mixer is depicted in Figure 2.36. An LC oscillator is stacked on a single balanced mixer for low power consumption. The core supply voltage,

V_{DD}, is chosen to be 1 V for nominal operation and the required bias current, I_{bias}, is fixed by both startup condition and output voltage swing to perform the mixing operation. The core bias current through tail

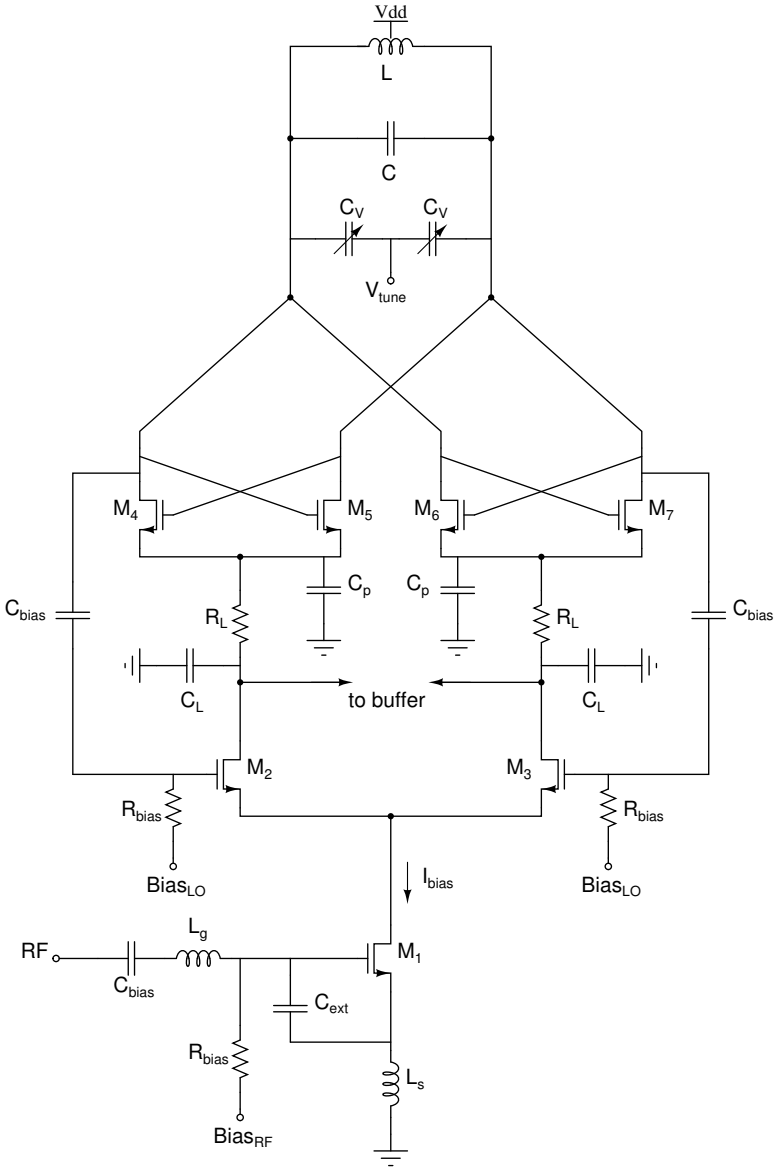


Figure 2.36: Schematic of the proposed self-oscillating mixer core

transistor M_1 is controlled by an external voltage $Bias_{RF}$ applied to the gate of M_1. Transconductor stage is biased in moderate inversion region

and inductively degenerated for input matching. The inductances needed for L_g and L_s are 2.2nH and 4.3nH respectively. Capacitor C_{ext} of 850fF was added to minimize the size of the inductance L_g (Eq 2.37). The value of C_{ext} imposes a tradeoff between L_g size, gain and noise of the RF transconductor stage.

$$Z_{in} = \omega_T L_s + j\{(L_g + L_s)\omega - \frac{1}{(C_{gs} + C_{ext})\omega}\} \tag{2.37}$$

with ω_T=$g_m/(C_{gs}$+$C_{ext})$

At the operating frequency, f_{RF}=2.4 GHz, the real part of Z_{in} must be equal to 50 Ω and its imaginary part to zero:

$$\omega_T L_s = 50\,\Omega \Rightarrow L_s = 50\frac{(C_{gs} + C_{ext})}{g_m} \tag{2.38}$$

$$(L_g + L_s)\omega_{RF} - \frac{1}{(C_{gs} + C_{ext})\omega_{RF}} = 0 \Rightarrow L_g + L_s = \frac{1}{(C_{gs} + C_{ext})\omega_{RF}^2} \tag{2.39}$$

The LC oscillator and the mixer part are connected through the source terminal of the cross-coupled pair. So, a single-ended configuration of the cross-coupled pair does not permit this connection because of differential output of the mixer, however, the same cross-coupled pair can be realized by connecting two cross-coupled pair in parallel as shown in Figure 2.37, where the transistor size is half the original thus permitting a differential connection. The overall small-signal negative resistance provided by the

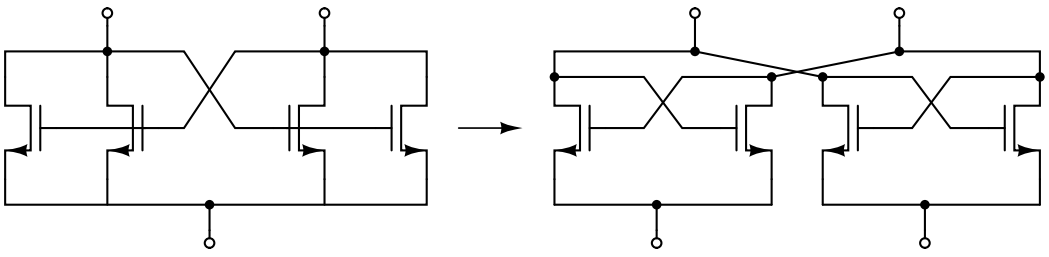


Figure 2.37: Single-ended and differential configurations for cross-coupled pair

two cross-coupled pair ($M_{4,5,6,7}$) must deliver enough energy to cancel

the tank losses and allow oscillations to build up. Therefore, the critical parameter for oscillator startup is the transconductance of the cross-coupled devices. The required g_m for startup establishes a lower limit on the current consumption of the SOM. The tank losses was evaluated to 670 Ω at 2.41 GHz, so the necessary $g_{m,crit}$ to start the oscillations is:

$$|g_{mc}| = \frac{g_{m,crit}}{2} = \frac{1}{R_{peq}} \Rightarrow g_{m,crit} = 2.9\,\text{mS} \tag{2.40}$$

To ensure reliable startup, the required transconductance must be at least twice the minimum value. The specified g_m provided by the two cross-coupled pair is set to 6 mS. In order to optimize the transconductance for minimal bias current, transistors M_4-M_7 are designed at the limit between weak and moderate inversion region. Referring to Figure 2.38 which represents the transconductance efficiency, the g_m/I_D is around 15 in this region. This leads to a core bias current of 500 µA. The impedance seen

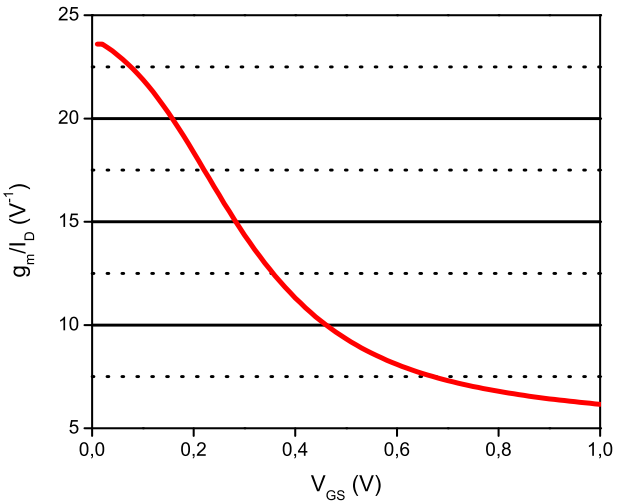


Figure 2.38: gm/I_D for a (30 µm/0.06 µm) nlvtgp transistor in 65 nm process

at the sources of the cross-coupled pairs is equal to $1/2g_{m4,5,6,7}$ ($\approx 80\,\Omega$). Due to the low bias current, this impedance is not sufficient to perform a

large current to voltage conversion at the output of the mixer. To improve the conversion gain, the resistors R_L are introduced. In Figure 2.39, a comparison between voltage conversion gain with and without R_L is shown and this for different IF frequencies. The mixer stage provides a negative gain in dB without R_L, less than $-12\,\mathrm{dB}$.

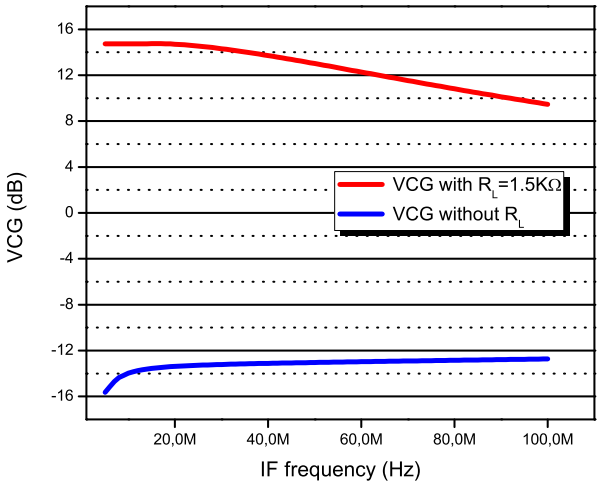


Figure 2.39: Voltage conversion gain with and without R_L

Under input matching conditions, the voltage conversion gain is expressed in Eq 2.41.

$$VCG \approx \frac{1}{\pi}\frac{\omega_0(L_g+L_s)}{R_s}g_{m1}R_L \tag{2.41}$$

$$\omega_0 = \frac{1}{2\pi\sqrt{(L_g+L_s)C_{gs1}}} \tag{2.42}$$

where R_s is equal to $50\,\Omega$.

The increase of g_{m1} and R_L improves the gain and enlarge the power consumption too. The impact of R_L on conversion gain and noise figure was investigated and depicted in Figure 2.40. For this SOM, R_L is made large, $1.5\,\mathrm{k}\Omega$, ensuring a sufficient voltage headroom for the switching pair (M_2, M_3) of the mixer. The overdrive voltage is fixed to zero for

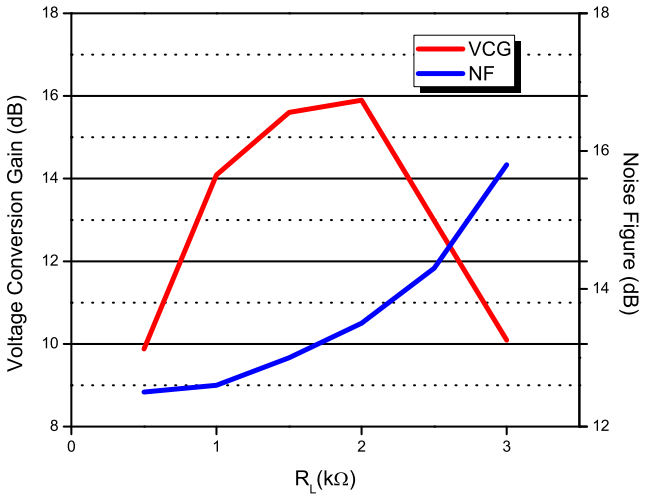


Figure 2.40: Voltage conversion gain and noise figure versus R_L

appropriate switching operation. Finally, the current is kept low, 500 µA, for power saving. A large capacitor C_p of 10 pF is added at the sources of the cross-coupled pairs in order to short cut to ground the oscillations and so prevent LO to IF feedthrough. At the mixer output, a low-pass filter (R_L(1.5 kΩ), C_L(5.3 pF), providing a large impedance in IF band and allows for a rejection of high frequency harmonics -*i.e.* RF and LO signals. To tune the frequency of oscillation, n-type inversion mode MOS varactors are used. The variable capacitors are connected in parallel with the inductors. The gate terminals are placed outside whereas drain/source terminals are connected together in a common mode node. This node acts as a virtual ground for the differential signal. The bulk parasitic capacitance of varactors is then shorted and do not load the LC tank. The tuning voltage is applied at the drain/source terminals as shown in Figure 2.41. Let us assume the gate voltage is the maximum available voltage, *i.e.* the supply voltage V_{DD}, and the bulk is connected to ground. When V_{CTRL} is equal to V_{DD} the channel

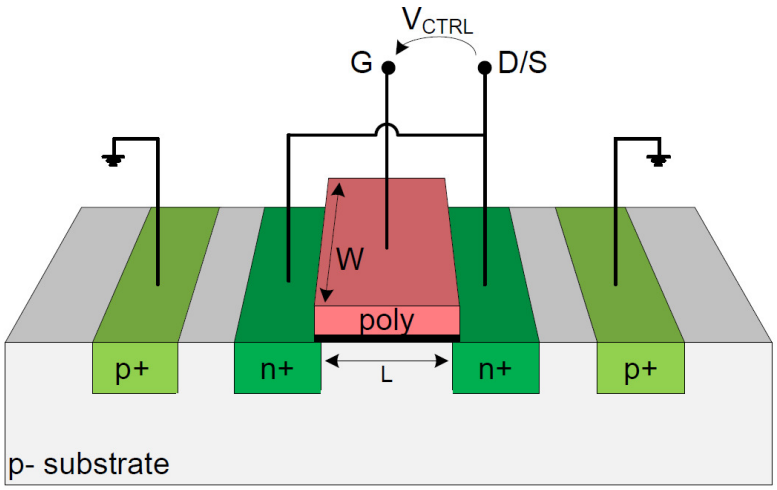


Figure 2.41: Cross section of I-MOS varactor

is strongly inverted and the capacitance is mainly the oxide capacitance ($C_{ox}\times$ W$\times$ L). The capacitance seen from the gate is hence given by the series of the gate oxide and the depletion oxide capacitances, the latter being smaller than the former. To further reduce the tank losses, it is important to maximize the varactor quality factor Q_C. The gate resistance is proportional to the channel length L, the quality factor increases as 1/L; therefore Q_C is maximum with the minimum length device. Usually the device is made up of several wide finger in parallel, in order to reduce the gate resistance. On the other hand, the fixed parasitic capacitance takes more relevance by reducing the finger width, thus reducing the achievable tuning range. W_{finger}=5 µm has been chosen as a tradeoff between varactor quality factor and tuning range. Figure 2.42 shows the Q_C and C_{max} to C_{min} ratio of a varactor with W_{TOT}=40 µm simulated for several gate lengths at 2.41 GHz. The minimum Q_C largely decreases with increasing the gate length, while the tuning ratio increases. It is worth noticing that a minimum length is mandatory to achieve a high Q_C at 2.41 GHz. Figure 2.43 shows the simulated C-V and Q-V characteristics, for a varactor structure with 8 fingers of 5 µm width and minimum length.

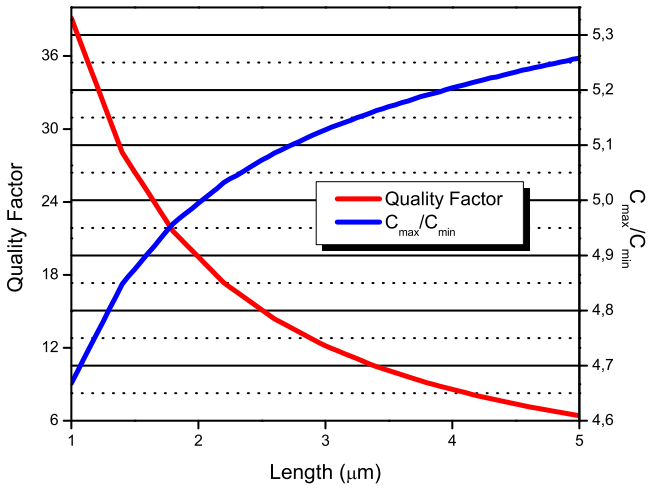


Figure 2.42: Varactor quality factor and C_{max}/C_{min} versus transistor length

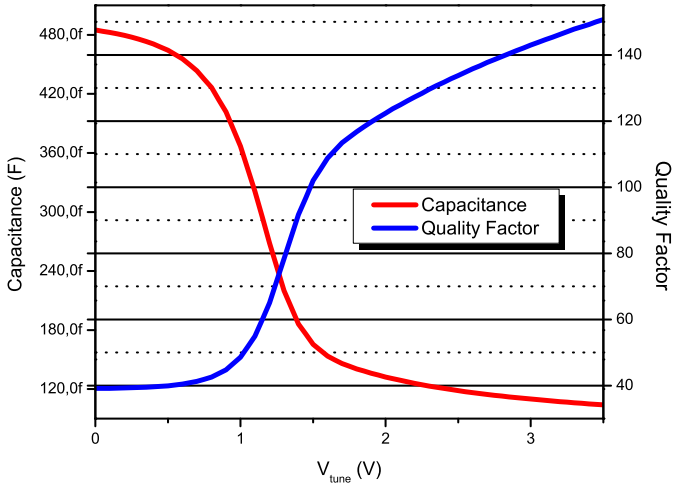


Figure 2.43: Varactor quality factor and capacitance versus V_{tune}

Output Buffer

The buffer used in this design is a differential common-source amplifier as shown in Figure 2.44. Capacitor C_2 of 10 pF is used for DC blocking and resistor R_2 of 10 kΩ for self-biasing transistor $M_{10,11}$ which is placed in saturation region. The transistor size of $M_{10,11}$ and the load resistor R_D are designed to provide a 1 V/V voltage gain and does not significantly affect the linearity of the SOM. The value of load resistor must also contribute for output matching, it is fixed to 140 Ω. A low-pass filter (R_1,

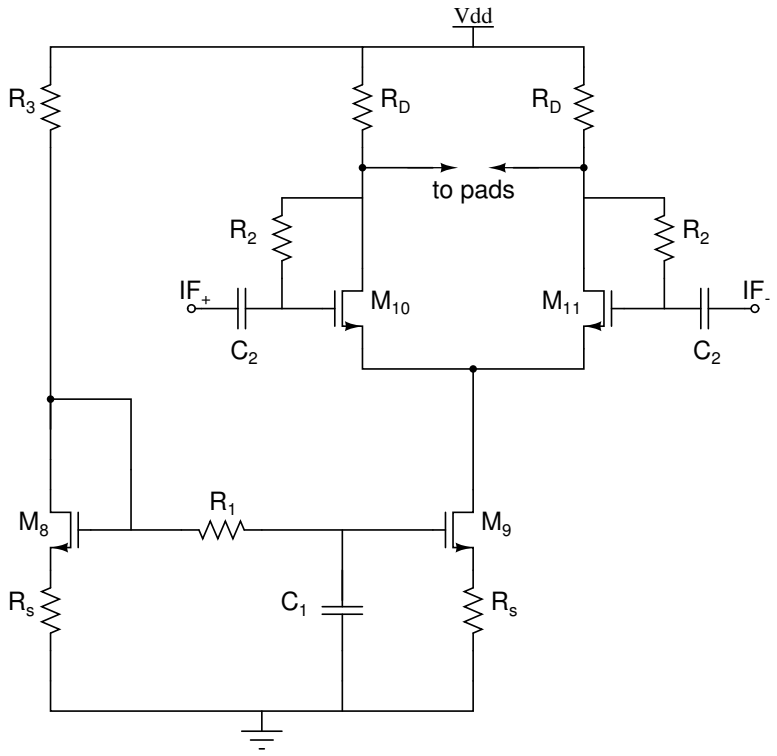


Figure 2.44: Schematic of the differential common source buffer

C_1) was introduced to reduce noise contribution of the current mirror (M_8, M_9). The buffer operates from a 1 V supply and has a total current consumption of 2.1 mA. The final device types and aspect ratios are summarized in Table 2.4.

Table 2.4: Sizes of SOM devices (core and buffer)

Device	Size	Device	Size
M_1(W/L)	25 µm/0.06 µm	C_L	5.3 pF
$M_{2,3}$(W/L)	20 µm/0.06 µm	C_p	10 pF
$M_{4,5,6,7}$(W/L)	30 µm/0.06 µm	C_1	5 pF
$M_{8,9}$(W/L)	60 µm/0.06 µm	C_2	10 pF
$M_{10,11}$(W/L)	15 µm/0.06 µm	R_{bias}	5 kΩ
L_g	2.2 nH	R_L	1.5 kΩ
L_s	4.3 nH	R_1	5 kΩ
L	4 nH	R_2	10 kΩ
C	470 fF	R_3	180 Ω
C_{bias}	10 pF	R_D	140 Ω
C_{ext}	850 fF	R_S	15 Ω

2.3.4 Measurement Results

Figure 2.45 shows a microphotograph of the implemented SOM in a 65 nm CMOS technology from STMicroelectronics. A single-ended ground-signal-ground (GSG) probe was used to generate RF input signal and a differential GSGSG probe to sense the IF signal. A bias-T was introduced at the input port for variable DC bias voltage to control the transconductor stage through $Bias_{RF}$. An external 180° hybrid is needed at the IF port to convert the differential output into a single-ended signal. Supply and bias voltages were generated by an Agilent E3631A DC power supply. Bias voltages was tuned to get best gain and noise performances, the nominal bias conditions are I_{bias}=600 µA and V_{DD}=1 V. The varactor control voltage is fixed for an oscillation frequency of 2.6 GHz. The input return loss of the circuit is depicted in Figure 2.46. It was measured using an Agilent E8361A PNA network analyzer. At the designed RF input

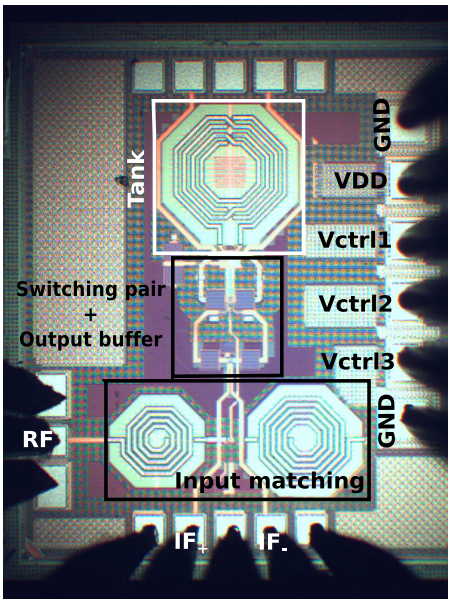


Figure 2.45: SOM microphotograph

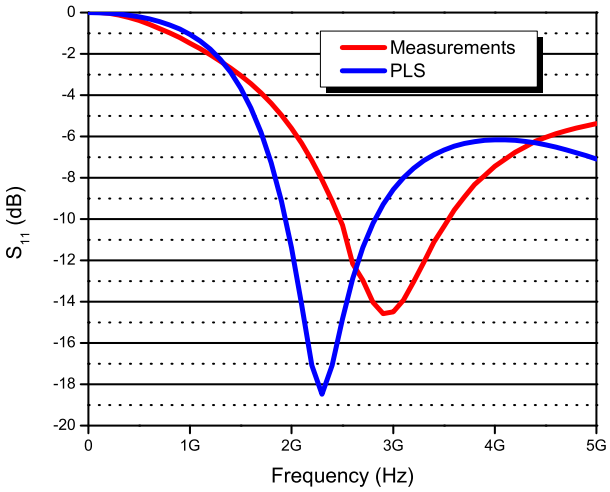


Figure 2.46: Input return loss of the self-oscillating mixer

frequency of 2.55 GHz, the measured S_{11} was −11 dB.

Due to the limited chip space, no pads were allocated to the oscillator's LO output and therefore the LO output power and phase noise could not be measured. However, the LO frequency could be deduced from the IF one with respect to RF frequency. For this purpose, the varactor drain/source voltage was tuned from 0 V to 2 V and IF frequency was measured. Figure 2.47 shows the frequency range of the oscillator. It varies from 2.55 GHz to 2.75 GHz which correspond to a tuning range of 7.5 %. To measure gain and noise performances, a −30 dBm 2.55 GHz RF

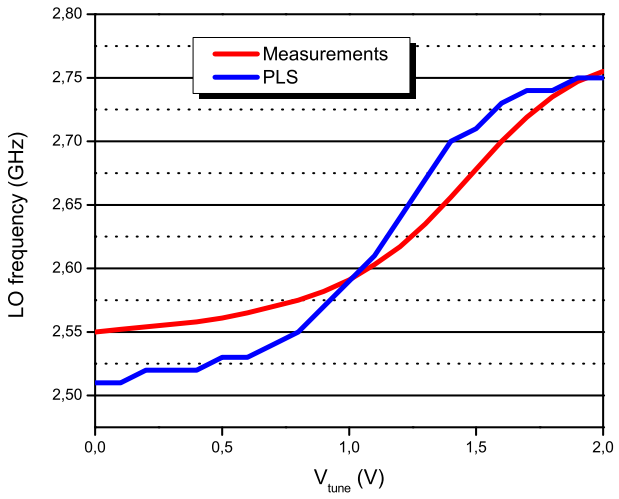


Figure 2.47: Tuning range of the SOM

signal was applied and the LO signal was tuned through V_{tune} in order to collect the performances at different IF frequencies. The proposed self-oscillating mixer achieves a voltage conversion gain and a single side band noise figure of 8.5 dB and 18 dB respectively at 15 MHz IF frequency. Measured results are shown in Figure 2.48 and Figure 2.49.

Several possible causes can justify the discrepancies between post-layout simulations and measurements. One possible explanation is that the

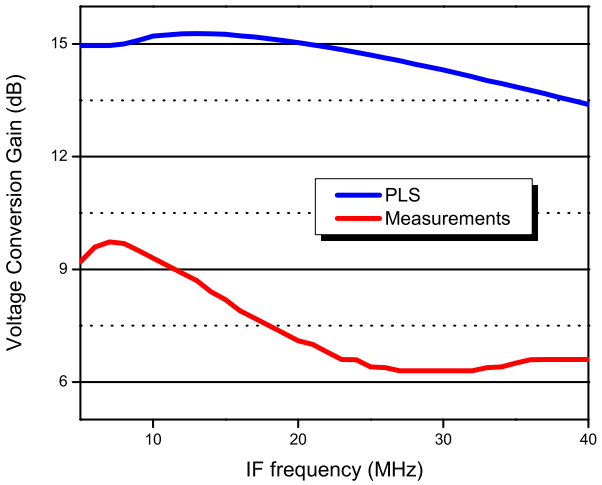


Figure 2.48: Voltage conversion gain at different IF frequencies

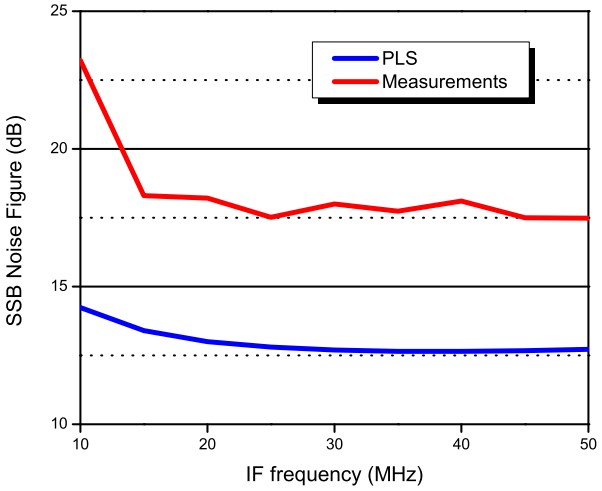


Figure 2.49: Single side band noise figure at different IF frequencies

actual gain of the output buffer is lower than unity. Any gain error or impedance mismatch in the buffer directly impacts the measured gain of the SOM. It is also possible that parasitic resistance in the layout increases losses in the tank, affecting the output voltage swing of the oscillator and therefore the switching operation of the mixer. A final possibility is the underestimation of parasitic elements by the extractor.

Voltage conversion gain was also investigated under different bias conditions. First, the bias voltage $Bias_{LO}$ controlling the switching pair of the mixer is held constant and the bias voltage of the transconductor stage $Bias_{RF}$ is varied. Secondly, $Bias_{LO}$ is swept while $Bias_{RF}$ is kept constant. This measurement demonstrates the performance for different transistor regions of operation. Figures Figure 2.50 and Figure 2.51 show the voltage conversion gain and the bias current versus $Bias_{RF}$ and $Bias_{LO}$ respectively. As shown in Figure 2.50, the self-oscillating mixer

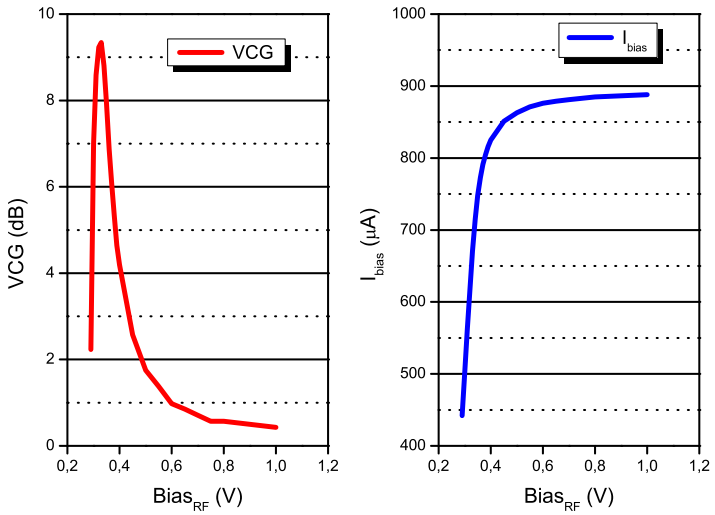


Figure 2.50: Voltage conversion gain and I_{bias} versus $Bias_{RF}$

achieves a maximum gain in moderate inversion region. Increasing $Bias_{RF}$ beyond this region no longer enhance the gain since the transconductor

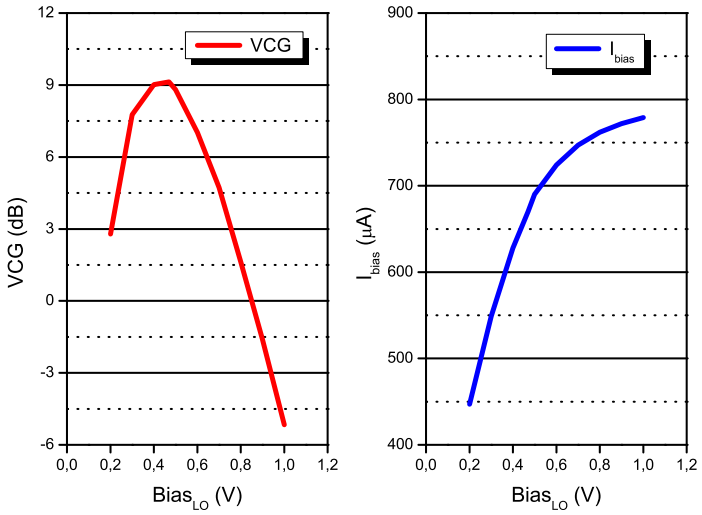


Figure 2.51: Voltage conversion gain and I_{bias} versus $Bias_{LO}$

stage leaves saturation region. Varying bias voltage $Bias_{LO}$ also varies the voltage conversion gain. When $Bias_{LO}$ is approximately equal to V_{TH}, which correspond to a zero overdrive voltage for the switching pair of mixer, the SOM exhibit a maximum gain. To measure the linearity of the implemented self-oscillating mixer, the input power was swept and the downconverted signal was measured by an oscilloscope. Figure 2.52 shows the input referred 1dB compression point. Mainly controlled by the transconductor stage, the input P_{1dB} is $-20.5\,\mathrm{dBm}$. Design effort undertaken between oscillating and switching parts (*i.e.* capacitive degeneration at the sources of the cross-coupled pairs) leads to a high RF to IF isolation, 42 dB with respect to RF input power. Since the LO power was not precisely known, the LO leakage power at the RF and IF ports was measured instead of LO-to-RF and LO-to-IF isolation. LO feedthrough at these ports are $-68\,\mathrm{dBm}$ and $-64\,\mathrm{dBm}$ respectively. The different leakages are depicted in Figure 2.53.

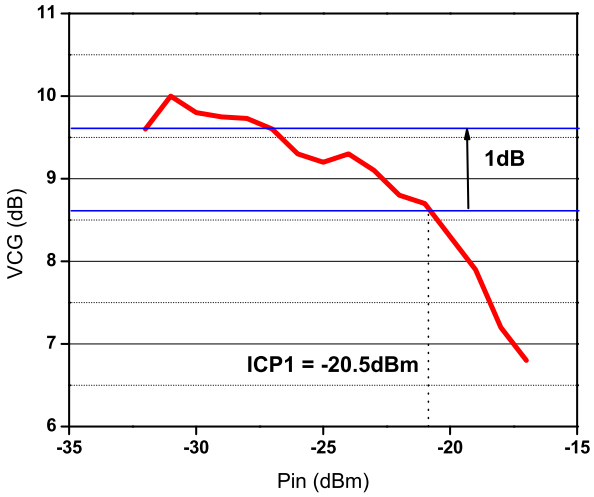


Figure 2.52: Measured input compression point ICP1

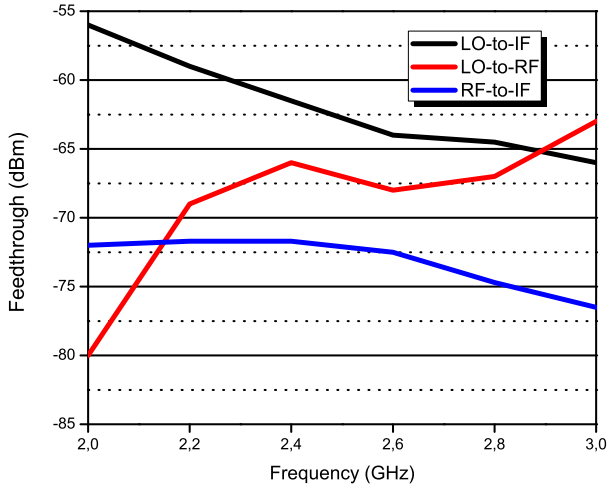


Figure 2.53: measured leakages of the SOM at different ports

Table 2.5 summarizes the SOM performances and compares its behavior to the state-of-the-art.

Table 2.5: Performance summary and comparison to other SOM

	This work	[4]	[5]
CMOS Technology [nm]	**65**	130	180
RF frequency [GHz]	**2.5**	7.8-8.8	4.2
Voltage Conversion Gain [dB]	**10@IF=**10 MHz	11.6	10.9
SSB Noise Figure [dB]	**17.5@IF=**25 MHz	4.39 (DSB)	14.5
ICP1 [dBm]	**-20.5**	-13.6	-
LO to RF Leakage [dBm]	**-68**	-59	-37
LO to IF Leakage [dBm]	**-64**	-44	-
P_{DC}[mW]	**0.6**	12	3.14

The implemented circuit proposed in this section has demonstrated the feasibility of an ultra-low power self-oscillating mixer by using design techniques such as current-reuse technique and taking benefits from moderate inversion operation. Obtained performances are deserving of respect if we consider the very low power consumption. Since the SOM in [41] is designed to meet stringent noise performances, it requires much more power. Nevertheless, in wireless sensor networks applications, the noise figure of the proposed SOM could correspond to the system specifications; such NF can ensure an acceptable sensitivity compatible with a low data rate, typically 100 kbit/s with a BFSK modulation scheme [1]. To further improve the sensitivity, the SOM can be combined with a LNA for an extra power consumption of a 100 µW according to [45].

2.4 Conclusion

In this chapter, design approaches were presented to enable the realization of very low power RF circuits for wireless sensor networks. Two main strategies were investigated to respond to these technical challenges of low power consumption. First, bias technique was adopted and subthreshold

device operation was explored as a method of reducing power consumption in transceiver circuits. A forward body biased transistor permits to reduce its subthreshold voltage and so the use of unusually low supply voltages. A new figure of merit $g_m f_T/I_D$ was also adopted to bias RF devices in order to capture both RF performances and DC power consumption. This FoM achieves its optimum in moderate inversion region so it is appropriate to operate in this region to reduce efficiently the power consumption. Second, at building blocks level, merging functionalities in a RF front-end seems to be attractive to further increase the battery life for wireless sensor's modules. Current-reuse technique was considered to meet this design requirement. Finally, to demonstrate these methodologies, a mixer and a self-oscillating mixer were designed and tested in 130 nm and 65 nm CMOS technologies. Ultimately, the ability to design RF circuits with nominal power consumption below 600 µW was demonstrated. The minimum power consumption achieved was less than 400 µW for the mixer. The circuit was biased to run in moderate inversion and operation with a supply voltage of less than 1 V was also demonstrated. Post layout simulations show a voltage conversion gain and a single side band noise figure of 18.7 dB and 11.5 dB respectively at an intermediate frequency of 10 MHz. Regarding the self-oscillating mixer, the circuit consumes 600 µW and measurement results demonstrate a voltage conversion gain of 10 dB and a single side band noise figure of 17.5 dB whereas the LO to IF feedthrough is −64 dBm.

Chapter 3

System Approach

The previous chapter presented strategies at transistor and building block levels to reduce power consumption in RF front-ends. In this chapter, a system level approach is proposed and described which uses a novel architecture to demodulate RF signals. The classical architectures existing in the state-of-the art are first discussed. Then, a demodulator system based on a pulled oscillator is proposed and investigated. Finally a test prototype is realized in 65 nm *CMOS technology to demonstrate its feasibility.*

3.1 Architecture Overview

There are several types of wireless receivers that allow detecting an RF signal. On one hand there are complex receivers that can detect very weak signals but consume a lot of power. On the other hand there are simple radio frequency identification (RFID) systems, which do not even have a power supply; however, they present a poor sensitivity. We can view this variety of receiver architectures on a scale of power consumption and complexity versus performance, which tend to move together on the continuum (Figure 3.1). The middle region between domains of low power passive detectors and high performance traditional wireless receivers is our

target region, using architectures with acceptable power and sensitivity.

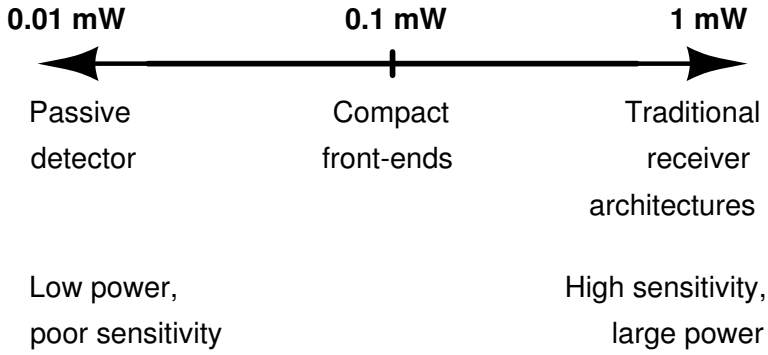


Figure 3.1: Receiver design space in terms of power consumption

3.1.1 Passive Detectors

Looking first at the lower bound of the scale, an RFID tag is one of the simplest, and therefore lowest power, wireless receivers. Although passive tags do not have power supply, they are able to derive power from the incoming RF waveform and, after storing sufficient energy, power up their own electronics to decode an incoming signal and transmit back to the reader. The RFID tag remains in sleep mode until it is remotely interrogated by RF energy reader. The latter is typically not power-constrained in RFID system and can transmit high output power, only regulatory constraints on effective isotropic radiated power (EIRP) must be respected. In the 2.4 GHz industrial-scientific-medical (ISM) band, for example, the reader may freely transmit up to 4 W EIRP for RFID applications [46]. However, in WSN applications, wireless links are peer-to-peer and the power of the transmitter cannot be ignored. To further understand the effect of the transmitter power in an RFID system, consider the example of an RFID tag designed in the 2.4 GHz band [46]. A simple diagram of the system is shown in Figure 3.2, with the reported operating specifications.

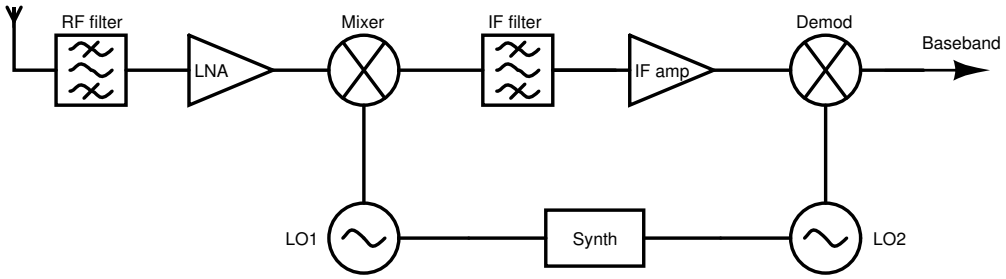
Figure 3.2: RFID link operating parameters

In active mode, the tag consumes only 1 µW. However, the RF sensitivity is poor, reported at −25.7 dBm on a 300 Ω antenna. In an RFID system, the problem can be overcome by simply transmitting higher power from the reader. This latter must transmit with 34.5 dBm output power at 2.4 GHz to communicate with the tag over a distance of 10 meters. In a peer-to-peer scenario where the transmitter is power-constrained, this power level is clearly much too high. Therefore, despite the attractive low power consumption of the RFID tag receiver, a practical compact front-end design will require much improved sensitivity in order to avoid shifting the burden of power consumption to the transmitter.

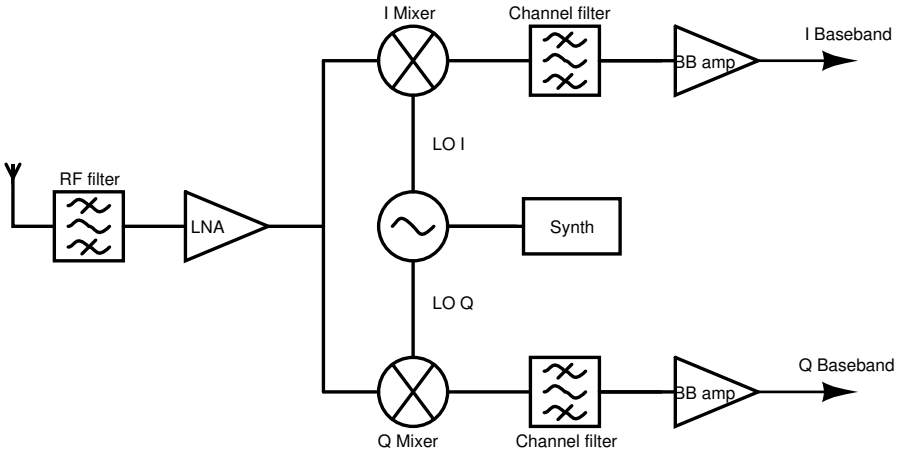
3.1.2 Traditional Architectures

Traditional wireless receivers lie on the other end of the scale from RFID system in Figure 3.1. In order to achieve high sensitivity and data throughput, these complex receivers utilize active devices and have much greater power consumption than passive detectors. The high-level architectures used in these receivers can generally be classified in a few major categories. The most commonly used architecture utilizes frequency conversion, where the input signal is shifted to a lower frequency to ease implementation of signal processing blocks such as gain and filtering. Selectivity is achieved through careful frequency planning, combining narrowband low frequency responses with high purity oscillators and mixers to perform frequency

conversion. In super-heterodyne architecture (Figure 3.3a), for example, two consecutive downconversion operations are used. First, the input RF signal is filtered by a pass-band filter to select the band of concern. Then, the RF signal is amplified by a low noise amplifier (LNA) to ease the noise requirements of the rest of the receiver chain. Next, a mixer performs the downconversion of the RF signal to intermediate frequency (IF) with a high-accuracy, tunable local oscillator (LO1). This IF signal is amplified and filtered with a fixed frequency filter to remove the image frequency and interferes. A second mixer converts the signal to DC using a fixed frequency oscillator (LO2) at the IF frequency.



(a) Super-heterodyne architecture



(b) Direct conversion or low-IF architecture

Figure 3.3: Traditional receiver architectures

Zero-IF and low-IF receivers (Figure 3.3b) got round the image problem by mixing the RF signal directly to baseband using quadrature downconversion. As in the super-heterodyne architecture, a local oscillator with high spectral purity and stability is required to drive the mixer. The power consumption of these architectures, along with super-heterodyne, is fundamentally limited by the RF oscillator and synthesizer. The stringent frequency accuracy and phase noise performance typically requires a resonant LC oscillator, usually embedded in a phase-locked loop (PLL). The limited quality factor (Q) of integrated passives leads to a typical power budget of a few hundred microwatts. In [47], an illustration of low-IF receiver implementation is described. To further reduce the power consumption, the design eliminates the typical LNA and feeds the RF input directly to the quadrature downconversion mixers. The mixers are implemented as passive switching networks using MOSFET switches, so the mixing circuits consume zero DC current. Following the mixers, the receiver circuits process the baseband signal at the low IF frequency (less than 1 MHz), so these amplifiers consume little power. To perform the downconversion operation, an oscillator is required to drive the LO port of the mixers. The oscillator must operate near the RF channel frequency with high accuracy and stability, while simultaneously driving the gates of the mixer switches with a large amplitude signal. For quadrature operation, the voltage-controlled oscillator (VCO) must also provide both in-phase and quadrature outputs. Therefore, it is not surprising that the LO generation is responsible for more than 80 % of the overall power consumption in the receiver. Despite the use of a large modulation index to eliminate the need for a complete PLL, the VCO itself still consumes more than 300 µW in single-phase, non quadrature mode. Focusing on a low-IF receiver, [3] proposes an architecture with solely a mere oscillator signal which allows to save power needed to generate and buffer the quadrature

LO signal. Quadrature generation is performed in the RF signal path and the only power consuming blocks of the receiver front-end are the VCO and the LNA. This latter has to compensate losses introduced by the poly-phase-filter and mixer. The receiver achieves a sensitivity of −102 dBm whereas consuming 26.5 mW. The LNA and frequency generation are responsible for more than 70 % of this power budget. So, despite their high sensitivity, traditional architectures are not suitable to meet the very-low power specification of compact front-ends. Clearly, the power allocated to the RF oscillator must be drastically reduced.

3.1.3 Compact Front-ends

As an alternative to frequency conversion architectures, the receiver can be implemented with just RF amplification and an energy detector, similar to the first AM receivers. This architecture, also called "tuned-RF" (TRF), eliminates the power-hungry LO altogether (Figure 3.4). There are two main drawbacks with the TRF architecture. First, selectivity must be provided through narrowband filtering directly at RF because the self-mixing operation is insensitive to phase and frequency. Second, high RF gain is required to overcome the sensitivity limitations of the energy detector, usually implemented with a nonlinear element like a diode. The TRF receiver is basically an enhanced version of the simple diode rectifiers used in RFID tags, which were shown earlier to have poor sensitivity. The addition of high frequency gain is expensive from a power perspective, so TRF receivers usually exhibit inferior sensitivity compared to mixing architectures for the equal power consumption. In [48], a TRF architecture is proposed by implementing a two-channel receiver at 2 GHz for wireless sensor networks, consuming about 3.5 mW. The receiver utilizes an OOK modulation scheme and achieves a sensitivity of −78 dBm. However, more than 80 % of the total receiver power is dedicated to the

RF gain stages, divided between the LNA at the antenna and the channel-select amplifiers. The power breakdown illustrates the critical problem with TRF architectures: providing adequate gain at RF usually requires large amounts of power. In order to overcome the gain limitations of

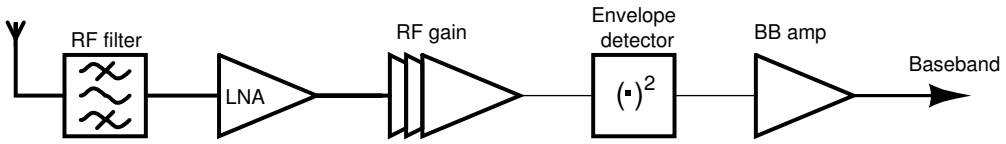


Figure 3.4: Tuned-RF (TRF) architecture

the tuned-RF receiver, a novel architecture is proposed in [49], it is called "Uncertain-IF" (Figure 3.5). Signal amplification is performed at intermediate frequency instead of radio frequency, which requires much less power consumption than TRF architectures. Another attractive aspect of the "Uncertain-IF" topology is the minimum power needed for LO signal generation. The major focus lies on how to reduce this amount of power without considering phase noise or frequency accuracy. Of course, these are important considerations for frequency conversion architectures. However, the receiver presented in [49] overcomes these problems at the architecture level, by employing an "uncertain-IF" to ease the phase noise and frequency accuracy requirements. The relaxed specifications allow the use of a free-running ring oscillator for LO generation. In fact, the LO signal must only be guaranteed to lie within some pre-determined frequency band $\pm BW_{if}$ around the RF channel frequency. Then, the exact IF frequency will vary, but the downconverted signal will lie somewhere around DC within BW_{if}. The signal is amplified at this IF frequency, resulting in substantial power savings. Finally, envelope detection performs the final downconversion to DC. The overall system performances show a power dissipation of 52 µW and a sensitivity of −72 dBm at low data rate, 100 kbit/s. The "Uncertain-IF" architecture may be viewed as super-heterodyne, where

the second downconversion is simply self-mixing, obviating the need for a precise LO at the IF frequency. However, a disadvantage of this architecture is its vulnerability to interferers. Any undesired signal within $\pm BW_{if}$ of the LO frequency that passes through the front-end filter will be mixed down and detected by the envelope detector. Therefore, a narrow and accurate RF bandpass filter is required to improve robustness to interferers. As another option to enhance gain and sensitivity at

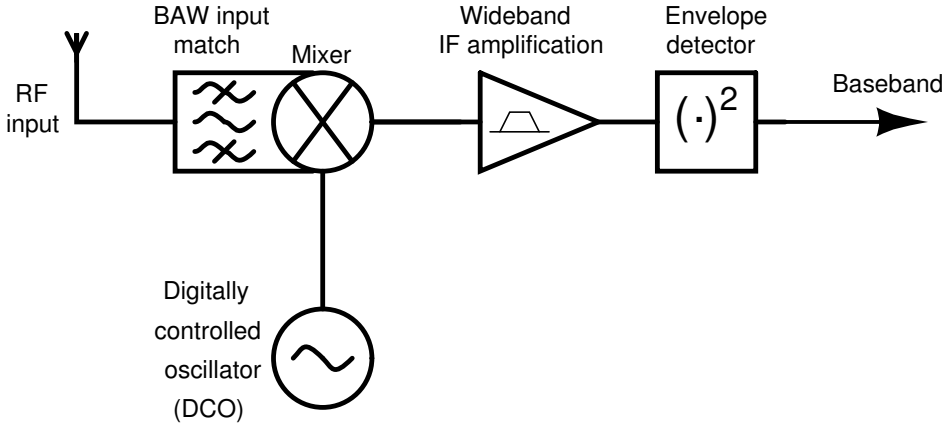


Figure 3.5: "Uncertain-IF" architecture

the same time, positive feedback or regeneration could be used in the amplifier. This technique was exploited at the beginning of wireless communication era [30] to increase the gain available from the vacuum tubes at the time. One major drawback of this technique is that the amount of feedback must be tuned and carefully controlled to improve the gain without triggering oscillation. In 1922, E. Armstrong patented the super-regenerative architecture which allows the amplifier to oscillate at RF, achieving a large amount of gain from a single stage. Thus, the need for feedback tuning is no longer necessary. [50] exploits the super-regenerative technique and demonstrates the utility of this architecture for low-power receivers. Whereas consuming 400 µW, the resulting high gain preceding the detector substantially improves sensitivity, to better

than −100 dBm. Despite the impressive performance of super-regenerative receivers, the need for a high accuracy local oscillator is mandatory, with performance requirements similar to those of the frequency conversion architectures described earlier. To circumvent this stringent bottleneck, [6] proposes a new low-power, low-complexity BPSK demodulator (Figure 3.6) that utilizes the phase response of two super-harmonic injection-locked LC oscillators to phase changes in their input signal. The injection-

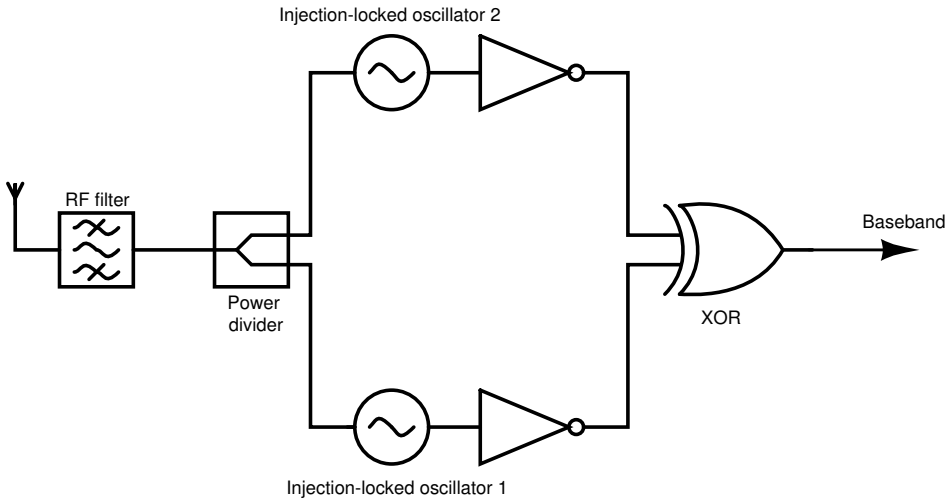


Figure 3.6: BPSK demodulator in [6]

locked oscillators must operate close to one-half of the receiver RF input frequency, while their free running frequencies are carefully chosen. Due to the inherent frequency selection of injection-locked oscillators, the need for any external or on-chip filtering is relaxed. However, owing to the limited free-running frequency offset of the oscillators, the implemented receiver achieves a sensitivity of −34 dBm. A power consumption of 120 µW is performed. In summary, simple RFID receivers are not sensitive enough for peer-to-peer links, while traditional frequency conversion architectures are inherently limited by LO power consumption. So, to circumvent these limits, several compact architectures have been proposed in the literature.

One approach is to eliminate squarely the oscillator and focus on envelope detection architectures, in this case, tuned-RF and super-regenerative receivers were revisited. Unfortunately, amplifying the input signal at RF still requires a large amount of power and reducing this latter comes at the expense of the receiver's sensitivity [51]. Another option is to relax the specifications on the local oscillator to further reduce its power dissipation. However, the burden of selectivity is shifted from LO to the front-end filter [49]. These proposed compact receivers achieve very low power consumption, few tens to few hundreds of microwatts, while performing reasonable sensitivity. Nevertheless, they are limited to a fixed modulation scheme. In this chapter, we present a new architecture based on a pulled oscillator and able to demodulate three modulation schemes: AM, FM and PM. The principle of the proposed demodulator as well as its system validation are discussed in the next section.

3.2 Modulated Oscillator for envelOpe Detection (MOOD) Architecture

In order to understand the method of operation for the proposed architecture, it is useful to review Frequency Shift Keying (FSK) modulation aspects. Binary FSK is a constant envelope modulation typically used to send digital information. The data are transmitted by shifting the frequency of a continuous carrier in a binary manner to one or the other of two discrete frequencies f_1 and f_2 as shown in Figure 3.7. A non-coherent demodulation of FSK signal can be achieved by a filter-type demodulator as depicted in Figure 3.8. The received signal is split between two parallel paths, in each path the signal is first filtered by a band-pass filter to eliminate one of the two discrete frequencies and then it is envelope detected. Finally, the envelope detector outputs are compared with a comparator

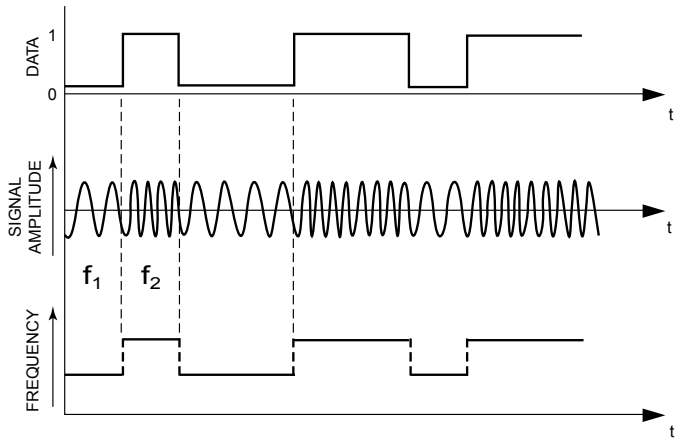


Figure 3.7: FSK modulation

to determine which has greater magnitude. Transmitted data are then reproduced. In practice, the frequency deviation of FSK modulation,

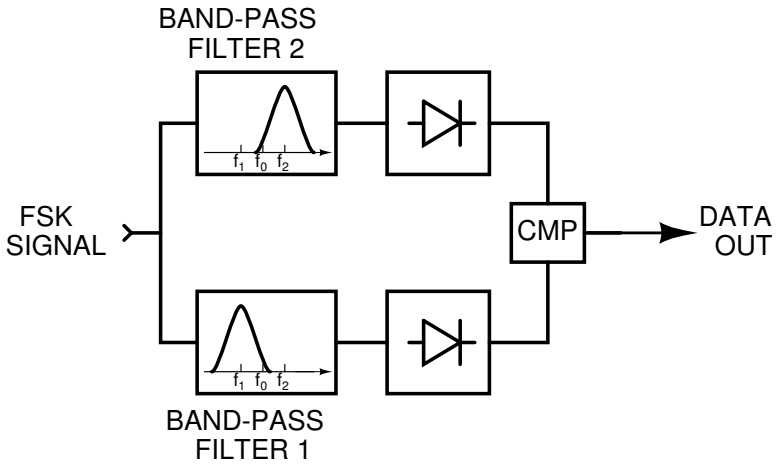


Figure 3.8: Non-coherent FSK demodulator

which fixes the shift between the two discrete frequencies, is usually in the range of few tens to few hundreds of Hz. Therefore, a narrow and accurate band-pass filter is required to perform an efficient selectivity. Such filters are in general costly and not suited with a low-power/low-cost solution. To circumvent the selectivity limitations of the previous topology, we propose a new architecture for a non-coherent demodulator.

It is composed by a band-pass filter and an envelope detector as shown inFigure 3.9. The bandwidth of the pass-band filter contains the two

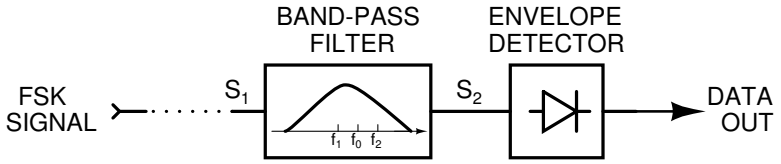


Figure 3.9: Proposed FSK demodulator

discrete frequencies f_1 and f_2 and its central frequency is different from the carrier frequency f_0. Stringent constraints on filter selectivity are now relaxed in comparison with the demodulator of Figure 3.8. It is no longer necessary to filter one of the two coding frequencies, the most important is to attenuate one frequency more than the other and then transform a frequency modulated signal into an amplitude modulated signal which can be detected by an envelope detector. In fact, since the filter frequency response is not centered on the carrier frequency f_0, the roll-off of gain is not the same for the two frequencies f_1 and f_2 which leads to a strong attenuation of one coding frequency with regards to the other. If ever the filter's frequency response is centered on the carrier frequency f_0, the FM to AM conversion will not be performed and the signal can not be demodulated, so a frequency tuned band-pass filter is required. The time evolution of the received signal through the proposed demodulator is shown in Figure 3.10. The relaxed selectivity requirements for the band-pass filter and the single signal path of the architecture extremely reduce the complexity, the power dissipation and the cost for the proposed solution in comparison with classical filter-type FSK demodulator and make it eligible to an implementation in a very low power receiver. Another attractive aspect of the proposed demodulator is its compatibility with amplitude and phase modulation. For an AM signal, it is obvious that it can be demodulated by the system since the

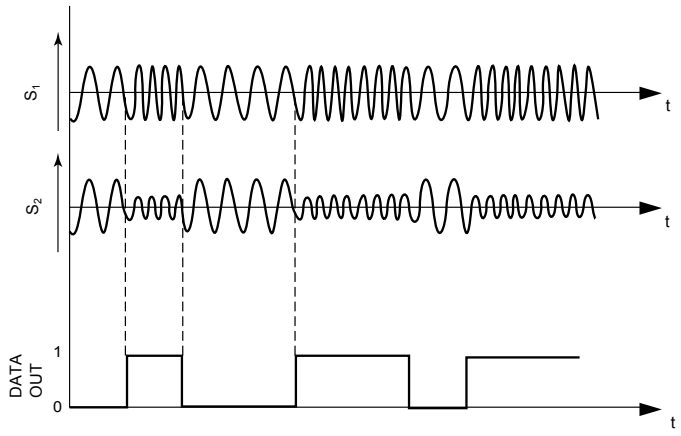


Figure 3.10: Time evolution of the received signal with the proposed architecture

envelope of the signal is already non constant. The demodulation is also performed even if the band-pass filter is centered on the carrier frequency. As discussed earlier, for FM or PM cases, if the carrier frequency falls in the center of the band-pass filter's bandwidth, thereafter, the signal is not properly demodulated; in this situation a re-calibration is required only to change the central frequency of the filter. Like any filter-type based demodulator, however, a drawback of the proposed architecture is its susceptibility to interferers. Any unwanted signal in the filter's bandwidth may corrupt the baseband signal and deteriorates the performances of the system. Therefore, an accurate RF band-pass filter is required to improve robustness to interferers.

The operating principle of the proposed demodulator was exposed and discussed; it is useful now to focus on the way in which we can efficiently implement the band-pass filter. One option is to use an LC Voltage-Controlled Oscillator (VCO). LC tank has a frequency response similar to that of a band-pass filter and can be used to transform a frequency variation into an amplitude variation; the basic operation of the proposed demodulator. However, in presence of an injected signal, the oscillator could be either locked or pulled, depending on the magnitude of the

incoming signal. While locking the oscillator is not constraining for AM signal, on the contrary, this can be profitable, a special care must be taken with FM and PM signals in order not to lock the oscillator and to have a proper demodulation. The phenomenon of injection locking or pulling [52], is a fundamental property of oscillators and should be investigated. It can be observed in a wide variety of oscillator topologies with the same qualitative behavior. Studied by Adler [53], Kurokawa [54] and others [55]-[56], these effects have found high attention because they manifest in many of today transceivers and frequency synthesis techniques. When an external periodic, voltage or current signal is mixed via the active devices, with the oscillator feedback signal, the oscillator can be locked to and track the injected signal frequency over a so called locking range. Depending on the ratio of the incident signal frequency to the oscillation frequency, different methods of injection locking are possible: fundamental, subharmonic, and superharmonic. In the first case the injected frequency is the same as the oscillation frequency while in the other two cases, the injected frequency is respectively a subharmonic or a harmonic of the oscillation frequency. If the injected signal frequency falls outside the locking range of the oscillator, the oscillator can be pulled and perturbed (instead of locked) by the external signal. To understand the mechanism of injection pulling we focus the attention on pulling by a modulated signal. Equations relating the oscillator output voltage in presence of a modulated signal are derived. Consider the simplified behavioral model for an injection pulled LC oscillator of Figure 3.11. The tank resonates at a frequency $\omega_0=1/\sqrt{LC}$ and the ideal inverting amplifier follows the tank to create a total phase shift around the loop of 2π. If the amplitude and frequency of I_{inj} are chosen properly, the circuit can continue to oscillate at ω_0 and injection pulling occurs. Under this condition, the output voltage contains both the injected signal and the free-running

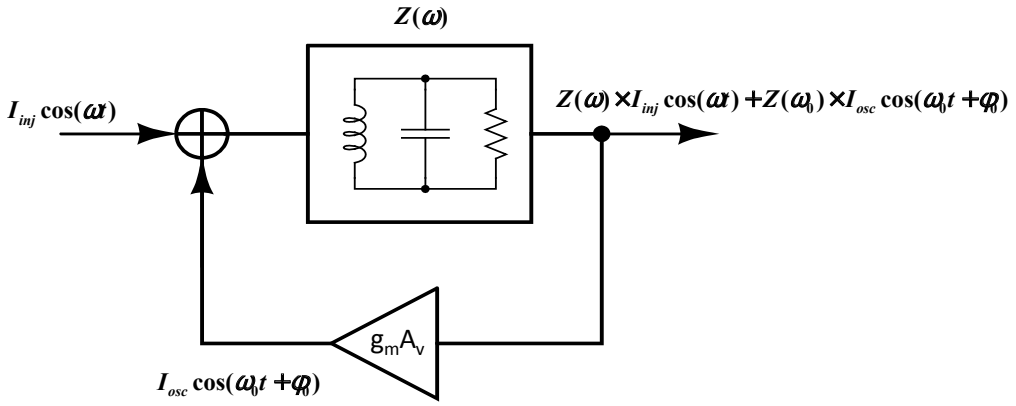


Figure 3.11: Simplified behavioral model for injection pulled oscillator

oscillation. To derive analytical equation of the output voltage when the injected signal is modulated, we assume the following simplified expression for the tank impedance:

$$Z(\omega) \approx \frac{R_p}{1 + j2Q\frac{\omega-\omega_0}{\omega_0}} \tag{3.1}$$

With R_p representing the tank losses and Q the tank quality factor. For the first case study, we consider an injected FM signal I_{FM}:

$$I_{inj}(t) = I_{FM}(t) = I_0 \cos\{\omega_c t + \beta \sin(\omega_m t)\} \tag{3.2}$$

Where ω_c and ω_m are the carrier frequency and modulating frequency respectively and β is the modulation index. The instantaneous phase and pulsation are derived as:

$$\phi(t) = \omega_c t + \beta \sin(\omega_m t) \tag{3.3}$$

$$\omega(t) = \frac{d\phi(t)}{dt} = \omega_c + \beta\omega_m \cos(\omega_m t) \tag{3.4}$$

Combining Eq 3.1 and Eq 3.2, the output voltage can be expressed as a superposition of the injected signal and the free-running oscillation:

$$V_{out}(t) = V_{inj}(t) + V_{osc}(t) \tag{3.5}$$

$$V_{out}(t) = Z(\omega) \times I_0 \cos\{\omega_c t + \beta \sin(\omega_m t)\} + Z(\omega_0) \times I_{osc} \cos\{\omega_0 t + \varphi_0\} \tag{3.6}$$

Let us focus now on the module of the output signal V_{out}:

$$|V_{out}| = |Z(\omega) \times I_0 \cos\{\omega_c t + \beta \sin(\omega_m t)\} + Z(\omega_0) \times I_{osc} \cos\{\omega_0 t + \varphi_0\}| \tag{3.7}$$

With respect to the triangular inequality we have:

$$|V_{out}| \leq |Z(\omega) \times I_0 \cos\{\omega_c t + \beta \sin(\omega_m t)\}| + |Z(\omega_0) \times I_{osc} \cos\{\omega_0 t + \varphi_0\}| \tag{3.8}$$

$$|V_{out}| \leq |Z(\omega) \times I_0| + |Z(\omega_0) \times I_{osc}| \tag{3.9}$$

$$|V_{out}| \leq R_p\{I_{osc} + \frac{I_0}{\sqrt{1 + 4Q^2(\frac{\omega - \omega_0}{\omega_0})^2}}\} \tag{3.10}$$

According to Eq 3.10, it is obvious that the module of the output voltage is modulated by the instantaneous frequency of the injected FM signal. Therefore, a pulled oscillator transforms any angle modulated signal to an amplitude modulated one, the signal's envelope is no longer constant and its variations can be detected by an envelope detector. Consider now the situation when the injected FM signal locks the oscillator. If the amplitude and frequency of I_{inj} are correctly chosen, the circuit oscillates at ω_c instead of ω_0 and injection locking occurs. Under this condition, the output voltage (V_{out}) and the injected current (I_{inj}) must bear a phase difference ϕ_{out}. It can be expressed as follow:

$$V_{out} \cos(\omega_c t + \phi_{out}) = \{I_0 \cos(\omega_c t + \beta \sin(\omega_m t)) + I_{osc} \cos(\omega_c t + \phi_{out})\} \times Z(\omega) \tag{3.11}$$

With the complex exponential notation and after some simplifications, Eq 3.11 becomes:

$$V_{out}(1 + j2Q\frac{\omega_c - \omega_0}{\omega_0}) = R_p(I_{osc} + I_0 e^{j(\beta \sin(\omega_m t) - \phi_{out})}) \tag{3.12}$$

Eq 3.12 can be separated into real and imaginary parts leading to:

$$V_{out} = R_p\{I_{osc} + I_0 \cos(\beta \sin(\omega_m t) - \phi_{out})\} \tag{3.13}$$

$$\sin(\beta \sin(\omega_m t) - \phi_{out}) = \frac{2Q}{I_0} \frac{V_{out}}{R_p} \frac{\omega_c - \omega_0}{\omega_0} \tag{3.14}$$

Equation Eq 3.13 provides the output amplitude while equation Eq 3.14 gives the output phase as a function of the injected signal frequency. The oscillator is actually locked and Eq 3.13 and Eq 3.14 have solutions for a given injected frequency ω_c. The correct expression for the locking range is found after substitution of V_{out} in Eq 3.14 from Eq 3.13 and can be found in [52][55]. However, a simplified expression can be derived noticing from eq, that for small injected currents (compared to the magnitude of I_{osc}) $V_{out}/R_p \approx I_{osc}$. Under this assumption, the double sided locking range is easily derived substituting V_{out}/R_p with I_{osc} in Eq 3.14 and requiring the last term to be in absolute value less than 1:

$$\frac{|\omega_c - \omega_0|}{\omega_0} \leq \frac{1}{2Q} \frac{I_0}{I_{osc}} \tag{3.15}$$

It is clear in Eq 3.13 that under injection locking condition, the amplitude of the output voltage does not depend on the instantaneous frequency of the injected FM signal and thus this latter can not be demodulated because FM-to-AM conversion is not performed. The case of an injected PM signal may be considered as the same of a FM signal since we have a phase variation. So it is useful to study the same previous analytical calculations with an injected AM signal, the output voltage expression is derived under pulling and locking injection cases:

$$I_{inj}(t) = I_{AM}(t) = I_0\{1 + \alpha \cos(\omega_m t)\} \sin(\omega_c t) \tag{3.16}$$

$$|V_{out}|_{AM,Pulling} \leq R_p\{I_{osc} + \frac{I_0(1 + |\alpha|)}{\sqrt{1 + 4Q^2(\frac{\omega - \omega_0}{\omega_0})^2}}\} \tag{3.17}$$

$$|V_{out}|_{AM,Locking} \leq R_p\{I_{osc} + I_0(1 + |\alpha|)\} \tag{3.18}$$

The output voltage depends on the amplitude variation of the injected signal. It is proportional to the modulation index α and achieves its maximum when the oscillator is locked. Therefore, when an injected AM

signal is applied, it is advantageous to operate under injection locking condition. From the previous analytical investigations, we can note that the LC oscillator plays a key role in the proposed architecture. When it is pulled, it converts any angle modulated signal at the input into an amplitude modulated one at the output. If it is locked, the latter conversion does not occur and the signal cannot be demodulated, however, this situation is beneficial for input AM signals since the output voltage reaches its maximum under injection locking condition and so a voltage gain can be performed. The proposed architecture may be viewed as a TRF receiver, where a modulated LC oscillator is introduced before the envelope detector to perform FM or PM-to-AM conversion required for the demodulation of angle modulated signals. For an ultra-low power receiver, the Modulated Oscillator for envelOpe Detection (MOOD) architecture holds several advantages over the architectures described in the first section of this chapter. First, LO phase noise and frequency accuracy requirements are significantly relaxed, resulting in consequent power savings. The envelope detector removes all phase and frequency content in the signal; it is only sensitive to the amplitude variation. As discussed earlier, it may be necessary to adjust the LO to ensure that it does not coincide with the RF channel when FM or PM signal is applied. In case of amplitude modulated RF signal, the fact of injecting the oscillator improves the magnitude of the output demodulated signal, this is useful to relax the decision bloc specifications, especially when digital modulation like OOK is used. Another advantageous aspect is the filtering behavior of the LC tank; it relaxes the selectivity requirements of the antenna filter. However, one drawback of the MOOD architecture is its susceptibility to blockers since they can lock the oscillator and prevent the system to work correctly. Therefore, a narrow and accurate RF filter is required.

3.3 Circuit Design

Figure 3.12 shows a block diagram of the complete MOOD system. The modulated input signal is first applied to the LC oscillator, followed directly by the envelope detector. The resulting signal is then amplified by a baseband amplifier for measurement purposes. This section describes the

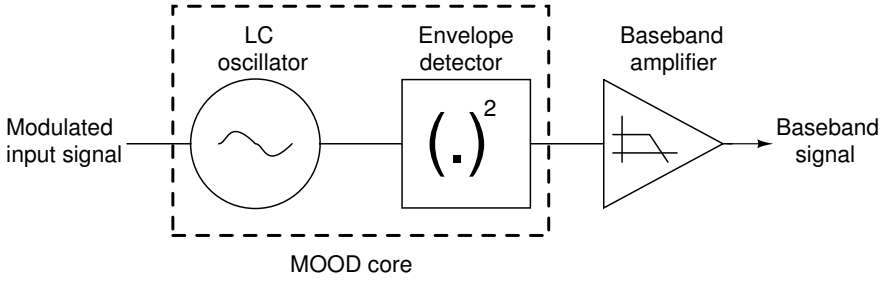


Figure 3.12: Block diagram of prototype MOOD system

design of each component in detail. In implementing each system block, the primary goal of reducing power consumption motivates simplicity in the circuit design. To further reduce power, the entire core system, which is composed by the oscillator and the envelope detector, is optimized to operate from a single 0.5 V supply.

3.3.1 LC Oscillator

The goals for this oscillator design are twofold. First, the design should consume minimal power and push the power limits of fully integrated RF oscillators. Secondly, the oscillator should be a test vehicle for the concepts of low voltage and low current design, since we have fixed the supply voltage to 0.5 V. A differential single cross-coupled LC oscillator was chosen for this design taking advantages from differential topology and the use of a single cross-coupled pair to cancel the losses in the tank, the tail device is used to inject the RF signal in order to modulate the oscillations. It is true that the complementary topology [57], using both

NMOS and PMOS cross-coupled pairs, is popular, as it improves phase noise, but it is also impractical for this design because it contains three stacked transistors. In order to enable operation on a low voltage supply, a standard topology is chosen with NMOS cross-coupled pair and NMOS tail device for biasing.

Oscillator Core

The schematic of the final core oscillator with input matching is shown in Figure 3.13.

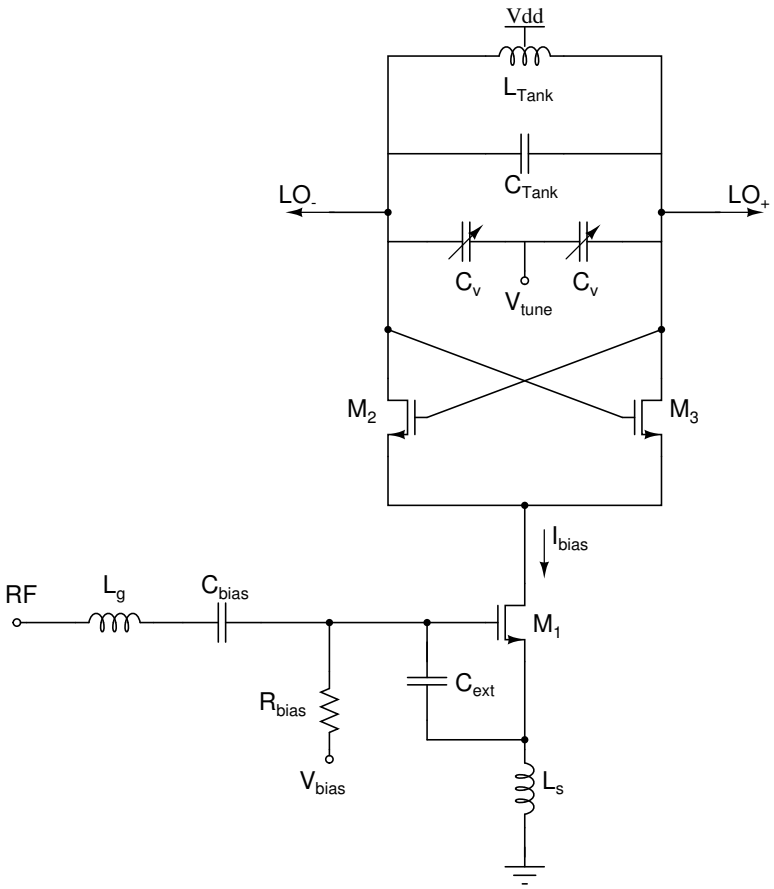


Figure 3.13: Schematic of the oscillator core

The core bias current I_{bias} through tail transistor M_1 is controlled by externally applied voltage V_{bias} on the gate of M_1. The required bias current is determined by both startup and output swing specifications. In order to decrease efficiently the power consumption of the oscillator, a loss budget of the tank must be established in order to determine the necessary negative transconductance provided from the cross-coupled pair which is equal to -1/$g_{m2,3}$ in small-signal regime. The required g_m for startup

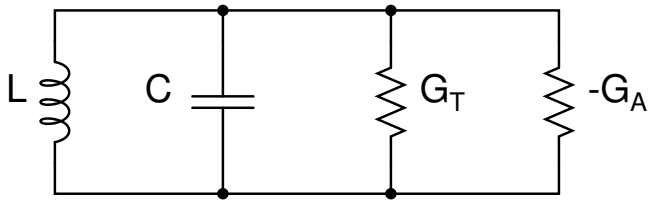


Figure 3.14: Simple model of oscillator as resonant tank

establishes a lower limit on the current consumption of the oscillator. At the resonant frequency, the LC tank may be modeled as depicted in Figure 3.14, where the tank losses are contained in the conductance G_T. The equivalent parallel resistance at resonance may be calculated by treating the capacitor as lossless and calculating the parallel conductance G_T for an inductor with finite Q given by the overall tank quality factor:

$$R_{p,tank} = \frac{1}{G_T} = Q_{tank}\omega L \tag{3.19}$$

Figure 3.15 depicts the tank losses $R_{p,tank}$ versus frequency. At resonant frequency 2.4 GHz, the estimated $R_{p,tank}$ is 1290 Ω. Therefore, the minimum g_m required for startup is:

$$g_{m,crit} = \frac{1}{R_{p,tank}} \approx 0.77\,\text{mS} \tag{3.20}$$

To ensure a reliable startup, the cross-coupled pair is designed to have a transconductance that is at least twice the minimum value. The specified transconductance is therefore fixed at 1.6 mS. Equation Eq 3.19

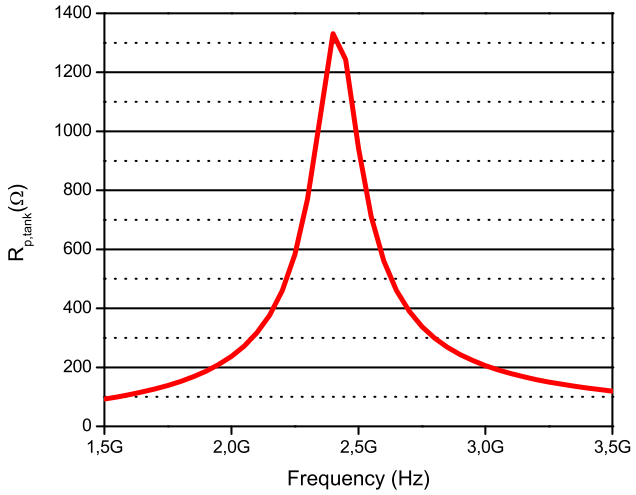


Figure 3.15: Tank losses

shows explicitly why large inductance values are beneficial from a power consumption perspective; for a given Q, the parallel tank resistance is directly proportional to the inductance L. For a given operating frequency, therefore, it is desirable to use the largest possible inductor in the LC tank, reducing the tank capacitance appropriately. In practice, the size of the inductor is usually limited by the difficulty of implementing large on-chip coils; inductors larger than 10nH are hardly integrated. The importance of high Q inductors is also plain from Equations Eq 3.19 and Eq 3.20. The critical transconductance for startup is inversely proportional to tank quality factor, so an improvement in inductor Q leads directly to reduced startup current requirements and lower power consumption. To further optimize the current efficiency for minimal bias current, devices M_2 and M_3 are designed to operate between weak and moderate inversion region. Referring to Figure 2.38 in chapter 2, g_m/I_D of around 15 is achievable in this range. The total bias current sourced by M_1 is designated I_{bias}, and the current flowing in either M_2 or M_3 is therefore $I_{bias}/2$. As dis-

cussed above, at the target inversion level the device g_m will be 15 times higher than the bias current. The required transconductance for startup is 1.6 mS, leading to a first estimate of 200 µA for the nominal bias current. Moderate inversion region is a good compromise for transistor M_1 to achieve at the same time a high current efficiency and maximum gain at RF for a given current. Figure 3.16 shows the phase noise of the oscillator versus the bias current. As outlined in section 2.3 of chapter 2, when the

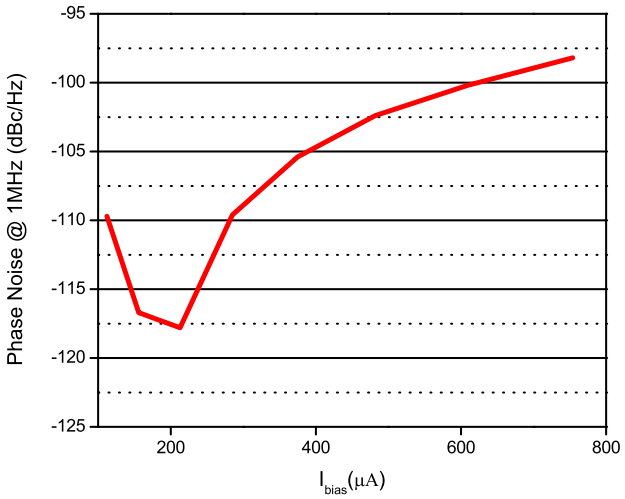


Figure 3.16: Phase noise versus bias current I_{bias}

oscillator operates in the current-limited region, as the tail current increases, the output amplitude increases. As a result phase noise improves as I_{bias}^2. Phase noise also improves linearly with the inductance value. In current-limited mode, the phase noise improves of 6 dB doubling the current consumption and of 3 dB doubling the inductance value. When the output amplitude is supply limited, an increase in bias current does not provide an equal increase in output swing; the differential pair's noise contribution to noise factor rises, degrading phase noise proportionally to I_{bias}. Minimum phase noise is achieved at the transition between current

and voltage limited regions.

Output Buffer

Output buffers are necessary for measurement in order to drive instrumentation with 50 Ω inputs. The only requirement for the buffer is that it should not load the oscillator excessively. An NMOS source follower topology was chosen due to its low input capacitance and flat gain response over a wide range of frequencies. A schematic of the output buffer design is depicted in Figure 3.17. The output impedance of the follower can be approximately considered to be $1/g_{m4}$, requiring:

$$50\,\Omega = \frac{1}{g_{m4}} \Rightarrow g_{m4} = 20\,\text{mS} \tag{3.21}$$

For high bandwidth and low input capacitance, transistor M_4 is sized to operate in strong inversion. When driving a 50 Ω load, the simulated gain of the buffer is roughly −1 dB up to 10 GHz. The output return loss is about −20 dB at the operating frequency, 2.4 GHz. The buffer operates from a separate 1 V supply to facilitate oscillator core testing with a wide range of supply voltages. Since the oscillator DC output level varies with the supply voltage, the buffer is AC-coupled to the oscillator output through a 10 pF metal-insulator-metal (MIM) capacitor, forming a 1 MHz high-pass response. A MIM capacitor was chosen because of its high quality and small backplate parasitics. A low-pass filter (R_f,C_f) is added to reduce the noise contribution of the current mirror. Resistor R_S degenerates the source of transistors M_5 and M_6 to improve the current mirror's stability. The total current consumption of each buffer, including biasing, is about 3.6 mA from a 1 V supply. The final device types and aspect ratios are summarized in Table 3.1.

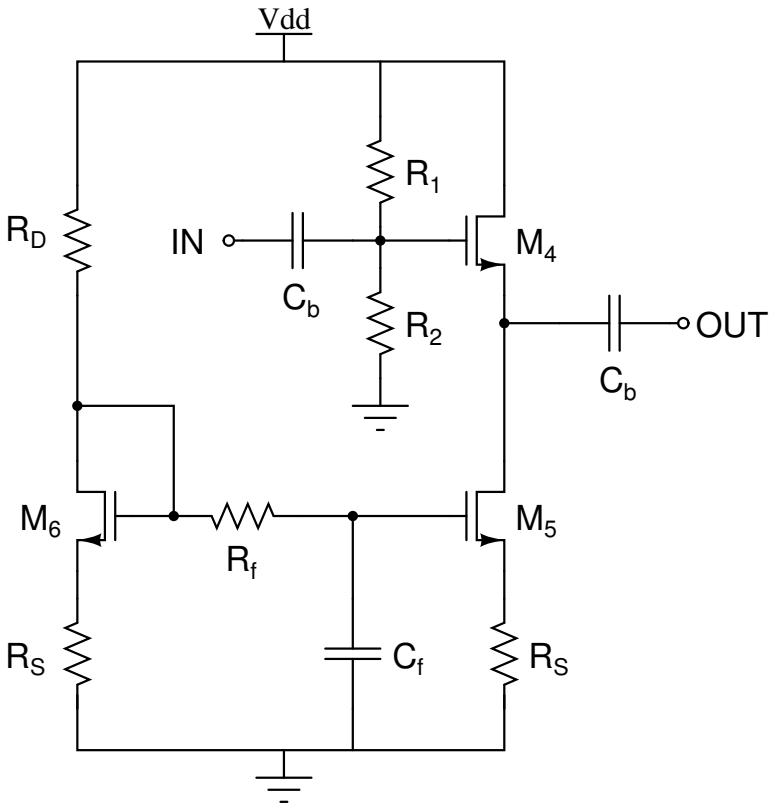


Figure 3.17: Schematic of the output buffer

Table 3.1: Sizes of Oscillator devices (Core and buffer)

Device	Size	Device	Size
M_1(W/L)	20 µm/0.06 µm	C_{bias}	5 pF
$M_{2,3}$(W/L)	15 µm/0.06 µm	C_b	10 pF
M_4(W/L)	25 µm/0.06 µm	C_f	5 pF
$M_{5,6}$(W/L)	15 µm/0.06 µm	R_{bias}	5 KΩ
L_g	5 nH	R_f	5 KΩ
L_s	5 nH	R_1	15 KΩ
L_{tank}	6 nH	R_2	30 KΩ
C_{tank}	530 fF	R_D	900 Ω
C_{ext}	450 fF	R_S	10 Ω
C_v	5 µm/1 µm		

3.3.2 Envelope Detector

The first step is to determine the nonlinear response of the envelope detector. The detection circuit can be implemented using any nonlinear circuit element, such as a diode. However, in a CMOS process it is convenient to realize the detector with the circuit shown in Figure 3.18 [58]. This circuit is a CMOS version of the standard bipolar topology described in [59], and is basically a band-limited source follower. The operation of the circuit in CMOS is similar to the bipolar version if device M_1 is biased in weak inversion, where its drain current is an exponential function of gate-source voltage instead of the weaker nonlinearity of square-law behavior in strong inversion. Device M_2 acts as a simple current source to bias M_1 with a constant current. A large filter capacitor C_f is connected to node V_{out}. The bandwidth at the output is set by the pole $f_{p,det}$ formed by C_f and the output impedance of the detector, which is

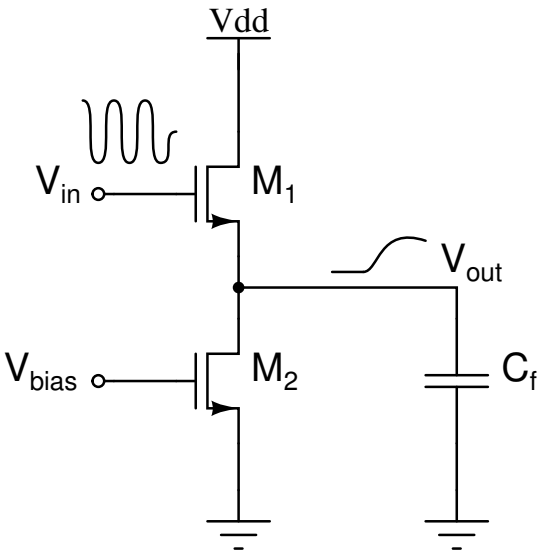


Figure 3.18: Schematic of basic envelope detector circuit in CMOS

approximately $1/g_{m1}$ neglecting body effect:

$$f_{p,det} = \frac{g_{m1}}{2\pi C_f} \tag{3.22}$$

This pole is designed to be low enough to filter out any signal at the fundamental and higher harmonics, while still affording enough bandwidth to avoid the baseband signal attenuation. For a typical OOK signal, the detected baseband waveform is a square wave with a given baseband data rate, so the detector bandwidth must be high enough to avoid filtering this desired signal. An AC input signal is applied to the input at V_{in} in Figure 3.18. Since the output bandwidth is much smaller than the input signal frequency, the full signal appears across the gate-source terminal V_{GS} of M_1. Device M_1 generates an output current that is an exponential function of the input voltage. The nonlinear transfer function contributes a DC term at the output in response to the AC input signal. In order to calculate a simple expression for the effective conversion gain from input AC to output DC, the exponential can be approximated by using Taylor series expansion and dropping terms above the second order. This

yields the simple model shown in Figure 3.19, where the detector circuit is modeled as squaring function that converts an input voltage V_{in} to an output current i_o. The linear term at the fundamental frequency, along

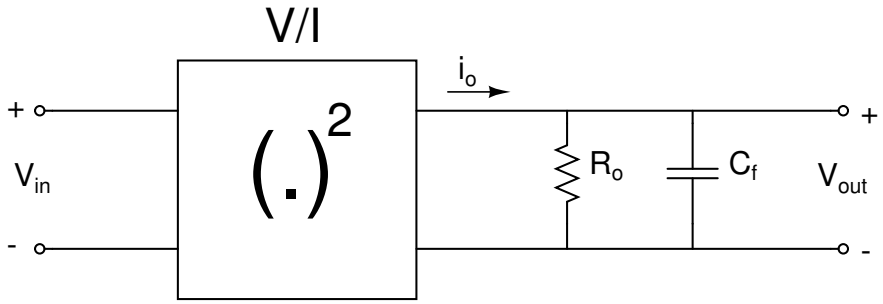


Figure 3.19: Simple model of envelope detector to calculate conversion gain

with higher order harmonics, will be filtered out by C_f. Although higher order terms will also generate DC components, these contributions are small compared to the squaring term. The output impedance R_o is simply $1/g_{m1}$. Using the model in Figure 3.19, the conversion gain G from the AC input voltage to the DC output response can be calculated. First, the large signal drain current of M_1 in weak inversion is modeled as [60]:

$$I_D = I_0 e^{(\frac{V_{GS}-V_{th}}{nV_t})}\{1 - e^{(\frac{-V_{DS}}{V_t})}\} \tag{3.23}$$

$$I_D \approx I_0 e^{(\frac{V_{GS}-V_{th}}{nV_t})} \tag{3.24}$$

Where I_0 is a constant depending on process and device size, V_{th} is the threshold voltage, V_t is the thermal voltage (kT/q), and n is the subthreshold slope factor. The variables V_{GS} and V_{DS} are the gate-source and drain-source terminal voltages, respectively. The approximation of I_D holds when the transistor is in saturation, which is valid for this source follower circuit. Next, we find DC output signal i_0 in Figure 3.19 due to an input signal V_{in}=$V_s$sin($\omega_s t$). Expanding Eq 3.23 in a Taylor series and focusing on the second order term:

$$i_0 = \frac{V_{in}^2}{2}\frac{d^2 I_D}{dV_{in}^2} \tag{3.25}$$

$$i_0 = \frac{V_{in}^2}{2}\frac{d}{dV_{in}}(\frac{I_D}{nV_t}) \tag{3.26}$$

$$i_0 = \frac{V_{in}^2}{2}\frac{I_D}{(nV_t)^2} \tag{3.27}$$

Substituting for V_{in} and recognizing that $I_D/\mathrm{n}V_t{=}g_m$:

$$i_0 = \frac{g_m}{2nV_t}V_s^2\sin^2(\omega_s t) \tag{3.28}$$

$$i_0 = \frac{g_m}{2nV_t}V_s^2\{\frac{1-\cos(2\omega_s t)}{2}\} \tag{3.29}$$

The second harmonic term will be filtered by the detector output pole, giving a DC output current:

$$i_0 = \frac{g_m}{4nV_t}V_s^2 \tag{3.30}$$

Finally, we arrive at the DC output voltage by multiplying the output signal current by the detector output impedance:

$$V_{out} = i_0 R_0 = \frac{i_0}{g_m} = \frac{V_s^2}{4nV_t} \tag{3.31}$$

Therefore the voltage conversion gain G from peak AC input amplitude V_s to output DC voltage V_{out} is given by:

$$G = \frac{V_{out}}{V_s} = \frac{V_s}{4nV_t} \tag{3.32}$$

The derivation above holds for small input signals where the response is dominated by the second order term and higher order effects are not significant. For the purposes of analyzing the detector sensitivity, the signals of interest are small and the simple form of Eq 3.32 is a convenient way to represent the detector response. Using the full Bessel function representation in [59], a more accurate expression for gain can be derived. The simulation result is depicted in Figure 3.20. The envelope detector was implemented in a 65 nm CMOS process with $(W/L)_1{=}(15\,\mu\mathrm{m}/0.18\,\mu\mathrm{m})$ and bias current of 2.5 µA. Interestingly, Equation Eq 3.32 predicts that the gain is independent of the device sizing and transconductance. The

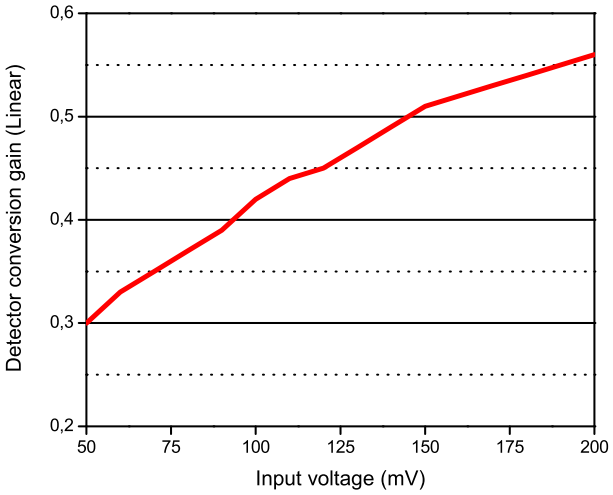


Figure 3.20: Simulated conversion gain of the envelope detector

derivation above assumes that the device drain current follows an exponential characteristic, so the transistor must be biased in weak inversion. In order to minimize loading on the preceding oscillator, the detector device sizing should be optimized for low input capacitance while still maintaining the device in weak inversion. In deep submicron technologies like 65 nm, minimum channel length should also be avoided due to the high drain-source conductance g_{ds} observed for devices with short channel length. An additional consideration is the output bandwidth, which is determined by the output pole (Eq 3.22) and may affect the bias design. Finally, the transistor may need to be sized larger to lower flicker noise, if it becomes dominant in the overall receiver noise calculation. It should be emphasized that this G factor is the conversion gain for high frequency signals at the detector input. Any input signals, including noise, at frequencies below the detector output bandwidth will experience the linear transfer function instead, with approximately unity gain ($G_{DC} \approx 1$). Since the oscillator output is differential, the envelope detection circuit is

implemented with a differential pair biased in weak inversion with 2 µA of current per side for maximum nonlinearity. A schematic of the differential envelope detector is shown in Figure 3.21. When a differential RF signal

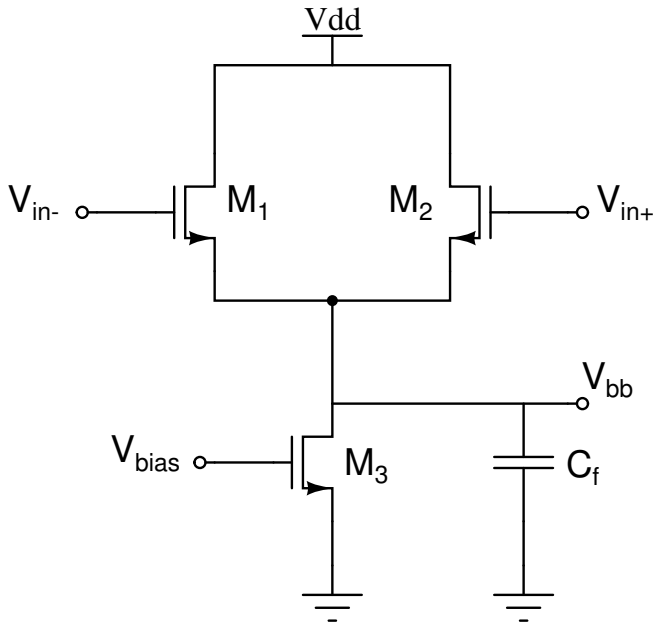


Figure 3.21: Circuitry of the differential envelope detector (Bias not shown)

drives the gates of M_1 and M_2, the nonlinear bias point shift appears at the drain of the tail current source, converting the RF energy to a DC baseband signal. In order to avoid loading the oscillator excessively, the detector pair must not be sized too large. Devices M_1 and M_2 have an aspect ratio of (15 µm/0.18 µm), with current source device M_3 sized at (5 µm/0.06 µm). A 50 pF capacitor at the output filters any feedthrough from the RF signal or higher harmonics, with a baseband bandwidth of about 700 kHz. Table 3.2 summarizes the final device types and aspect ratio.

Table 3.2: Sizes of envelope detector devices

Device	Size	Device	Size
$M_{1,2}$(W/L)	15 µm/0.18 µm	$g_{m1,2}$	74 µS
M_3(W/L)	5 µm/0.06 µm	g_{m3}	50 µS
C_f	50 pF		

3.3.3 Baseband Amplifier

Signals at the output of the envelope detector are quite small with about few millivolts, so a baseband amplifier is needed here in order to deliver a measurable signal to the test equipments, in our case it will be an oscilloscope probe. The circuit is based on a basic common source topology with resistive load as depicted in Figure 3.22. The input is AC coupled

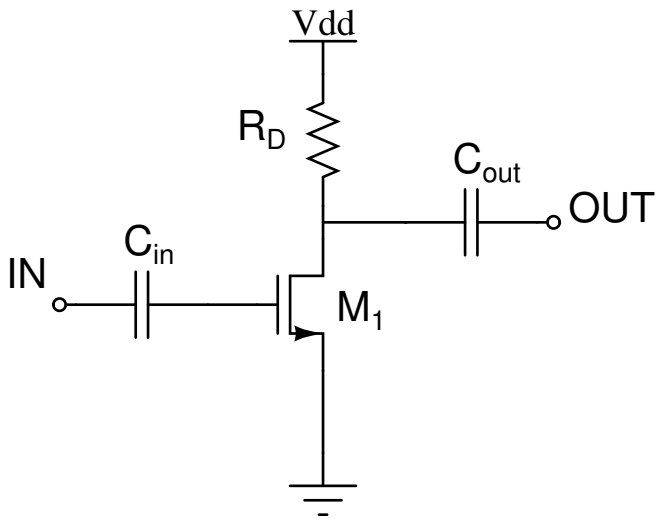


Figure 3.22: Schematic of the baseband amplifier (Bias not shown)

to the envelope detector as shown in Figure 3.22. Transistor M_1 is sized (20 µm/0.18 µm) and biased in moderate inversion with maximum channel length for higher gain and acceptable gain bandwidth. The designed bandwidth must be high enough to avoid attenuating the baseband signal. The

−3 dB bandwidth is marked in Figure 3.23, verifying that the baseband amplifier has a gain of 12 dB across the band from 1 kHz to 10 MHz, While consuming 350 µA from 1.2 V supply voltage.

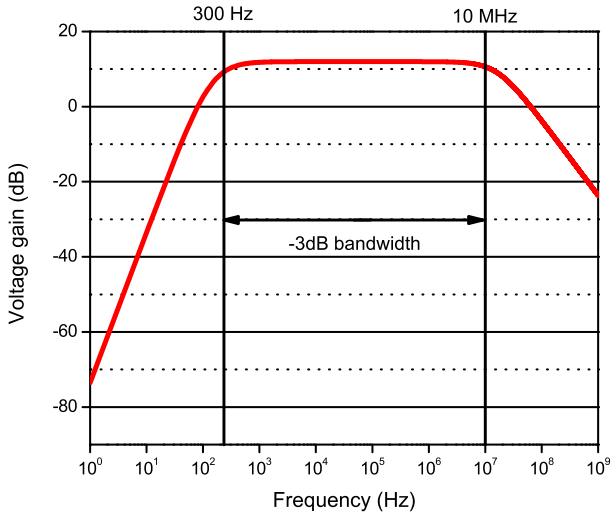


Figure 3.23: Simulated baseband amplifier frequency response

The devices size of the baseband amplifier are reported in Table 3.3.

Table 3.3: Sizes of baseband amplifier devices

Device	Size
M_1(W/L)	20 µm/0.18 µm
C_{in}	90 pF
C_{out}	80 pF
R_D	1 kΩ

3.4 Results

After the description of the system design parameters, the system simulations and measurement results are presented and discussed in this section.

3.4.1 Complete System Post-layout Simulations

In order to validate the analytical calculations of section 3.2, system simulations were performed using Goldengate simulator in Cadence environment and after extracting parasistic capacitors and resistors. First, the oscillator voltage gain is simulated when an AM signal is applied. Then, system validation results with OOK and FSK modulation are presented. Figure 3.24 shows the spectrum at the output of a pulled LC oscillator

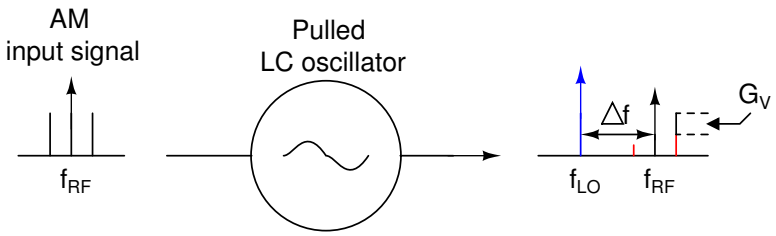


Figure 3.24: Pulled oscillator's output spectrum in presence of AM signal

when an amplitude modulated signal is applied. In this case we define the oscillator's voltage gain as the ratio of the highest output sideband level of the AM signal over its input sideband level. This voltage gain versus Δf is depicted in Figure 3.25. It is clear that the oscillator performs more gain when the RF signal is close to the LO one. As we move away the free-running frequency, the voltage gain drops and follows the frequency response of the LC tank. Therefore, when AM signal is applied, it is better to operate closer to the LO frequency and even inject the oscillator, where the maximum gain is achievable. This helps to improve the sensitivity of the system. To further confirm the comments above,

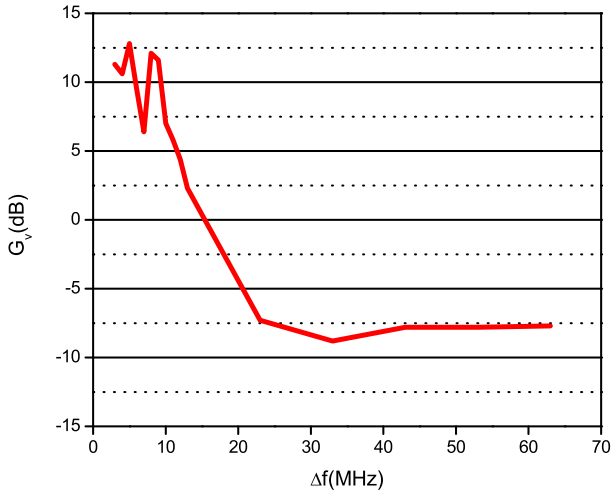


Figure 3.25: Oscillator's voltage gain versus Δf

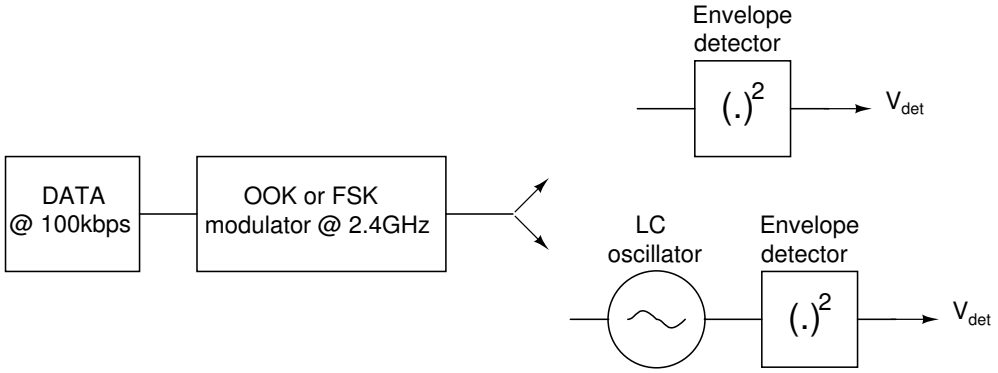


Figure 3.26: Testbench simulation for system validation

system simulations were realized with OOK and FSK modulation scheme testbench as shown in Figure 3.26. The data rate is fixed to 100 kbit/s and the carrier frequency to 2.4 GHz with zero-peak voltage of 20 mV. LO frequency is tuned to achieve different simulation setups. Figure 3.27 shows the voltage amplitude V_{det} at the envelope detector's output in the case of OOK modulation and for different distance Δf between the RF and LO frequencies.

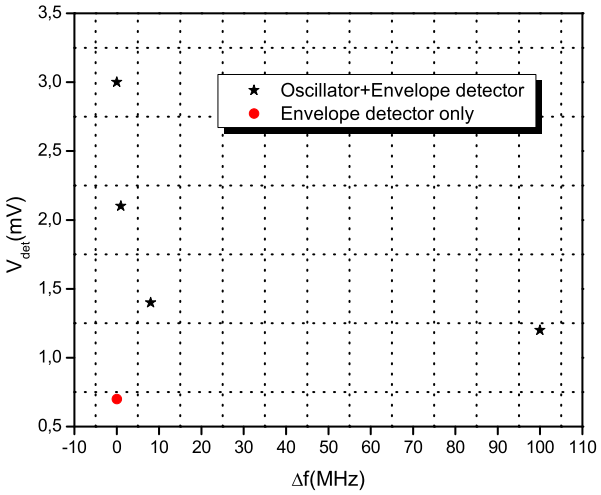


Figure 3.27: Envelope detector's output voltage in OOK setup

What we can note from Figure 3.27 that a larger amplitude at baseband signal can be obtained when the oscillator is added before the envelope detector; this could be attractive especially in relaxing constraints on LNA and improving the required SNR for demodulation. Another advantageous aspect in introducing the oscillator is the part of selectivity that can be achieved when the oscillation frequency is close to the RF frequency; it could be beneficial for relaxing the antenna filtering. Concerning the case of FSK modulation, the envelope detector could not demodulate the signal since it is insensitive for frequency and phase variations. The fact of adding the oscillator helps for demodulation. The LC tank converts the frequency modulated signal to an amplitude modulated one, due to its frequency response and then the envelope detector can pick up the envelope variation. In this case, an output voltage, V_{det}, of 600 µV is achievable with a modulation frequency shift of 1 MHz.

3.4.2 Measurement Results

The prototype system was fabricated in 65 nm standard CMOS technology from STMicroelectronics. All measurements were performed with single-ended ground-signal-ground (GSG) probe at the input and a differential GSGSG probe to sense the LO output. A bias-T was introduced at the input port for variable DC bias voltage to control the transconductance stage of the oscillator. Oscillation frequency and output power were measured with a Rhode&Schwartz FSUP (20 Hz-26.5 GHz) source analyzer. The modulated signals were generated by a Rhode&Schwartz signal generator and the time domain measurements were obtained with an Lecroy wavepro 960 2 GHz oscilloscope. Finally, supply and bias voltage were generated by Agilent E3631A DC power supply.

Standalone envelope detector and LO measurements

The LC oscillator and the envelope detector are two main blocks in MOOD system. standalone test blocks are included on the prototype chip for characterization purposes. A die photo of the single envelope detector is depicted in Figure 3.28. The total area is about 0.64 mm^2. The circuit consumes 1.5 µA from 0.5 V supply. For system functionality, the most

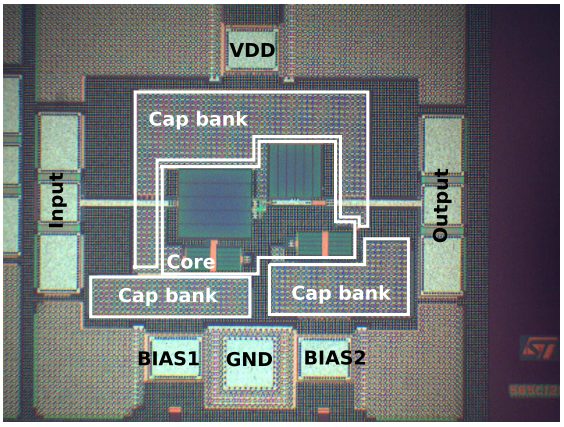
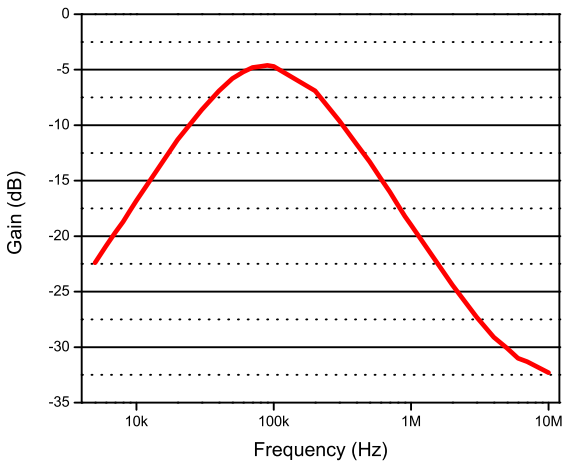
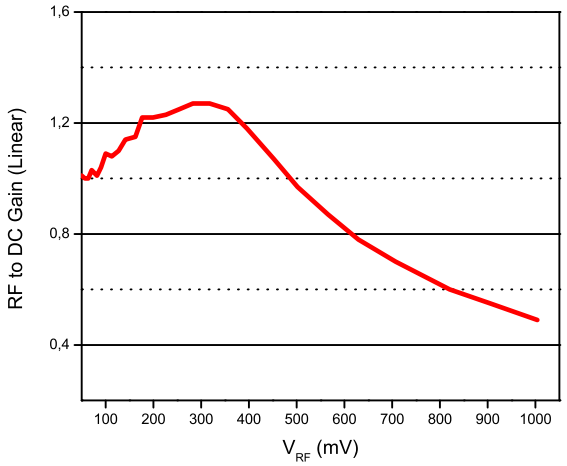


Figure 3.28: Die photo of the envelope detector

important features for the envelope detector are its bandwidth and conversion gain, they are reported in Figure 3.29. The achievable bandwidth



(a) Bandwidth



(b) Conversion gain

Figure 3.29: Measured bandwidth and conversion gain of the envelope detector

is about 300 kHz, quite enough to address low data rate specification for wireless sensor networks. However, detector conversion losses must be compensated by the oscillator to perform better sensitivity. In Figure 3.30, a

die photo of the oscillator is shown. The total area is 1.1 mm^2. As defined

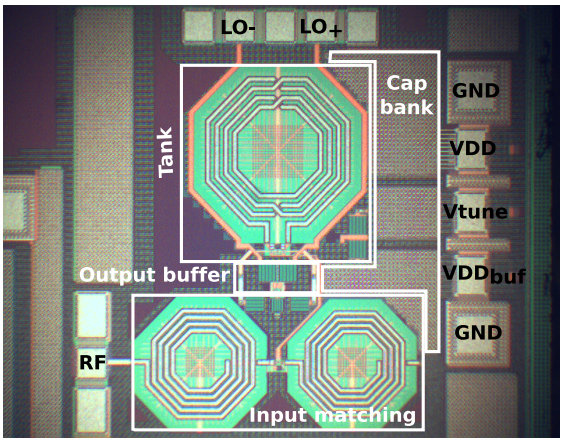


Figure 3.30: Die photo of the LC oscillator

in section 3.3.1, the nominal oscillator bias conditions are I_{bias}=200 µA and V_{DD}=0.5 V. Figure 3.31 shows a capture of the output spectrum. The nominal oscillation frequency is 2.56 GHz with −24 dBm output power at the buffer output. The oscillator is designed to be tested over a wide range

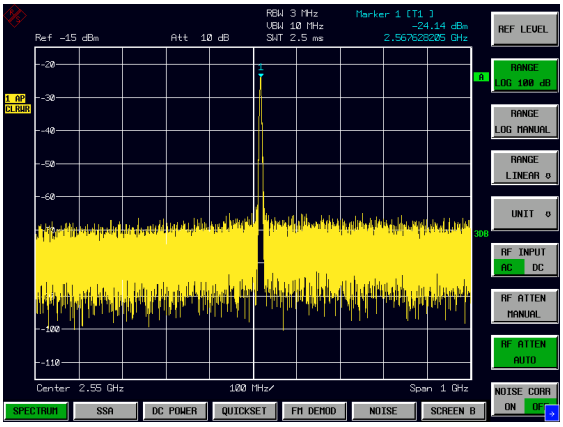


Figure 3.31: Measured output spectrum

of bias points in order to verify performance at low supply voltages along with various levels of inversion. Oscillation frequency and output power are the two performance metrics of interest; accordingly, two different parameter sweeps were performed. First, the tail transistor is kept in

moderate inversion region while the supply voltage is varied. This verifies the functionality at low supply voltages. Secondly, the bias current is swept while supply voltage is held constant at a nominal value. This measurement demonstrates the performance for different transistor regions of operation. Figure 3.32 shows the measured oscillation frequency and output power as V_{DD} is swept from 0.5 V to 1 V. The nonlinear device

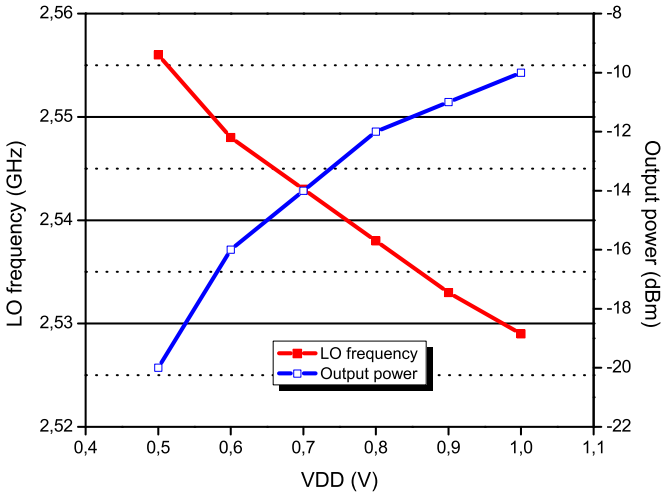


Figure 3.32: Measured oscillation frequency and output power for different V_{DD}

capacitance changes with applied voltage, so the oscillation frequency varies across the supply range. For very low supply voltages, below 0.5 V, the drain-source voltage of the tail current source transistor is compressed and the device enters the triode region. Beyond this point, it becomes difficult to keep the tail transistor in MI region, the bias current falls and therefore the output voltage swing also. Figure 3.33 presents the variation of frequency and output power, when the supply is held constant at 0.5 V and bias current is swept from 200 µA to 1500 µA. On the lower end, the bias current is reduced until the oscillator no longer starts up with the adequate robustness. Varying the bias current also changes

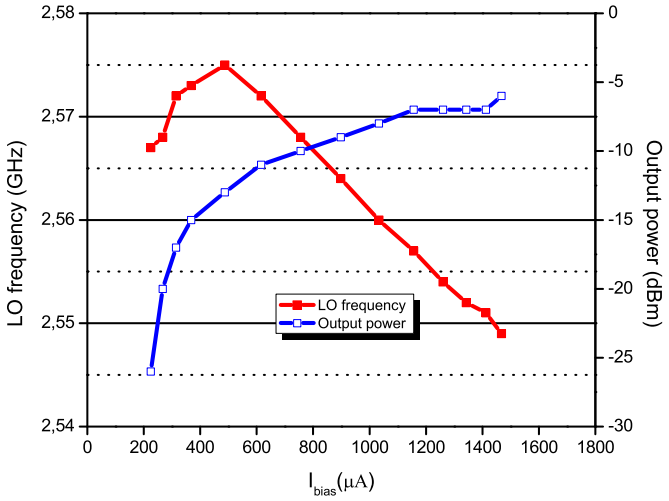


Figure 3.33: Variation of oscillation frequency and output power for range of I_{bias}

the nonlinear device capacitance and therefore the oscillation frequency. Note that Figure 3.33 illustrates a linear dependence of output power on bias current, between 200 and 400 µA, confirming that the oscillator is operating in the current-limited regime. This is because the output swing is small enough and is not being limited by the available voltage headroom. In order to measure phase noise, all supply voltage generators were turned off to reduce their noise contributions. Bias voltages are internally generated except for V_{bias} which controls the oscillator tail current. For this measurement, V_{DDosc} and V_{DDbuf} are set at 0.5 V and 1 V respectively. Figure 3.34 illustrates the effect of bais current variation on phase noise at a fixed 1 MHz offset. Spot noise is plotted for Ibias ranging from 200 µA to 1500 µA. The phase noise exhibits a minimum phase noise of −100 dBc/Hz in MI region. Beyond this point, the phase noise increases rapidly since the oscillator operates in voltage-limited regime. To measure the oscillator's tuning range, the varactor drain/source voltage is tuned from 0 V to 2 V.

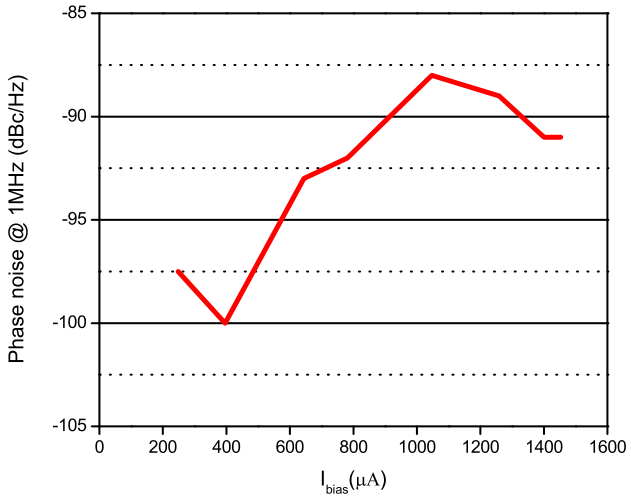


Figure 3.34: Oscillator's phase noise for different bias current

Figure 3.35 demonstrates a frequency variation from 2.53 GHz to 2.64 GHz which corresponds to a tuning range of 4.2 %.

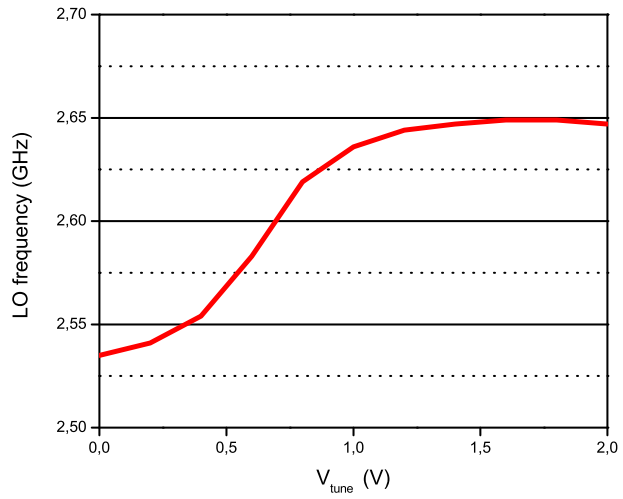


Figure 3.35: Tuning range of the oscillator

The oscillator is the main block in MOOD system since it performs, under pulling condition, the FM-to-AM conversion required for demodulation. So, it is important to examine the oscillator's frequency response when an external signal is applied. For this measurement, the oscillator is held at nominal bias conditions and a continuous wave is injected with a total power of −31 dBm. First, as depicted in Figure 3.36, the frequency of this continuous wave is changed and its power level is measured at the oscillator's output. The output power follows the frequency response of the free-running oscillator with a maximum achievable gain of 6 dB at 1 MHz shift from the free-running oscillation. Beyond this frequency shift, the oscillator is locked. Therefore, the locking range is about 2 MHz. In

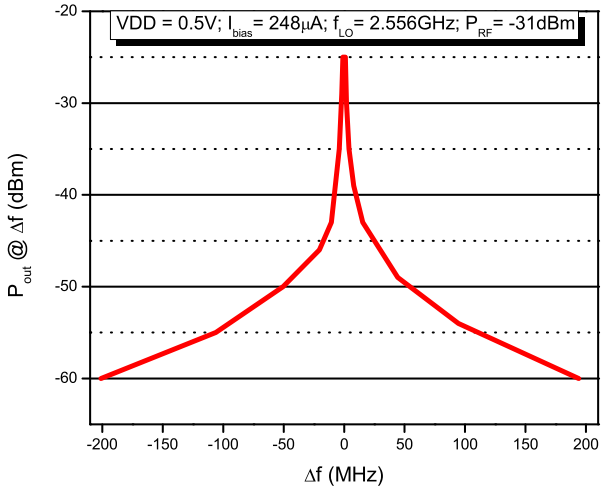


Figure 3.36: Output power for different frequencies of a continuous wave

Figure 3.37, the required power to lock the oscillator is measured for different frequency distance between the LO signal and the injected one. It is clear that as we get far from the free-running oscillation, a larger amount of power is required to lock the oscillator. This point limits the sensitivity of the overall system.

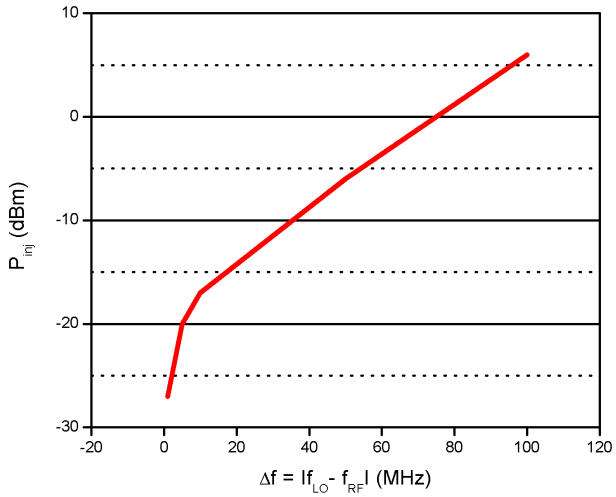


Figure 3.37: Required injection power for different Δf

System measurements with analog modulation schemes

In this section the validation of MOOD system is demonstrated with different analog modulation types (AM, FM and PM). As depicted in Figure 3.38, a modulated signal is applied and the demodulated peak-to-peak voltage is measured at the output. Different setups were carried out for characterization. Figure 3.39 shows the amplitude of the demodulated

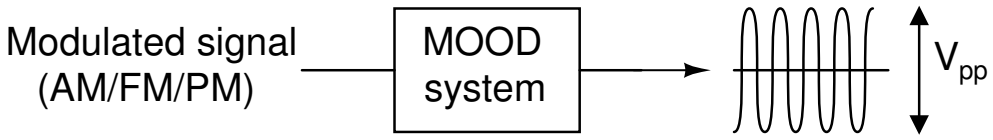
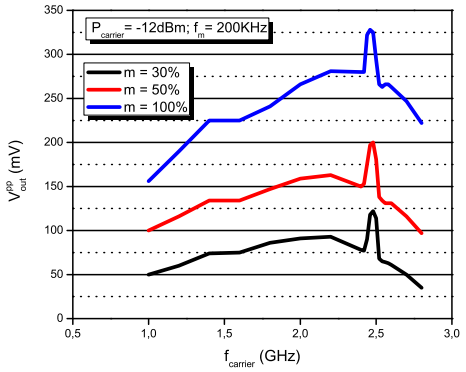
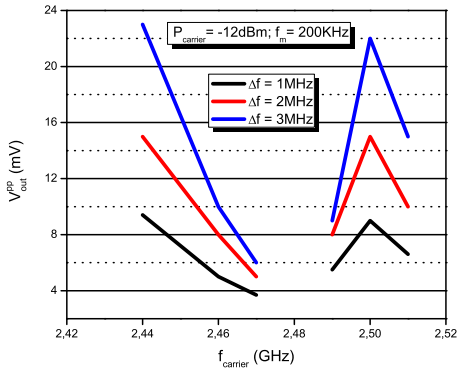


Figure 3.38: Measurement setup for system validation

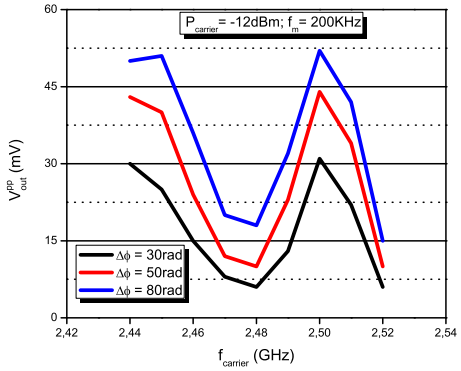
signal in case of AM, FM and PM input signal and this for different carrier frequencies $f_{carrier}$. The modulating frequency f_m and the carrier power level $P_{carrier}$ were kept constant at 200 kHz and -12 dBm respectively, while the modulation depth is changed. The free-running oscillation is fixed to 2.48 GHz under nominal bias conditions.



(a) AM



(b) FM

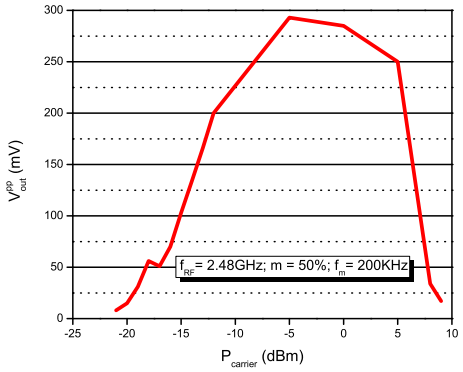


(c) PM

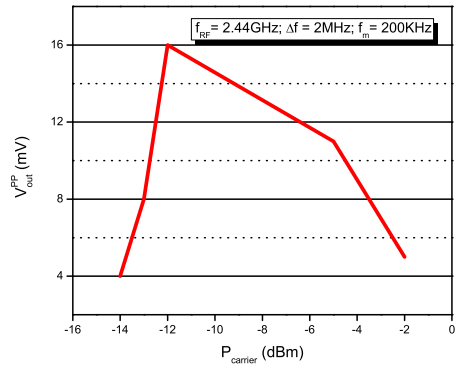
Figure 3.39: Demodulated amplitude versus $f_{carrier}$

The peak-to-peak output voltage increases with modulation depth in all configurations (AM, FM and PM). In AM case (Figure 3.41a), the demodulated amplitude grows linearly as the carrier frequency is close to the LO one. It reaches its maximum when the oscillator is locked. However, in FM and PM cases, the fact of locking the LO does not help to demodulate the signal. These measurement results confirm the analytical calculations discussed in section 3.2. In Figure 3.40, the carrier power $P_{carrier}$ was varied, whereas the carrier and modulating frequencies were kept constant. An idea about the sensitivity range for MOOD system could be deduced from these results. When an AM input signal is applied, a carrier power level of -20 dBm helps to get 20 mV of peak-to-peak output voltage. On the other hand, the sensitivity is lower in case of FM or PM input signals. Carrier power should be increased to correctly demodulate the signal without reaching the injection level. Figure 3.41 demonstrates the demodulated amplitude for different modulating frequencies f_m, carrier frequency and power were held constant. Up to 300 kHz, the peak-to-peak output voltage increases linearly with the modulating frequency. Beyond this point, it falls down. This limited level is fixed by the envelope detector's bandwidth which was measured to 300 kHz.

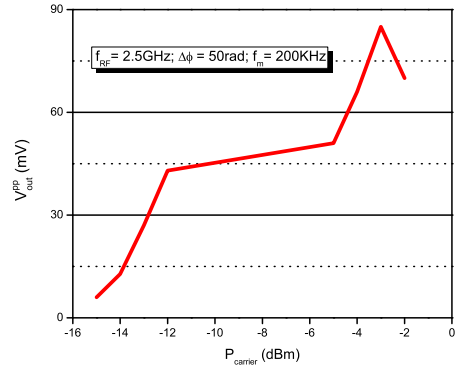
The implemented prototype proposed in this section has demonstrated the feasibility of an ultra-low power compact RFFE by using an original technique to demodulate a RF signal. This helps to considerably reduce the system power consumption in comparison with frequency conversion architectures. The principle of operation of the proposed demodulator was validated with three analog modulation scheme (AM, FM and PM). If we consider the very low power consumption of the MOOD system ($\approx$120 µW for the core), its performances are good. The limited sensitivity is caused by the lack of amplification at RF signal and could be improved by introducing a LNA before the oscillator.



(a) AM

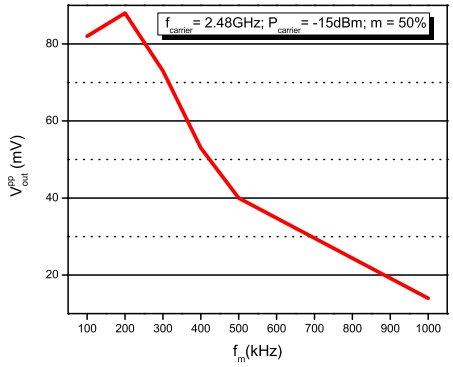


(b) FM

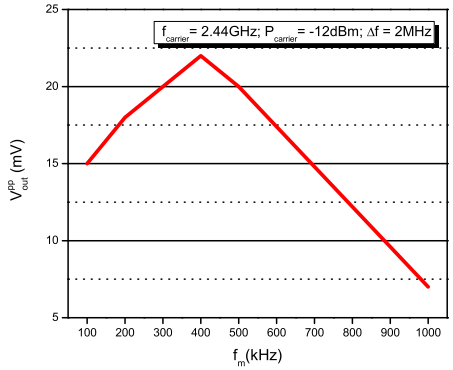


(c) PM

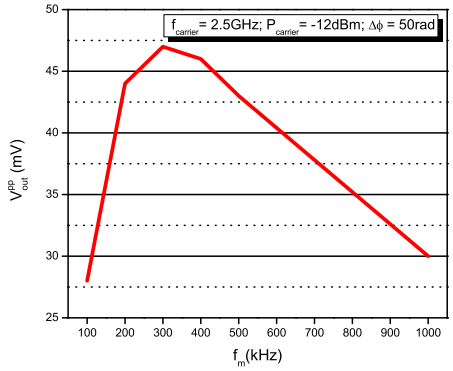
Figure 3.40: Demodulated amplitude versus $P_{carrier}$



(a) AM



(b) FM



(c) PM

Figure 3.41: Demodulated amplitude versus f_m

3.5 Conclusion

In this chapter, an approach at system level was presented and investigated to further reduce the power consumption of radio frequency front-end in wireless sensor networks. First, an overview of the existing solutions in the literature was given. Their advantages and drawbacks were discussed. Then, equipped with this investigation, a Modulated Oscillator for envelOpe Detection (MOOD) architecture was proposed. It is based on a pulled oscillator that converts a frequency modulated signal to an amplitude modulated one. The baseband conversion is performed by the envelope detector. In order to demonstrate the feasibility of this system, a prototype was designed and carried out in 65 nm CMOS technology. A standalone oscillator and envelope detector were included in the test prototype for characterization purposes. The measurement results illustrate the feasibility of an ultra-low power LC oscillator with power consumption of 120 µW. MOOD system was tested under different conditions to investigate its limits. Locking the oscillator helps to achieve a maximum of peak-to-peak output voltage when an AM signal is used. However, the oscillator must stay far from the locking range in case of FM or PM for proper demodulation. The sensitivity of the demodulator is mainly limited by the noise figure of the system, since no low noise amplification is performed. In AM case, the sensitivity is estimated to less than −30 dBm.

Chapter 4

Conclusions

4.1 Performance Summary

This thesis investigates the design of ultra low power radio frequency circuits for wireless sensor networks. Such networks require a low power consumption, a low cost and a high level of integration. Accordingly, the implementation of a wireless sensor node needs a careful choice at different design steps: protocol, system, circuit and transistor levels. This thesis focuses on lowering power dissipation of the radio communication since it is the most power hungry part of a sensor node. Moreover, it is also the most promising module to address system challenges.

This research work includes both circuit and system level approaches. First is exploited the subthreshold operation of MOS device. This technique enables the design of very low power circuits using low supply voltages. In the building block approach, the figure of merit $g_m f_T / I_D$ is explored to bias the transistor in moderate inversion region where current efficiency and RF performances can be achieved at the same time. Forward body bias is used to further reduce supply voltages of the circuits. Three circuits are designed using the proposed techniques: a current switching mixer, a self-oscillating mixer and a LC tank oscillator. A single balanced topology

is selected to implement the mixer since it introduces less noise than a double balanced configuration and do not require a balun to perform the connection with the LNA. The circuit exploits bleeding and current-reuse technique to further improve the performances. The transistor of transconductor stage is biased in moderate inversion region and it has been demonstrated that this operating mode maximizes the mixer's figure of merit in comparison with the ones biased in strong inversion region. A voltage conversion gain and single side band noise figure of 18.7 dB and 11.5 dB respectively are achieved for a power dissipation of 330 µW from a 0.8 V supply. Concerning the self-oscillating mixer, a cross-coupled LC oscillator is stacked on the top of a single ended mixer to share the same bias current, and therefore, to lower the power consuption. The SOM consumes 600 µA from a 1 V supply voltage and performs a voltage conversion gain and a single side band noise figure of 10 dB and 17.5 dB respectively. Finally, a LC voltage controlled oscillator is designed and tested. The cross-coupled pair operates at the limit between weak and moderate inversion region to optimize the current efficiency for minimal bias current. The tail transistor operates in moderate inversion region to achieve at the same time a high current efficiency and maximum gain at RF for a fixed bias current, as it will be used later in the proposed system to inject RF signals. These efforts lead to a minimum power consumption of 100 µW from a 0.5 V supply. At nominal bias, the circuit achieves an output power of −24 dBm and a phase noise of −100 dBc/Hz at 1 MHz offset.

Regarding the system approach, an original idea is patented with ST Microelectronics, namely Modulated Oscillator for envelOpe Detector (MOOD). It consists in the use of a pulled LC oscillator to convert a frequency or phase modulated signal into an amplitude modulated one and then perform the conversion to baseband with an envelope detector.

It has been shown that putting the oscillator under pulling condition helps to demodulate angle modulations. When the oscillator is locked to the injected signal, FM or PM demodulation does not occur. However, this condition is advantageous for amplitude modulation since a maximum of gain, introduced by the oscillator, can be achieved. Using the ultra-low power oscillator designed in the circuit approach, the core of the system has a power consumption of roughly 120 µW. A sensitivity less than −30 dBm could be achieved when an AM signal is applied.

4.2 Future Work

The main goal of this research activity is the realization of an ultra low power RF receiver for wireless sensor networks with active power consumption less than 1 mW. To achieve this goal, design methodologies and techniques for low power RF circuits are required. The techniques described and applied in this work are one step towards the realization of a very low power receiver. They have resulted in the development of a system solution that consumes roughly 700 µW for the MOOD based receiver.

It is important to note that the overall gain of the proposed system is supported by the baseband amplifier which consumes more than 50 % of the total power consumption. This amplifier is added for measurement purposes. A future development would consider the introduction of a low noise amplifier to improve the sensitivity of the system. At the high end, an operational amplifier is needed to provide an adequate amplification to the baseband signal. Depending on the input signal level, the LNA gain must be variable to allow the oscillator to work either under pulling condition in case of constant envelope modulation or under locking condition when a variable envelope modulation is applied.

Future development in RF-MEMS may provide exciting alternatives to

exciting on-chip passive components. In the proposed LC oscillator, the low quality of the integrated inductors sets the lower bound on power consumption of the oscillator core. The use of MEMS resonator structures in transceiver circuits is an area for future exploration, as these components may help to reduce the power consumption by eliminating the dependence on low Q passives. Another advantageous aspect is to shift the selectivity burden to the RF-MEMS filter and relax the constraints on the oscillator.

Bibliography

[1] T. Song, H.-S. Oh, E. Yoon, and S. Hong, "A low-power 2.4-GHz current-reused receiver front-end and frequency source for wireless sensor network," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1012 –1022, May 2007.

[2] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2757 –2766, Dec. 2006.

[3] W. Kluge, F. Poegel, H. Roller, M. Lange, T. Ferchland, L. Dathe, and D. Eggert, "A fully integrated 2.4GHz IEEE 802.15.4 compliant transceiver for ZigBee applications," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, Feb. 2006, pp. 1470 –1479.

[4] S. Ho and C. Saavedra, "A low-noise self-oscillating mixer using a balanced VCO load," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1705 –1712, Aug. 2011.

[5] T.-P. Wang, C.-C. Chang, R.-C. Liu, M.-D. Tsai, K.-J. Sun, Y.-T. Chang, L.-H. Lu, and H. Wang, "A low-power oscillator mixer in 0.18-/spl mu/m CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 88 –95, Jan. 2006.

[6] H. Yan, J. Macias-Montero, A. Akhnoukh, L. de Vreede, J. Long,

J. Pekarik, and J. Burghartz, "A 120 #x00b5;w fully-integrated BPSK receiver in 90nm CMOS," in *2010 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2010, pp. 277 –280.

[7] "S. roundy, energy scavenging for wireless sensor nodes with a focus on vibration to electricity conversion. PhD thesis," Ph.D. dissertation, University of California, Berkeley, May 2003.

[8] *Wireless Technologies - CRC Press Book*. [Online]. Available: http://www.crcpress.com/product/isbn/9780849379963

[9] "IEEE standard 802.15.4, Low–Rate wireless personal area network, october 2003."

[10] T.-K. Nguyen, V. Krizhanovskii, J. Lee, S.-K. Han, S.-G. Lee, N.-S. Kim, and C.-S. Pyo, "A low-power RF direct-conversion Receiver/Transmitter for 2.4-GHz-Band IEEE 802.15.4 standard in 0.18- CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4062 –4071, Dec. 2006.

[11] D. Steingart, S. Roundy, P. K. Wright, and J. W. Evans, "Micropower materials development for wireless sensor networks," *MRS bulletin*, vol. 33, no. 4, pp. 408–409. [Online]. Available: http://cat.inist.fr/?aModele=afficheN&cpsidt=20354692

[12] D. Steingart, C. Ho, J. Salminen, J. Evans, and P. Wright, "Dispenser printing of solid polymer-ionic liquid electrolytes for lithium ion cells," in *6th International Conference on Polymers and Adhesives in Microelectronics and Photonics, 2007. Polytronic 2007*, 2007, pp. 261 –264.

[13] B. Otis and J. M. Rabaey, *Ultra-Low Power Wireless Technologies for Sensor Networks*. Springer, Jan. 2007.

[14] J. Kao, S. Narendra, and A. Chandrakasan, "Subthreshold leakage modeling and reduction techniques [IC CAD tools]," in *IEEE/ACM*

International Conference on Computer Aided Design, 2002. ICCAD 2002, Nov. 2002, pp. 141 – 148.

[15] L. Zhou, J. Kahn, and K. Pister, "Corner-cube retroreflectors based on structure-assisted assembly for free-space optical communication," *Journal of Microelectromechanical Systems*, vol. 12, no. 3, pp. 233 – 242, Jun. 2003.

[16] A.-S. Porret, T. Melly, D. Python, C. Enz, and E. Vittoz, "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: architecture and receiver," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 452 –466, Mar. 2001.

[17] "www.greenpeak.com."

[18] "E.-y. lin, "a comprehensive study of power-efficient rendezvous schemes wireless sensor networks," Ph.D. dissertation, university of california, berkeley, 2005." Ph.D. dissertation.

[19] E. Shih, P. Bahl, and M. J. Sinclair, "Wake on wireless: an event driven energy saving strategy for battery operated devices," in *Proceedings of the 8th annual international conference on Mobile computing and networking*, ser. MobiCom '02. New York, NY, USA: ACM, 2002, pp. 160–171. [Online]. Available: http://doi.acm.org/10.1145/570645.570666

[20] H.-R. Kim, C.-Y. Cha, S.-M. Oh, M.-S. Yang, and S.-G. Lee, "A very low-power quadrature VCO with back-gate coupling," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 6, pp. 952 – 955, Jun. 2004.

[21] A. Shameli and P. Heydari, "Ultra-low power RFIC design using moderately inverted MOSFETs: an analytical/experimental study," in *2006 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, Jun. 2006, p. 4 pp.

[22] A. Liscidini, A. Mazzanti, R. Tonietto, L. Vandi, P. Andreani, and R. Castello, "Single-stage low-power quadrature RF receiver front-

end: The LMV cell," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2832 –2841, Dec. 2006.

[23] "(2003) international technology roadmap for semiconductors, 2003 edition. [online]. available: http://public.itrs.net/." [Online]. Available: http://public.itrs.net/

[24] R. Hegde and N. Shanbhag, "A voltage overscaled low-power digital filter IC," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 388 – 391, Feb. 2004.

[25] T. Manku, G. Beck, and E. Shin, "A low-voltage design technique for RF integrated circuits," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 10, pp. 1408 –1413, Oct. 1998.

[26] H.-H. Hsieh and L.-H. Lu, "Design of ultra-low-voltage RF frontends with complementary current-reused architectures," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 7, pp. 1445 –1458, Jul. 2007.

[27] H. Mostafa, M. Anis, and M. Elmasry, "A novel low area overhead direct adaptive body bias (d-ABB) circuit for die-to-die and within-die variations compensation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 10, pp. 1848 –1860, Oct. 2011.

[28] A. Hokazono, S. Balasubramanian, K. Ishimaru, H. Ishiuchi, T.-J. K. Liu, and C. Hu, "MOSFET design for forward body biasing scheme," *IEEE Electron Device Letters*, vol. 27, no. 5, pp. 387 – 389, May 2006.

[29] C. Enz and Y. Cheng, "MOS transistor modeling for RF IC design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 186 –201, Feb. 2000.

[30] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, Dec. 2003.

[31] H. Darabi and A. Abidi, "Noise in RF-CMOS mixers: a simple physical model," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 1, pp. 15 –25, Jan. 2000.

[32] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 4, pp. 365 –373, Dec. 1968.

[33] B. Razavi, *RF Microelectronics*, 1st ed. Prentice Hall, Nov. 1997.

[34] M. Terrovitis and R. Meyer, "Noise in current-commutating CMOS mixers," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 772 –783, Jun. 1999.

[35] S.-G. Lee and J.-K. Choi, "Current-reuse bleeding mixer," *Electronics Letters*, vol. 36, no. 8, pp. 696 –697, Apr. 2000.

[36] H. Lee and S. Mohammadi, "A 500 mu;W 2.4GHz CMOS subthreshold mixer for ultra low power applications," in *2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, Jun. 2007, pp. 325 –328.

[37] C. Hermann, M. Tiebout, and H. Klar, "A 0.6-v 1.6-mW transformer-based 2.5-GHz downconversion mixer with +5.4-dB gain and -2.8-dBm IIP3 in 0.13- mu;m CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 488 –495, Feb. 2005.

[38] V. Vidojkovic, J. van der Tang, A. Leeuwenburgh, and A. van Roermund, "A low-voltage folded-switching mixer in 0.18- mu;m CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1259 – 1264, Jun. 2005.

[39] A. Do, C. Boon, M. A. Do, K. S. Yeo, and A. Cabuk, "A weak-inversion low-power active mixer for 2.4 GHz ISM band applications,"

IEEE Microwave and Wireless Components Letters, vol. 19, no. 11, pp. 719 –721, Nov. 2009.

[40] C.-H. Wu and H.-T. Chou, "A 2.4GHz variable conversion gain mixer with body bias control techniques for low voltage low power applications," in *Microwave Conference, 2009. APMC 2009. Asia Pacific*, Dec. 2009, pp. 1561 –1564.

[41] H. Sjoland, A. Karimi-Sanjaani, and A. Abidi, "A merged CMOS LNA and mixer for a WCDMA receiver," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 1045 – 1050, Jun. 2003.

[42] A. Mazzanti, "Analysis and design of injection locked CMOS oscillators for radio frequency quadrature generation," Ph.D. dissertation, Universitá degli Studi di Modena e Reggio Emilia, Italia, 2005.

[43] D. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 329 – 330, Feb. 1966.

[44] J. Rael and A. Abidi, "Physical processes of phase noise in differential LC oscillators," in *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000*, 2000, pp. 569 –572.

[45] T. Taris, J. Begueret, and Y. Deval, "A 60 #x00b5;w LNA for 2.4 GHz wireless sensors network applications," in *2011 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2011, pp. 1 –4.

[46] J.-P. Curty, N. Joehl, C. Dehollain, and M. Declercq, "Remotely powered addressable UHF RFID integrated system," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2193 – 2202, Nov. 2005.

[47] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. Pister, "An ultra-low power 2.4GHz RF transceiver for wireless sensor networks in 0.13/spl mu/m CMOS with 400mV supply and an integrated passive RX front-end," in *Solid-State Circuits Conference, 2006. ISSCC 2006.*

Digest of Technical Papers. IEEE International, Feb. 2006, pp. 1460 –1469.

[48] B. Otis, Y. Chee, R. Lu, N. Pletcher, and J. Rabaey, "An ultra-low power MEMS-based two-channel transceiver for wireless sensor networks," in *2004 Symposium on VLSI Circuits, 2004. Digest of Technical Papers*, Jun. 2004, pp. 20 – 23.

[49] N. Pletcher, S. Gambini, and J. Rabaey, "A 2GHz 52 #x003bc;w wake-up receiver with -72dBm sensitivity using uncertain-IF architecture," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, Feb. 2008, pp. 524 –633.

[50] B. Otis, Y. Chee, and J. Rabaey, "A 400 mu;W-RX, 1.6mW-TX super-regenerative transceiver for wireless sensor networks," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, Feb. 2005, pp. 396 –606 Vol. 1.

[51] N. Pletcher, S. Gambini, and J. Rabaey, "A 65 #x003bc;w, 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes," in *IEEE Custom Integrated Circuits Conference, 2007. CICC '07*, Sep. 2007, pp. 539 –542.

[52] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1415 – 1424, Sep. 2004.

[53] R. Adler, "A study of locking phenomena in oscillators," *Proceedings of the IEEE*, vol. 61, no. 10, pp. 1380 – 1385, Oct. 1973.

[54] K. Kurokawa, "Injection locking of microwave solid-state oscillators," *Proceedings of the IEEE*, vol. 61, no. 10, pp. 1386 – 1410, Oct. 1973.

[55] L. Paciorek, "Injection locking of oscillators," *Proceedings of the IEEE*, vol. 53, no. 11, pp. 1723 – 1727, Nov. 1965.

[56] M. Armand, "On the output spectrum of unlocked driven oscillators," *Proceedings of the IEEE*, vol. 57, no. 5, pp. 798 – 799, May 1969.

[57] A. Hajimiri and T. Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 717 –724, May 1999.

[58] N. M. Pletcher, "Ultra-low power wake-up receivers for wireless sensor networks," Ph.D. dissertation, UNIVERSITY OF CALIFORNIA, BERKELEY, 2008.

[59] R. Meyer, "Low-power monolithic RF peak detector analysis," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 1, pp. 65 –67, Jan. 1995.

[60] P. R. Gray, *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Jan. 2009.

[61] H. Stover, "Theoretical explanation for the output spectra of unlocked driven oscillators," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 310 – 311, Feb. 1966.