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Adhesion and leakage current characteristics of selective CVD tungsten films on the silicon substrate

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ABSTRACT - In this study we investigated the effects of SF_6 and CF_4 plasma pretreatments on the adhesion and junction leakage characteristics of the selective CVD W films by SiH_4 reduction of WF_6 on the Si substrate. The SF_6 plasma pretreatment performed in situ prior to W deposition to remove the polymer films in contact holes results in enhancement of the adhesion of W films to the Si substrate but degradation of junction leakages due to vertical and lateral Si consumptions. The CF_4 plasma pretreatment performed as the last step of the reactive ion etching for contact window opening produced the W/Si contacts of good adhesion, low contact resistances and low junction leakages for thin W films, while it produced the W/Si contacts of poor adhesion and high contact resistances for thick W films. The selective CVD W films deposited by the three step process of SiH_4 reduction / in situ annealing / SiH_4 reduction was found to have both good adhesion and low junction leakage characteristics.

1) INTRODUCTION

Selective CVD W is an attractive technology for filling contact holes and via holes with high aspect ratio in very large scale integrated circuits. The reduction of tungsten hexafluoride (WF_6) by silane (SiH_4)[1-3] is generally preferred to the reduction of WF_6 by hydrogen[4] in the selective W process, since the former provides higher deposition rate and produces W films without the problems of encroachment and tunneling[5, 6] which lead to junction leakages. However, the silane reduced W films also have several drawbacks such as less good step coverage and imperfect adhesion. Lifting or peeling of W films which sometimes occurs in contact holes is one of the major obstacles in developing the silane reduced selective CVD W technology. Besides them the silane reduced W films have the problem of junction leakages which are not low enough to accept for mass production, although the leakages are much lower than those of the hydrogen reduced W films.
The SF_6 or CF_4 plasma pretreatment[7, 8] is commonly performed prior to the selective W film deposition to remove the surface area of the Si substrate damaged by the ion implantation for n^+ diffusions[9] and the polymer film produced during the dry etching for contact hole opening which result in high contact resistances. However, the excessive Si etching due to the high etch rate of SF_6 etching is likely to cause vertical and lateral Si consumptions which lead to junction leakages. The purpose of this paper is to investigate the effects of the SF_6 and CF_4 plasma pretreatments on the adhesion and junction leakage characteristics of the silane reduced selective CVD W films.

2) EXPERIMENTAL

The active regions were defined on p-type (100) Si wafers by standard local oxidation of Si (LOCOS) process. The n^+/p junctions were formed by As ion implantation with an energy of 40 KeV at a dosage of 5×10^{15} atoms/cm^2 followed by annealing at 900℃ for 60 min. The junction depths for the n^+ diffusions were about 0.25 μm. After the deposition of the 900 nm borophosphosilicate glass (BPSG) layer contact holes were patterned and etched using the reactive ion etching (RIE) technique. Wafers were then precleaned by immersion in H_2SO_4 - H_2O_2 and 100:1 HF solutions followed by a 10 min rinse in H_2O and spin drying. Prior to the W film deposition the Si surface was etched by the CF_4 plasma etching as the last step of the RIE for contact hole opening or the SF_6 plasma etching in the W deposition chamber to remove the polymer residues at the bottom of contact holes. This in situ plasma pretreatment is often called a Si polishing procedure in the industry.

W films were subsequently deposited selectively in the contact holes on the n^+/p diodes using silane reduction in a commercial single wafer cold wall LPCVD reactor. The reaction chamber was pumped with a turbomolecular pump and the working base pressure of the mid 10^{-7} torr was maintained during the deposition. Wafers were heated from the front side of the wafers using the IR lamp. The process parameters were : substrate temperature = 300℃, pressure = 100 mtorr, SiH_4 flow = 10 cc/min, WF_6 flow = 20 cc/min, H_2 flow = 1,000 cc/min. After the W deposition the Al-1%Si film 600 nm thick was sputter-deposited followed by annealing at 450℃ for 30 min in the mixture of H_2 and N_2.

W/Si contact resistances were measured using the test structure shown in Fig. 1(a). The test pattern consists of 360 contact holes. Junction leakages of the n^+/p diodes were measured at 5 V reverse bias using the test struture shown in Fig. 1(b). To evaluate the effects of the lateral distance from a contact window edge to an adjacent field oxide edge (ΔL) on the adhesion and junction leakages of the selective CVD W films, test patterns with various Δ L's (0.1, 0.19, 0.28 and 0.36 μm) were used.

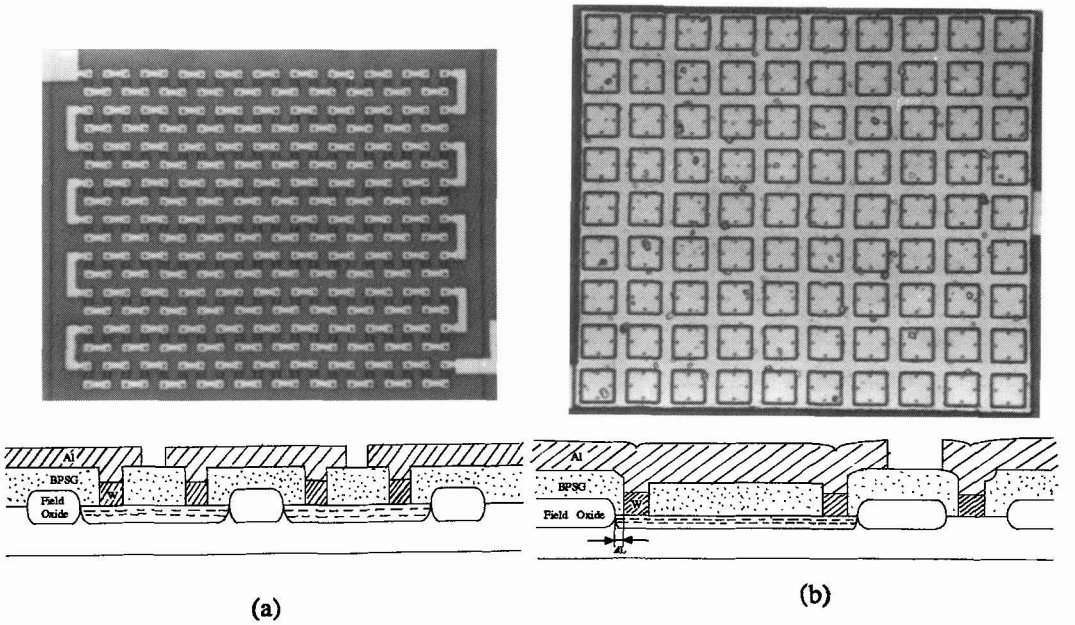


Fig. 1. The test structure used to measure W/n^+ contact resistances : (a) surface SEM micrograph and schematic corss-sectional view and (b) The test structure used to measure $W/n^+/p$ junction leakage currents : surface SEM micrograph and schematic corss-sectional view

3) RESULTS AND DISCUSSION

Figs. 2(a) and 2(b) show the cross-sectional SEM micrograph of a contact hole and the surface SEM micrograph of a scribe line filled with W deposited using silane reduction at 300℃ for 120 sec. Prior to W deposition wafers were precleaned using a dilute HF dip to remove native oxides but were not given the plasma pretreatment. We can see that W films are lifted partially from the Si substrate in the contact hole (Fig. 2(a)) and peeled off in the scribe line (Fig. 2(b)). The dark area at the bottom of the contact hole (Fig. 2(a)) is the void formed by W lifting and the bright area on the right side of the scribe line (Fig. 2(b)) is the place where W films are peeled off and gone. There was no lifting of as-deposited W films from the Si substrate either in the contact hole or in the scribe line. However, the W films in some contact holes and scribe lines were peeled off during the annealing process at 450℃ for 30 min in the mixture of H_2 and N_2 after Al deposition. The contact resistances at the contact holes where W films were lifted or peeled off were very high (> 1 KΩ).

To remove the polymer film produced during the reactive ion etching for contact hole opening the SF_6 plasma pretreatment was performed in situ in the W deposition chamber prior to W deposition. The optimized SF_6 plasma etching conditions were : rf power = 20 watt, total pressure = 50 mtorr, SF_6 flow = 30 cc/min, time = 15 sec. W films 500 nm thick were then deposited at 300℃. The contact resistances and the junction leakage currents for the selective CVD W film deposited by SiH_4 reduction on the n^+/p diodes with the in situ SF_6 plasma pretreatment are shown in Figs. 3(a) and 3(b), respectively. The contact resistances were measured for the W/n^+ contacts while the leakage currents were for the n^+/p junctions. The W films in the contact holes were not lifted, although the contact resistances (Fig. 3(a)) are about 100 ohm higher than those for the Al/n^+ contacts with no W used as standards (Fig. 4(a)). However, the junction leakages for the W/n^+ contacts with the SF_6 plasma pretreatment (Fig. 3(b)) are considerably higher than those for the Al/n^+ contacts (Fig. 4(b)) and thus too

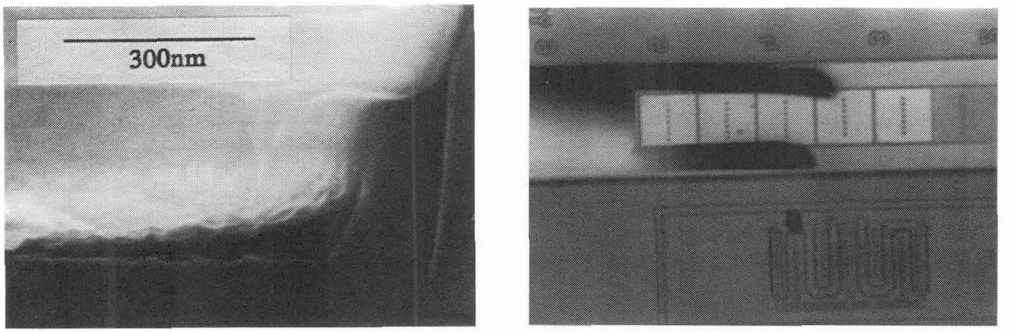


Fig. 2. SEM micrographs showing lifting of the selective CVD W films (a) in a contact hole (cross-sectional view) and (b) at a scribe line (plan view)

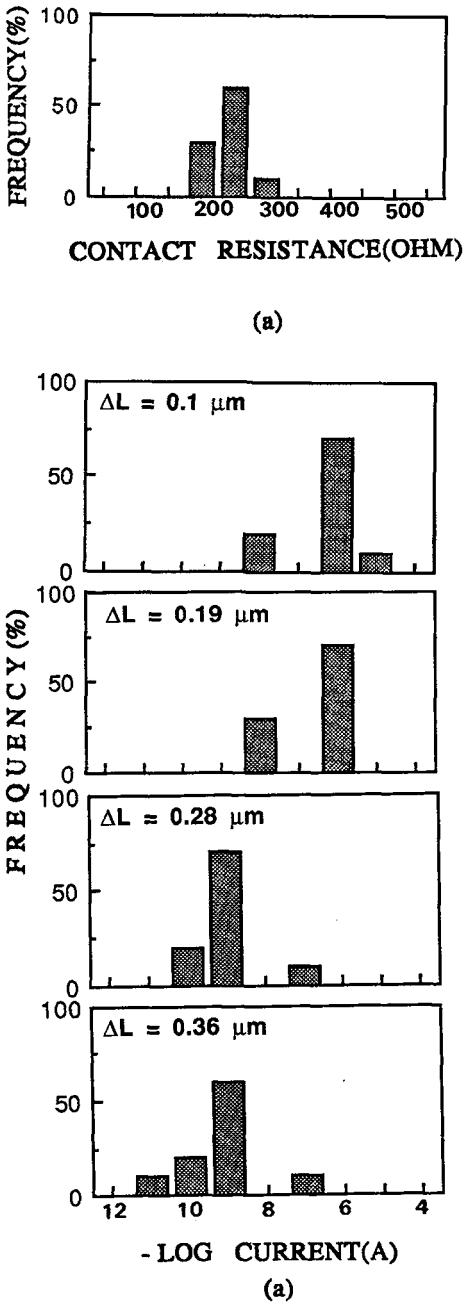


Fig. 3. Histograms showing (a) the contact resistance distribution and (b) the junction leakage distribution at 5V reverse bias for the SiH_4 reduced selective CVD W films with SF_6 plasma pretreatment.

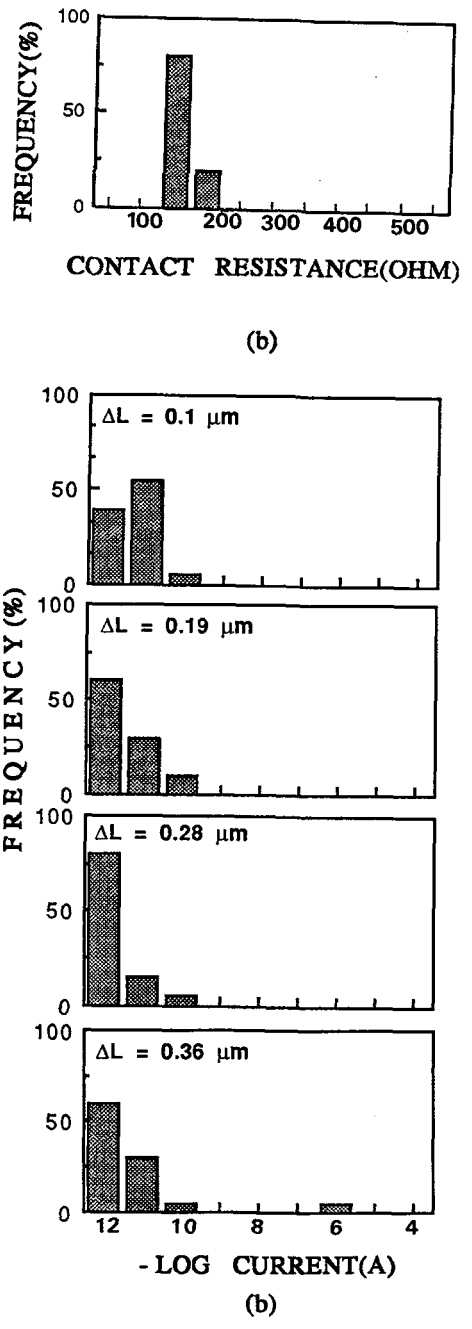


Fig. 4. Histograms showing (a) the contact resistance distribution and (b) the junction leakage distribution at 5V reverse bias for the Al/n^+ contacts used as standards

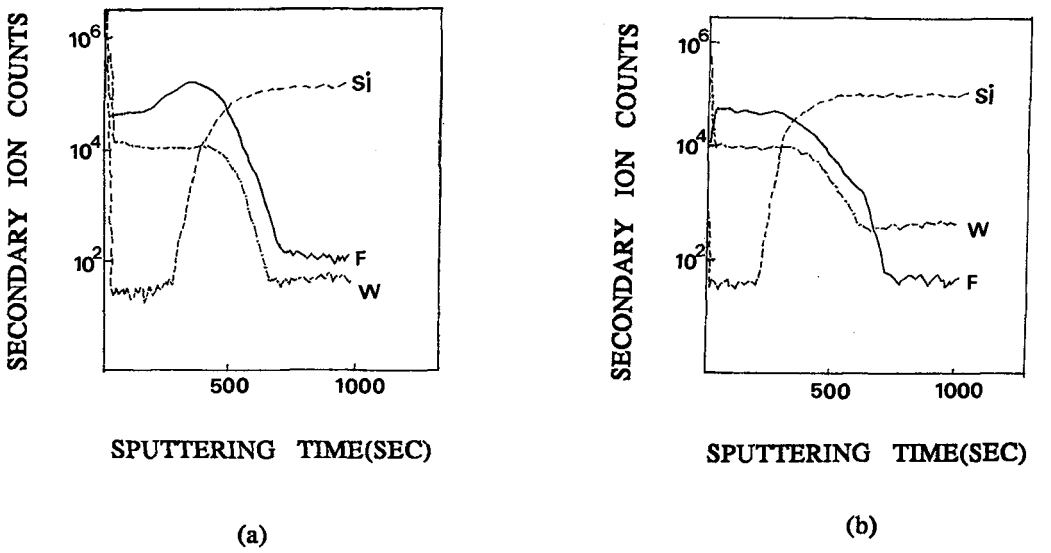


Fig. 5. SIMS depth profiles of the selective CVD W film on the Si substrate (a) with and (b) without SF_6 plasma pretreatment

high to accept. Also junction leakages tend to increase with decreasing ΔL. This implies that junction leakages are mainly caused by the lateral Si consumptions under the Si - SiO_2 interface as well as the vertical Si consumptions. The high etch rate of the SF_6 plasma etching readily consumes up the Si in shallow junctions and in turn causes junction leakages and high contact resistances. We made every effort to lower the SF_6 plasma etch rate further by changing the etching process parameters but failed to because of the hardware limitations of the W deposition system. The lateral Si consumptions seem to be caused by the incorporation of the F species from SF_6 plasma into the Si substrate along the Si - SiO_2 interface. We can see F piled up at the W-Si interface after the SF_6 plasma etching from the comparison of the SIMS depth profiles of the selective CVD W films with (Fig. 5(a)) and without (Fig. 5(b)) the SF_6 plasma pretreatment.

Si etching with CF_4 plasma is also commonly performed instead of the in situ SF_6 plasma pretreatment to remove the polymer films in contact holes prior to the W deposition. The CF_4 plasma etching is known to have the advantages of a lower Si etch rate and a higher degree of anisotropy over the SF_6 plasma etching. The CF_4 plasma etching was conducted slowly at a very low rf power as the last step of the reactive ion etching for contact window opening. The CF_4 plasma etching conditions were : rf power = 50 watt, total pressure = 150 mtorr, CF_4 flow = 45 cc/min, time = 20 sec. The junction leakages for the W/n^+ contact with the CF_4 plasma pretreatment was as low as those for the Al/n^+ contact with no W. The contact resistances for the silane reduced CVD W films 150 nm and 500 nm thick with CF_4 plasma pretreatment are shown in Figs. 6(a) and 6(b) respectively. The mean contact resistance of the W/n^+ contacts with the CF_4 plasma pretreatment for the W film 150 nm thick (Fig. 6(a)) is 100 ohm which is almost the same as that for the Al/n^+ contacts with no W. In

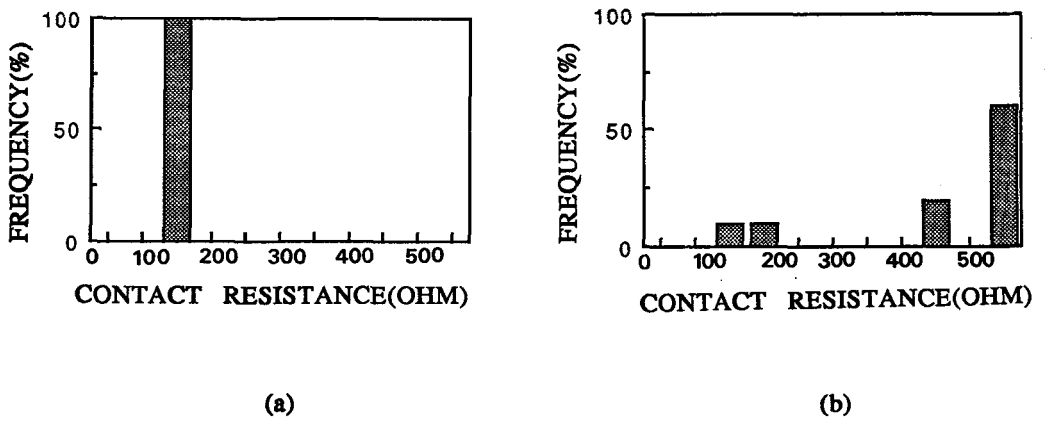


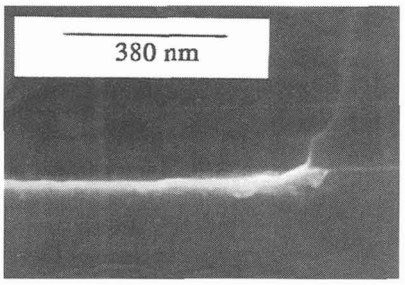
Fig. 6. Histograms showing the contact resistance distribution for the SiH_4 reduced selective CVD W films (a) 150 nm and (b) 500 nm thick with CF_4 plasma pretreatment

contrast the contact resistances of the W/n^+ contacts with the CF_4 plasma pretreatment for the W film 500 nm thick (Fig.6(b)) is widely distributed in the range from a few hundred to a few thousand ohm. This implies that the W films in some of the 360 contact holes of the contact resistance test pattern were lifted when the W film was thick (500 nm). Ohba et al.[10] reported that the stress of the W film deposited by IR heating from the wafer front is tensile for the W film thickness < 200 nm and that the stress changes to compressive with increasing the W film thickness. The compressive stress of the W film 500 nm thick reaches about 8×10^9 dyne/cm^2 and the lifting of the W film 500 nm thick may be due to this high compressive stress.

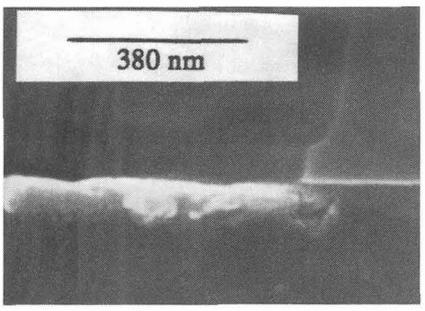
As we can see from the above discussion neither the SF_6 nor the CF_4 plasma pretreatment guarantees the selective CVD W films with good adhesion and low contact resistance as well as low junction leakages when the W films are as thick as 500 nm. Hence we decided to try two step and three step deposition processes to prevent W lifting and to improve the electrical properties of the selective CVD W.

First, we tried a two step W deposition process : hydrogen reduction process of 280℃ for 30 sec for good adhesion followed by silane reduction process at 300 ℃ for low leakages. The two step process was successful in preventing W lifting, but produced contacts with extremely high junction leakages (a few nA - a few μ A). The junction leakages may be caused by the lateral encroachment of W under the $Si\text{-}SiO_2$ interface as shown in Figs. 7(a) and 7(b). The bright lateral lines along the Si-BPSG interface in Figs. 7(a) and 7(b) indicate the W encroachment. We can see that the bright line for the deposition time of 60 sec is thicker than that for 30 sec, which implies that the encroachment increases with increasing the deposition time.

Next, to improve the adhesion and junction leakage characteristics of the selective CVD W we tried a three step process : the first step of the silane reduction at 300℃ for 40 sec, the second step of the in situ annnaling at 450℃ for 120 sec in H_2, and the third step of silane reduction at 300℃. Figs. 8(a) and 8(b) show the contact resistance and junction leakage distributions for the W film 500 nm thick deposited by the three step deposition process,

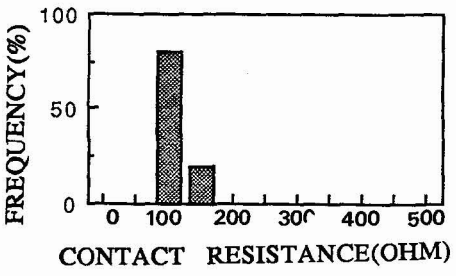


(a)

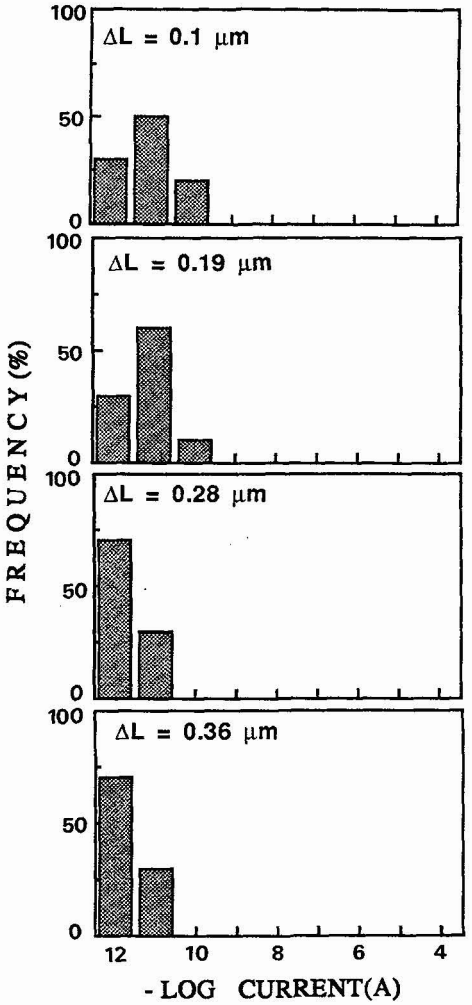


(b)

Fig. 7. Cross-sectional SEM micrographs showing lateral encroachment of W under the Si-SiO_2 interface for the H_2 reduced selective CVD W films deposited at 280℃ (a) for 30 sec and (b) for 60 sec



(a)



(b)

Fig. 8. Histograms showing (a) the contact resistance distribution and (b) the junction leakage distribution at 5V reverse bias for the SiH_4 reduced selective CVD W films 500 nm thick deposited by the two step process : SiH_4 reduction (300℃, 40 sec) / in situ annealing (4500℃, 120 sec) / SiH_4 reduction (300℃, 100 sec)

the Al/n^+ contact and no lifting was observed for the W film thickness of 500 nm. The in situ annealing process seems to enhance the adhesion of W flims to the Si substrate by effectively lowering W film stress and inducing interdiffusion of W and Si at the W-Si interface.

4) CONCLUSIONS

The SF_6 plasma pretreatment performed in situ prior to W depositon to remove the polymer films in contact holes has an enhancing effect on the adhesion of W films to the Si substrate but a degrading effect on junction leakages. The CF_4 plasma pretreatment performed as the last step of the dry etching for contact window opening is more desirable than the SF_6 plasma pretreatment in that the CF_4 plasma pretreatment produces the W/Si contacts of good adhesion, low contact resistances and low junction leakages for thin W films, although the CF_4 plasma pretreatment produces the W/Si contacts of poor adhesion and high contact resistances for thick W films. The adhesion and electrical properties of the silane reduced selective CVD W can be improved by the three step process of SiH_4 reduction / in situ annealing / SiH_4 reduction.

ACKNOWLEDGEMENTS

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