Méthode de simulation rapide de capteur d'image CMOS prenant en compte les paramètres d'extensibilité et de variabilité

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ECOLE CENTRALE DE LYON

ECOLE DOCTORALE Electronique, Electrotechnique,

Automatique

Institut des Nanotechnologies de Lyon

Année : 2014 Thèse Numéro : 2014-06

Thèse

Pour obtenir le grade de

DOCTEUR DE L'ECOLE CENTRALE DE LYON

Discipline : Electronique

Présentée et soutenue par

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31 Janvier 2014

Fast Scalable and Variability Aware CMOS Image Sensor Simulation Methodology

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To my families and Electronics world!

Abstract

Along with the semiconductor and integrated circuit industry development, the CAD tools play a more and more important role in the design cycle. The simulation methodology is also explored in different domains. In the design flow of CMOS image sensor, there is optics simulation, CMOS process TCAD simulation, pixel electrical simulation and system simulation. Unfortunately, these simulations have to be performed separately because they belong to different domains in different levels. Specifically, for CMOS image sensor electrical performance prediction, circuit designers need do some extra work to identify the circuit performance due to the gap between circuit low level simulation and system level simulation. This thesis is intended to bridge the circuit level performance and system level performance, from low level to high level while keeping the accuracy. The thesis work is dedicated to solve the time consumption problem and memory consumption problem which is encountered in the sensor matrix classical simulation.

Acknowledgements

I would like to thank my advisor Professor Ian O'Connor for his invaluable guidance, support, and for the encouragement he gave me during this thesis work. I am grateful to Dr. David Navarro for being my associate advisor. I am thankful for all the valuable time he has spent on discussion with me.

Special thanks to my jury: P. Magnan, G. Sicard, D. Houzet, thank you for spending your time on reviewing my thesis.

I would like to thank my sponsor, the China Scholarship Council (CSC), for the financial support of my PhD work. I am also thankful for the research facilities and support provided by the Lyon Institute of Nanotechnology and Ecole Centrale Lyon.

I would like to show my gratitude for my colleagues at INL. I would especially like to thank Felipe Frantz who is always willing to offer any help and share his knowledge. I thank all my former and current officemates Wan Du, Vijay Viswanathan, Nanhao Zhu, Zhen Li, Xuchen Liu. I also thank the engineer Laurent Carrel for his support. I would like to thank Patricia Dufaut, Nicole Durand, Sylvie Goncalves for their administrative support.

I would like to thank my dear girl friend Dan Wu for her understanding, belief and support all these years. I thank her for being patient and supporting me during my thesis life. Thanks to all.

Contents

CHAPTER 1 Introduction

The Solid-state imaging is based on a physical process of converting energy, from a light energy or photon energy into another measurable quantity, from the photons to electrons. The output measurable quantity is usually electric current or voltage. A solid state device, such as a Photodiode, Photogate, etc, can convert the photons into electrons. The quantum efficiency which presented by the ratio of number of the collected electrons to the numbers of incident photons characterizes the conversion efficiency of the solid imaging device. The other conversion efficiency related parameters are listed in Table 1. 1. The photons energy is directly related to the wavelength, it results in the quantum efficiency varying with the wavelength, and it can be represented by a function named spectral response. The sensitivity is an important parameter of pixel, and it is used to characterize how much output quantity could be attained when a unit photon is absorbed at a specific wavelength.

Table 1. 1. The parameters of solid state image sensor

Quantum efficiency	The ratio of the number of collected electron/hole pairs to the number of incident photons at a given light wavelength.
Spectral Response	Quantum efficiency as a function of the wavelength measured within the desired wavelength range.
Sensitivity	The ratio of the pixel output change obtained after photon integration to the amount of light change on a given wavelength
Dark Current	The current generated by the detector in the absence of any incident radiation
Dynamic Range	The ratio of the maximum non-saturating signal to the dark signal measured over the desired image capture time period.
Fixed pattern noise	The variation in pixel currents at uniform illumination, measured at the output the sensor array.
Fill factor	The ratio of sensing area to the pixel square area.

The Solid-state imaging technology has been widely studied, and it has extensive applications ranging from consumer electronics (e.g. security cameras, digital still cameras) and machine vision systems (e.g. robot vision and auto-drive for vehicles).

1.1 Solid state image sensor

The solid-state imaging technique is mainly classified into two categories: Charge Coupled Devices (CCDs) and CMOS image sensor. A CCD image sensor is basically an array of capacitors formed by polycrystalline silicon (POLY) wires over a p-type substrate[1]. The deep depletion region will be formed by holding the ϕ_2 as a positive voltage as referring to Figure 1. 1. The photons passed through the POLY can inject and reach in the depletion region which will generate electron-hole pairs (*EHPs*) according to the photo-electric theory. Some of those electrons, generated in the depletion region or close enough to diffuse into it, will then be separated and swept into the potential well and the stuck there. The simplified cross-section of a pixel in a CCD sensor is shown in Figure 1. 1. The CCDs pixel consists of the area bounded electrode E_1 and E_3 and the column isolators. The surface potential will be increased considerably under the gate if a positive pulse is applied to ϕ_2, this surface potential forms a well which is potentially used to store the electrons.

The generated electrons are needed to be shifted down the column as the photons have been integrated in the well below the electrode E_2. A combined potential well can be formed under E_2 and E_3 by setting the ϕ_3 as positive voltage, thus the generated electrons will be stored in this new well. The electrons will be transferred completely to the well under E_3 when changing ϕ_2 from positive to zero with maintaining the ϕ_3 as positive. In this way, the electrons will be transferred from well to well, from pixel to pixel.

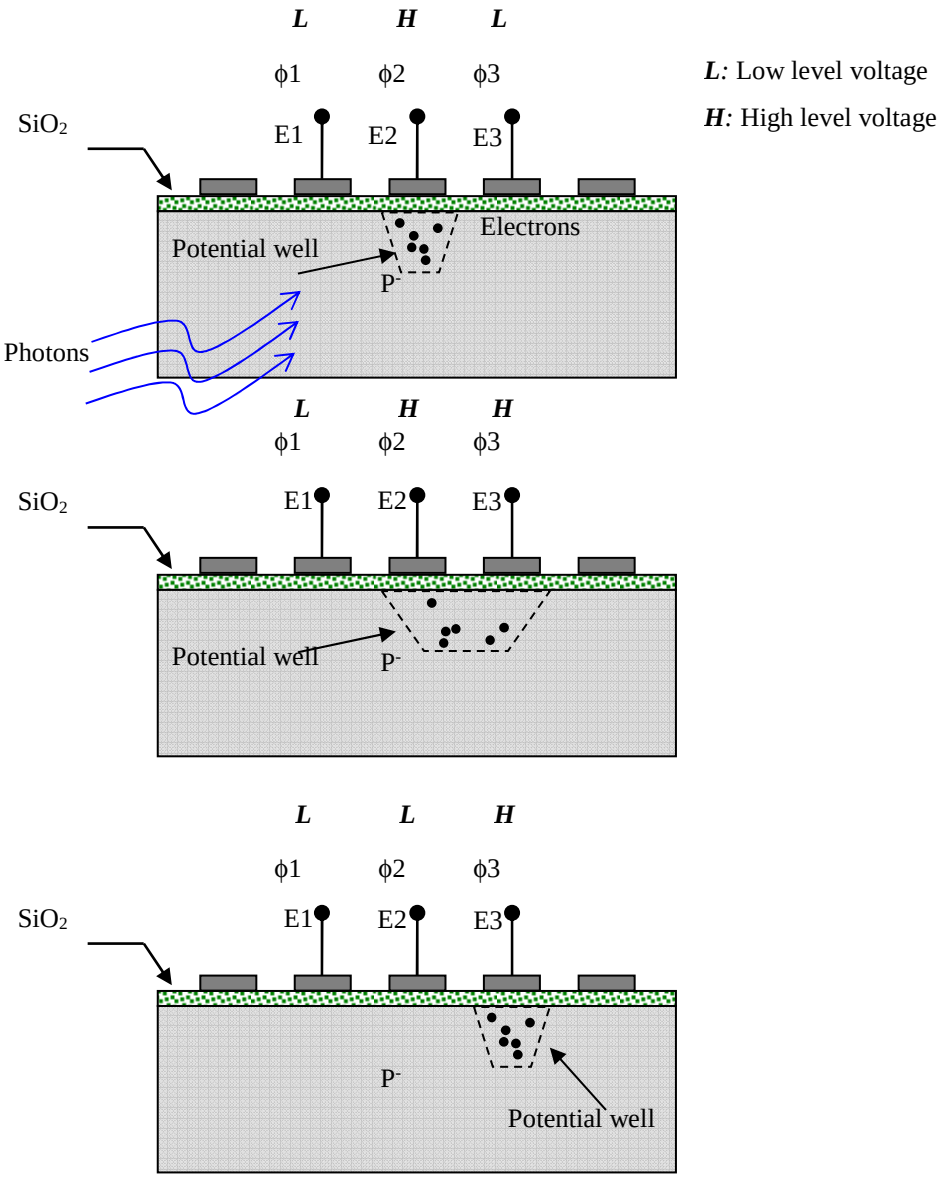


Figure 1. 1. The cross section of simplified CCD sensor [2].

Finally electrons are shifted into an analog register located at the end of the row and be converted into a voltage by the readout amplifier. The charge to voltage or current conversion is done out of the pixel, so the CCDs could achieve a 100% fill factor. Due to the specific fabrication process and long term development, CCDs have a high

imaging quality and it is widely used in the scientific applications and high performance imaging applications.

As the integrated circuit development, more and more functionalities are expected to be integrated together. In VLSI design, people hope to combine the pixel matrix with the signal processing circuit on the same chip. In the last decades, as the CMOS technology have become more matured, a relatively new image sensor technology called active pixel sensor (APS) that uses existing CMOS manufacturing facilities has emerged as a potential replacement of CCD. The principle of converting light into charge is almost the same as CCD in CMOS image sensor, just the read out scheme is different. Electron-hole pairs generated within or close to the depletion region of a reverse biased *pn* diode will be collected, electrons accumulated at the cathode node and holes accumulated at the anode node. These electrons are then read out as either a voltage or as charges via a column bus to the row of readout circuits. Comparing with CCD technology, CMOS APS has several advantages as listed in the Table 1. 2.

Table 1. 2. Advantages of CCD image sensor versus CMOS APS image sensor[3].

CCD	CMOS
Lower noise	Low power consumption
Smaller pixel size	Single power supply
Lower dark current	High integration capability
100% Fill Factor	Lower cost
Higher sensitivity	Single master clock
Electronic shutter without artifacts	Random access

CMOS image sensor is gaining the low end of the imaging market by its superiority in cost, and also in some high end application field. Its revenue increases steadily year by year as indicated in the Figure 1. 2. Benefiting of the possibility of integrating lots of functional circuitry around the pixels in a chip, the camera on chip is on the way of image sensor design in CMOS technology.

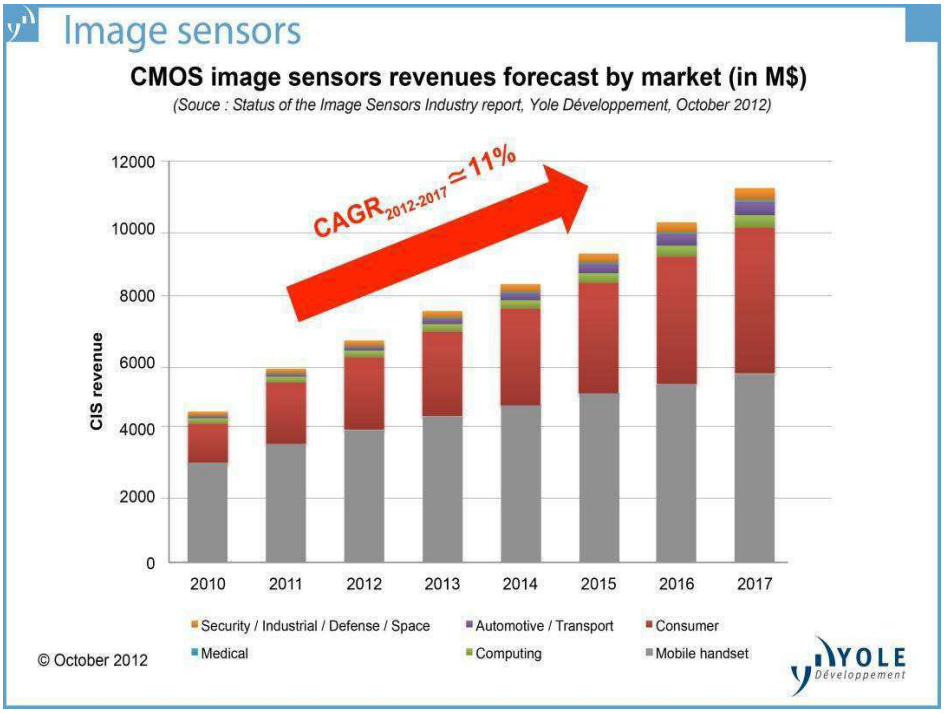


Figure 1. 2. CMOS image sensors market[4].

1.1.1 Evolution of CMOS technology

The first working point contact transistor developed by *J. Bardeen*, *W. Brattain* and *W. Shockley* at Bell laboratories in 1947 initiated the rapid growth of the information technology industry [5]. In 1958, *Rolland R. Roup* and *Jack S. Kilby* invented the first integrated circuit flip flop at Texas [6]. The first CMOS logic gate (NMOS and PMOS) is described by *F. Wanlass* at Fairchild in 1963. In 1963 *G. Moore* predicted that as a result of continuous miniaturization, transistor count would double every 18 months which is known as Moore's law [7]. The speed of transistors increases and their cost decreases as their size is reduced. In 1971, the first introduced microprocessor *Intel 4004* had 2300 transistors with manufacturing technology of 10μm, following the Moore's law during the last decades in 2007 *Quad-Core Intel Xeon* processor had 820M transistors with technology 45nm, the processor frequency has been improved from 108k Hz to 3G Hz. After having crossed 90nm and 65nm technological nodes, 32 nm and 22 nm technology is in the development. CMOS transistors have become smaller and smaller, faster and

faster, lower operative power, and these characteristics meet the requirement of integrating large number of transistors on a chip.

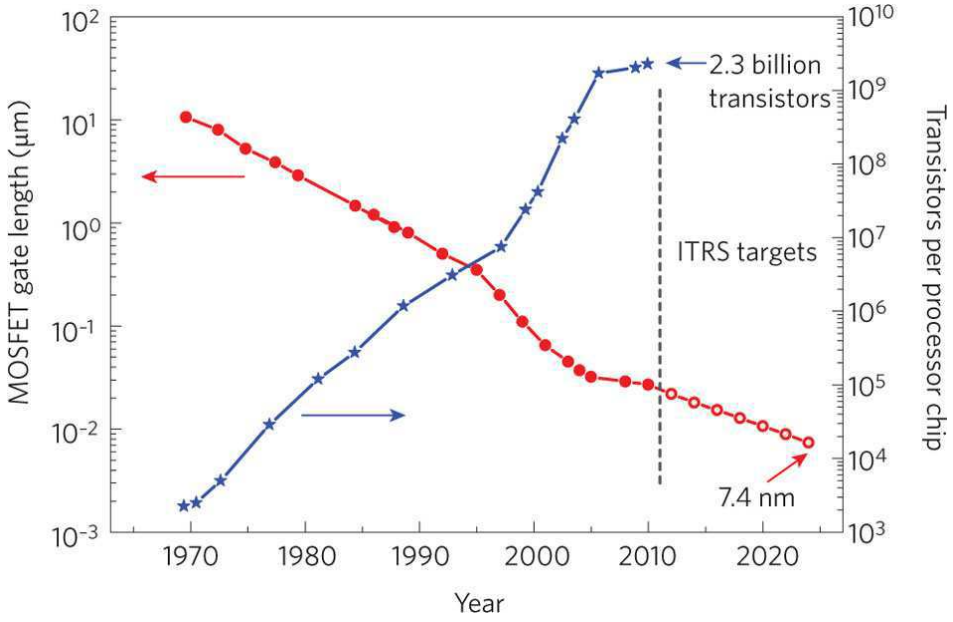


Figure 1. 3. CMOS technology roadmap [8].

The evolution of MOSFET gate length is indicated in Figure 1. 3, the MOSFET gate length shrinks generation after generation as shown in the red points, and International Technology Roadmap for Semiconductors (ITRS) gives a prediction of gate length evolution, the transistor gate length will continue to shrink in the following years, the 7.4nm technological node is expected to be achieved in 2024 as indicated by open red circles [9]. As gate lengths have decreased, the number of transistors per processor chip has increased indicated by blue stars. CMOS technology is widely used in microprocessors, microcontrollers, static RAM, mixed and analog circuits such as amplifier, radio frequency transceivers, image sensors etc. Nowadays, the modern integrated circuit is developing through very large scale integration (VLSI), ultra large scale integration (ULSI), system on chip (SOC), and system in package (SIP). It begins to follow “More than Moore” law according to the report from ITRS as shown in Figure 1. 4.

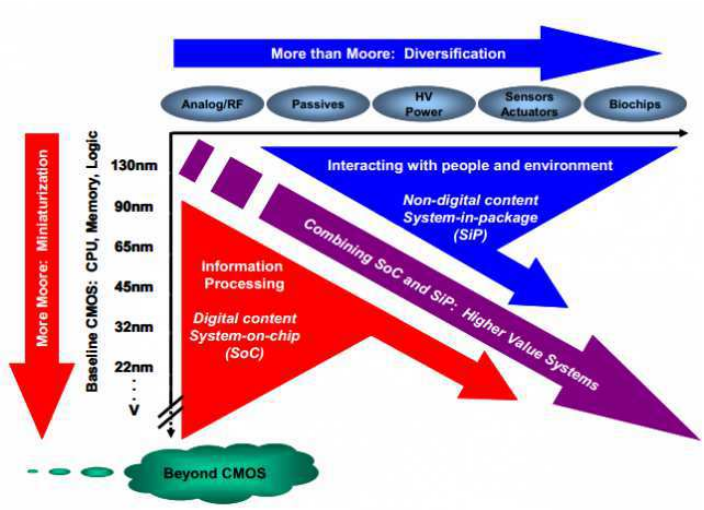


Figure 1. 4. Miniaturization vs. diversification [10]

Due to the CMOS transistor size shrink continuously, it is possible to integrate much more transistors and integrate large functionalities on a single chip. Additionally, the smaller transistor feature size will result in switching faster between on and off state of transistor operation, low power requirement, etc. This smaller size makes CMOS technology suitable for high volume integration, especially for portable device. For example, in recent years, CMOS image sensor is becoming the first choice for its lost cost, highly volume integration possibility and lower power consumption in cell phone application.

1.1.2 Evolution of CMOS imaging

In 1963, a structure which allows determination of a light spot's position using photoconductivity effect [11] was reported by *S. Morrison*. IBM reported a Scanistor in 1964, and this Scanistor used an array of n-p-n junctions addressed through a resistive network to produce an output pulse proportional to the local incident light intensity [12]. Operating p-n junction in a photon flux integrating mode was suggested in 1967, the photocurrent from the junction is integrated on a reverse-biased p-n junction capacitance [13]. The signal charge is converted into a voltage pulse using a series resistor, a PMOS switch was suggested to readout the signal. *P.J. Nobel* described several configurations of

self-scanned silicon image detector arrays [14], both surface photodiodes and buried photodiodes for reducing dark current were reported. *P.J. Nobel* also discussed a charge integration amplifier for readout, similar with the later approaches implemented by the others. The active pixel sensor (APS) with a MOS source follower in pixel was firstly introduced by *P.J. Nobel* in 1968. *S.G. Chamberlain et al.* proposed an improved model of operation of the sensor in 1969 [15]. In 1970, *P.W. Fry et al.* explored the issue of Fixed Pattern Noise (FPN) [16]. The limitations of MOSFET performance results in the CMOS image sensor was sporadically investigated, MOS image sensor were not able to achieve the above performance criteria compared to CCD's [17] in that time. In the late 1970's and early 1980's, the company *Hitachi* and *Matsushita* continued the development of MOS image sensor [18] [19] for camcorder-type applications, including single-chip color imagers. In the early 1990's, as the CMOS technology and fabrication process matured, two main efforts have been devoted by the end user in CMOS image sensor development. Firstly, the NASA's need for highly miniaturized, low power, instrument imaging system for the next generation deep space exploration spacecraft brings the CMOS image sensor new design challenge and development opportunity. Secondly, the low cost demand drives a highly functional single-chip imaging systems in CMOS technology. The convergence of efforts has led to significant advances in CMOS image sensors and the development of the CMOS APS. The performance of CMOS image sensor is almost comparable with CCDs in read noise, dynamic range and responsivity, but an apparent advantage is the increased functionality and lower operative power, this lowers imaging system power requirement [5]. Along with the semiconductor technology revolution, the CMOS technology has gone into deep submicron processes, the imager pixel is becoming smaller and smaller in new technological node. These years, designers have moved their technology process from 0.35μm, 0.25μm and 0.18μm, and then 90nm, 55nm for Back Side Image sensor[20] with pixel pitch size 1.75μm. For meeting the market, much more attention has been focused on the CMOS image sensor's characteristics and performance, intending to design new pixel structure and new functional circuitry for special applications, such as high Fill

Factor for portable device, high frame rate for video camera, high resolution for high-end camera, and so on. After a long period of development, CMOS image sensor is comparable with the CCDs on performance. It seems that the CMOS image sensor will gain much more market due to its advantage in lower cost and become the mainstream of the solid-state imaging device.

1.1.3 CMOS Image Sensor Chip

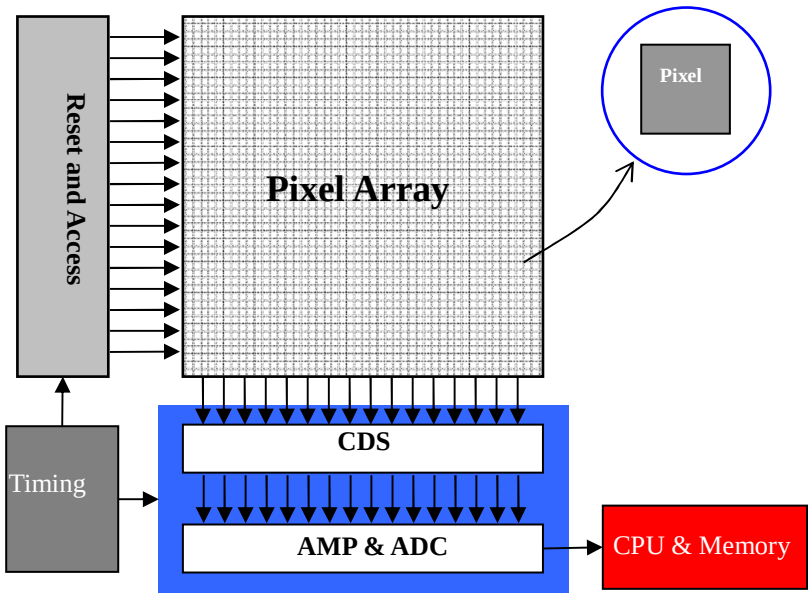


Figure 1. 5. Overall architecture of CMOS image sensor chip

Currently, the camera on chip has become true. The overall architecture of CMOS image sensor is shown in Figure 1. 5 and the functionalities refer to Table 1. 3. The CMOS image sensor chip consists of a matrix of pixels and peripheral functionalities, such as timing block, multiplexer, Analog-to-Digital Converter (ADC). The pixel is in charge of integrating the injected light intensity and converting the light into measurable voltage. After a certain time of exposure, the signal (voltage) in the pixel is readout and processed by CDS (Correlated Double Sampling) circuit, the CDS output voltage will be amplified and finally converted into digital number (DN) by ADC. The image

processor combing with high level algorithm, such as color interpolation, FPN suppression and color correction will process the digital numbers into images.

Table 1. 3. The function of on chip blocks

Module	Function
Timing Generator	The overall control module provides the whole chip with proper time sequence
Reset	Reset the sensing node and clear the residual charges, set the sensing node reverse potential
Access	Enable the sensing node voltage be buffered to the column bus and controls the power consumption when the charge signal is read out (whole matrix)
Pixel Array	Sensing the incident light and generating the charge signal
CDS	Sampling the signal in reset stage and integration end for suppressing the FPN
Multiplexer	Select which column to connect to the column ADC
AMP	Amplify the analog signal to the swing range of ADC
ADC	Convert the pixel output analog signal to the digital signal
Processor	Process the sensor raw data, such as color interpolation, white balance
Memory	Stores the digital data outing of the processor

1.1.3.1 CMOS image sensor pixel structures

There are three predominant approaches to implement pixel in CMOS technology: 1, passive pixel; 2, photodiode-type active pixel, and 3, photogate-type active pixel.

1.1.3.1.1 Passive pixel (PPS)

The first and simplest pixel structure is called passive pixel, the photodiode is connected directly to the column bus through closing the TX gate (RS high voltage) as shown in Figure 1. 6. This structure with the fewest transistors gains the highest ratio of light sensitive area to the total pixel area in a single pixel which is defined as fill factor (FF), this structure achieves the higher quantum efficiency. In spite of the small pixel size capability and a high Fill Factor, they suffer from low sensitivity and high noise due to the large column’s capacitance compared to the pixel’s own [21].

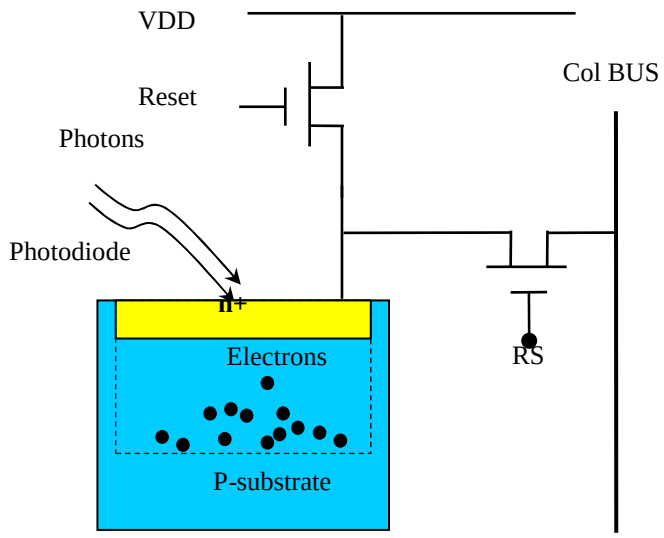


Figure 1. 6. Schematic of passive pixel sensors (PPS)

1.1.3.1.2 Active pixel sensor

The Active Pixel Sensor (APS) is the pixel with an inner amplifier (buffer) implemented by a MOS transistor as shown in Figure 1. 7. There are three CMOS transistors for resetting, amplifying and transferring the electrical signal in pixel, so this pixel structure is commonly called 3T-APS. [63] gives an accurate simulation of 3T-APS pixel architecture and proposed a new model of reset noise, which achieves a better approximation than the normal used the KTC reset noise model, in the new model, the coupling capacitance of source following is taken into account. It improves the pixel performance and minimizes the power dissipation during the signal readout phase. Owing to the extra transistors added, normally, the 3T-APS can get the Fill Factor of 20% to 30%. Additionally, the CMOS process parameter variation causes the transistor threshold voltage difference, which makes conventional 3T-APS suffering from high Fixed Pattern Noise. With the purpose of increasing effectively sensor dynamic, an extra transfer gate and storage node can be added in the basic 3T-APS to from the 4T pinned photodiode APS, it aims at a better pixel performance. This structure is widely used due to its capability of minimizing dark current generated by silicon oxide interface defects

in Photodiode region[22]. As indicated in Figure 1. 8, the sensing node (photodiode) and charge storage node (Floating diffusion) is separated by the transfer gate, this can achieve simultaneously a high conversion gain and full well capacity. These two parameters are normally a pair of conflict in the conventional 3T-APS.

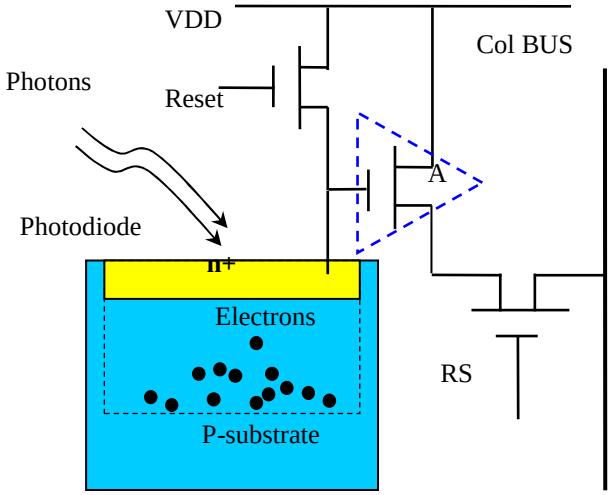


Figure 1. 7. Schematic of 3T active pixel sensor (APS)

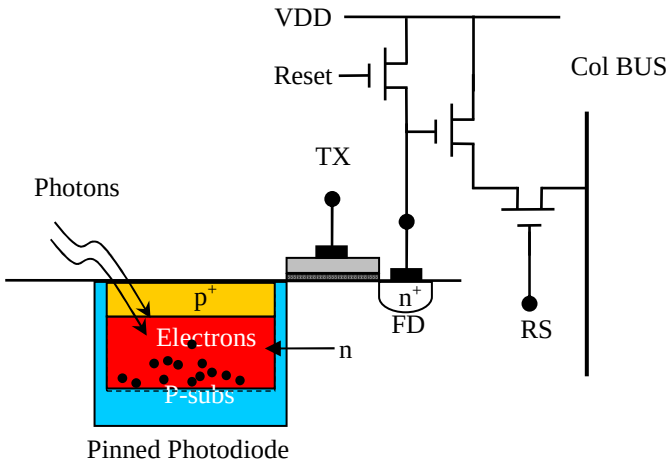


Figure 1. 8. Pinned photodiode 4T-APS structure

By connecting the reset transistor as a forward diode, the logarithmic APS can be formed. In a forward biased diode, the current is proportional logarithmically to the voltage, and the photocurrent following through the photodiode is equal to the diode

current due to theirs serial connection. Hence, the photodiode voltage is not a linear function of its current any more, this operation results in a non-linear sensor output versus injected light intensity (photocurrent). This permits an increase on the intra-scene dynamic range. Logarithmic APS are suitable for High Dynamic Range applications, although they suffer from large FPN. Owing to this fact, currently, they are not as used as before. It must be pointed out that they are used a lot in silicon retinas where the high dynamic range is the primary concerning. A typical schematic is shown in the Figure 1. 9.

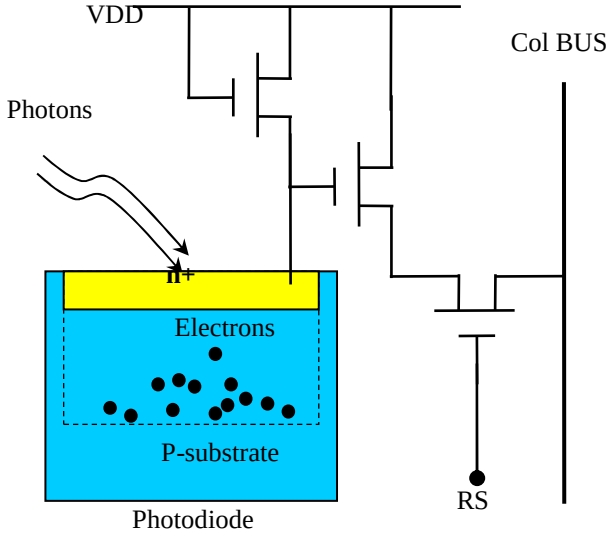


Figure 1. 9. The structure of log PD-APS

1.1.3.1.3 Photogate APS

The photogate APS was introduced later than PD APS, in 1993. It employs the principle of operation of CCDs concerning photons integration. The photogate type APS consists of five transistors including a photogate, transfer gate (TG) and the other three transistors as typical APS, as shown schematically in Figure 1. 10. A depletion region will be formed under the gate when a positive voltage VG is applied to the polysilicon gate. During the integration time (Tint), photons pass through the polysilicon gate and generate electron-hole pairs. Holes are pushed into substrate due to the electric field force

in the depletion region. Electrons are attracted and accumulated in the silicon surface underneath the gate. A transmission gate M4 is used to transfer charges from the PG potential well to the floating-diffusion diode (FD) node where charge-to-voltage conversion is done due to its associated depletion capacitance C_{FD}. The voltage change will be buffered and read out through M1-M3.

The dynamic range and conversion gain is a pair of conflictive parameter in conventional APS because the sensing node is used as the voltage conversion node as well. This confliction has been overcome in Photogate image sensor, because in Photogate image sensor, the photon integration and voltage conversion are done separately in sensing node (photogate) and floating diffusion node (FD). By enlarging the photogate area and reducing the Floating Diffusion capacitance, an improved dynamic range and conversion gain in photogate image sensor can be realized. Generally, the Fill Factor is reduced caused by the extra transistor added in the pixel. Due to the existence of overlap polysilicon layer, the light refraction and absorption cause a lower light transmission and thus lower quantum efficiency compared with other types APS sensor. Thus, this structure is dedicated to the high dynamic range and high performance imaging applications in normal natural scenes.

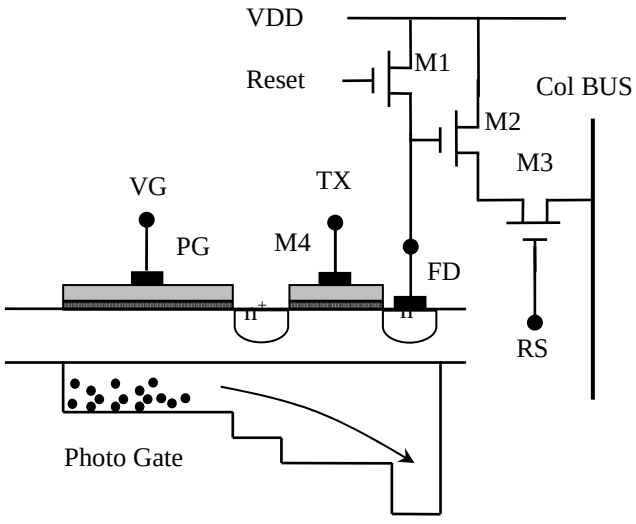


Figure 1. 10. Photogate image sensor

1.1.3.2 Correlated Double Sampling Technique

For suppressing the Fixed Pattern Noise caused by the transistor mismatch in pixels, a technique called Correlated Double Sampling (CDS) is applied in the sensor signal readout cycle. Before starting the photon integration in pixel, the output node is firstly reset to a reference voltage and sampled. And then photocurrent begins to discharge the sensing node voltage. The output node is sampled again after the integration. The pixel final output is the difference value between these two sampling. This two steps readout procedure reduces the reset noise, 1/f noise and FPN caused by threshold voltage variation [23].

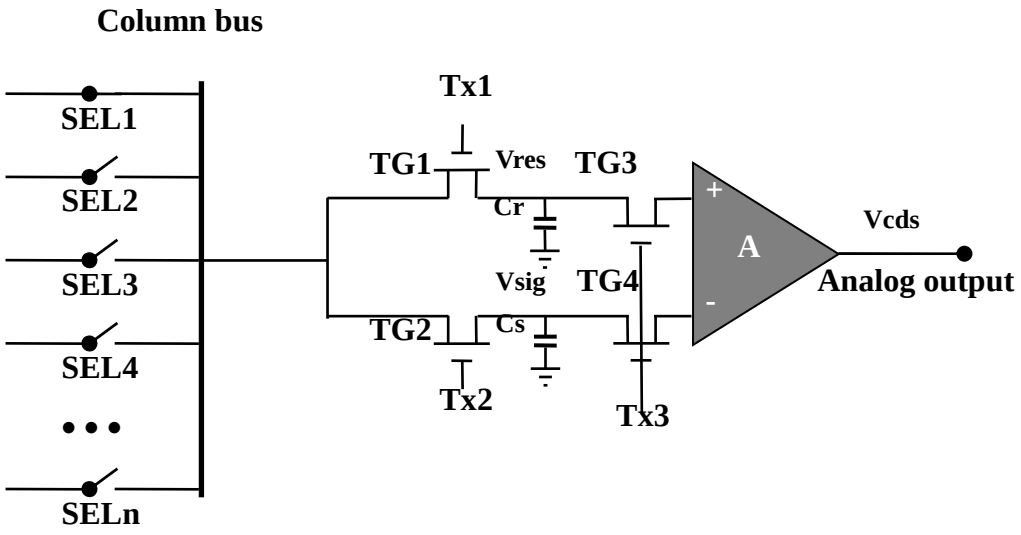


Figure 1. 11. The schematic of correlated double sampling (CDS)

As shown in Figure 1. 11, in a rolling shutter read out mode, only a row of pixels is selected and connected to the column bus each time, for example, the SEL1 is closed and the others is open. The output node reset value and the signal after integration will be sampled by Cr and Cs when closing transfer gate TG1 and TG2, respectively. Then, the voltage on the Cr and Cs will be transferred to the differential amplifier by synchronize switching TG3 and TG4, the final output signal is present by difference of V_{res} and V_{sig}. Then the analog output voltage will be processed into digital numbers by Analog-to-Digital Convertor (ADC).

1.1.3.3 Analog-to-Digital Converter

Nowadays, most of CMOS image sensors chip integrate analog-to-digital converter (ADC), this converter works as the interface to convert a continuous physical quantity (usually voltage) into a digital number that represents the physical quantity amplitude[24]. This is because that the signal robustness, reliability can be kept easily in digital domain. According to the strategy of readout method in CMOS image sensor, the ADC can be classified into three categories: pixel level, column level and matrix level. Due to the simplicity of matrix level ADC, a high pixel fill factor can be maintained without adding extra transistor into pixel, and a better uniformity can be achieved because all pixels share the same ADC, there is no offset during different column and different pixel. But the drawback of this architecture is the larger power consumption due to the higher required bandwidth for processing the large numbers of pixel. In addition, the frame rate is limited by chip level ADC and can not be very high. For a higher frame rate, the column level ADC is always used. The column level ADC readout circuit needs more chip area and hence increases the cost. Another drawback goes to a higher Fixed Pattern Noise caused by the column bias offset and mismatch. A pixel level ADC can achieve theoretically the highest frame rate, but this is at the expense of pixel area resulting in a lower Fill Factor. This readout strategy is suitable for the high speed imaging applications.

The common topologies of ADC can be classified into Slope ADC, Flash ADC, SAR ADC, Pipeline ADC and Sigma Delta ADC. A comparison between the ADCs can be referred as Table 1. 4.

Table 1. 4. The comparison of different ADC architectures

Architecture	Latency	Speed	Accuracy	Area
Flash	Low	High	Low	High
SAR	Low	Low-medium	Medium-high	Low
Sigma-Delta	High	Low	High	Medium
Pipeline	High	Medium-high	Medium-high	Medium
Slope	Low	Low	High	Medium

The algorithm which forms the basis of the Successive Approximation Register (SAR) ADC has a long history. It was first reported implemented in ADC in 1958 [25]. As shown in Figure 1. 12, there are five parts in the SAR ADC.

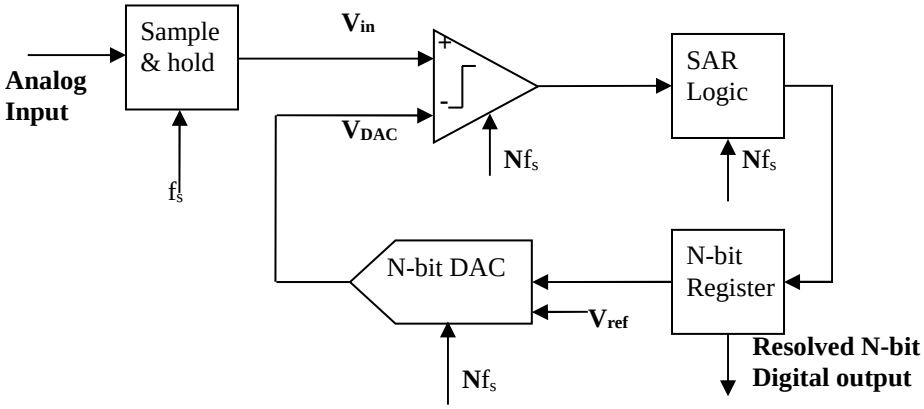


Figure 1. 12. SAR ADC topology [26].

The well known dual slopes ADC is shown in the figure 1.13. The final conversion result is insensitive to errors in component values, and it has greater noise immunity than the other type ADCs.

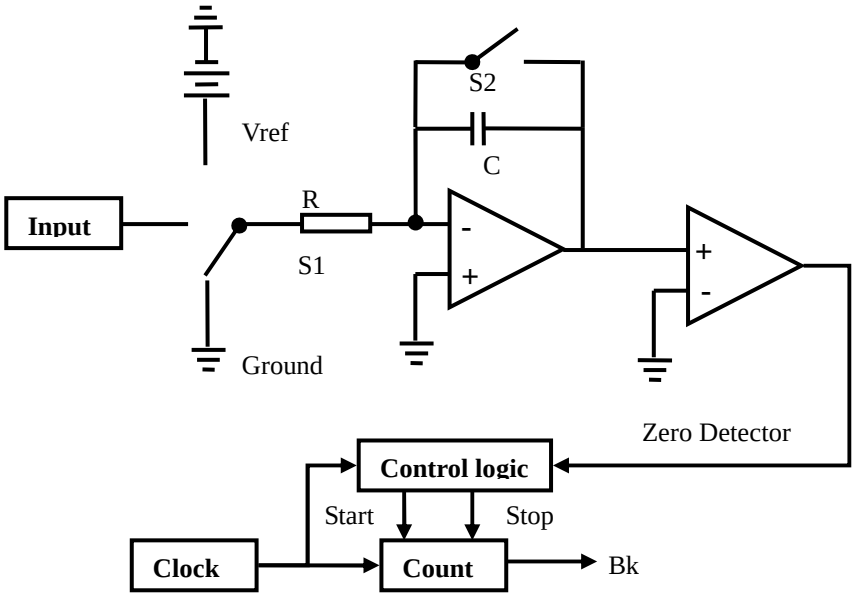


Figure 1. 13. Dual slopes ADC topology.

1.2 CMOS Image Sensor Simulation

The modern circuit design methodology is facing this great challenge due to the gap between the complex application and complex physics. For example, the digital still camera contains lens, image sensor matrix, and signal processing circuit, etc.; it is a multiple domain system. In the electrical domain, the image sensor matrix containing millions of pixels will bring a big problem to circuit simulation tools, as stated previously, each pixel architecture is commonly consists of 3 to 5 transistors. To perform an image sensor matrix simulation, it requires large computational cost and memory consumption. The compromise between simulation time and precision is reached by simulating a small matrix, and then simulation result is used to predict the big matrix performance.

For CMOS image sensor design and performance prediction, it is necessary to verify the design before manufacturing. Different levels of CMOS image sensor simulation and modeling are needed. These simulations include the process development in TCAD, pixel electrical performance simulation in ECAD and modeling in high level, etc.

1.2.1 CMOS Image Sensor Device TCAD Simulation

In the field of Electronic Design Automation (EDA), Technology Computer Aided Design (TCAD) simulation is used for development and optimization of semiconductor device structures. For providing accurate simulation results for a wide range of device technologies based on various material systems, a physics-based approach is employed. The TCAD is expected to give a reliable prediction of the device characteristic and performance due to much physical effects has been taken into account. For solid state imaging study, Synopsys has developed a 3D simulation pixel model and has implemented micro lens on the top of image sensor, Synopsys announced the tool TCAD *Sentaurus* has the ability of developing *Kodak's* next generation image sensor. This tool can analyze the single pixel and mainly focus on the process development. *H. Mutoh* talked how to analyze readout, crosstalk, and light gathering power of micro-lens by the

3D simulation device simulator *SPECTRA* and 3D optical simulator TOCCATA [27]. *A. Crocherie* mentioned a complete 3D simulation flow for CMOS image sensor modeling from photons to electrons, and the strategy is to couple the optical and TCAD simulation results. It is stated that the error between simulation and real image sensor measurement is within a few percents [28], and the simulation accuracy is validated in 1.75um pixel. This methodology is capable of simulating the optical cross-talk in image sensor, and it is mainly used for modeling pixel. The company *silvaco* has developed a simulator for 2D-3D imager simulation [29]. It consists of 3 parts, *ATLAS*, *ATHENA* and *TLAS CLEVER*. *ATLAS* is in charge of simulating input light, and *ATHENA* can convert photons into electrons, and *ATLAS CLEVER* will convert charges (carriers) into output voltage as the output signal. *Crosslight* reported a complete approach for 3D image sensor simulation focusing on the device level, not on 3D stack chip [30]. In 2011, *Z. Essa* [31] reported a full 3-Dimensionnal TCAD simulation methodology for advanced CMOS image sensors. They compared the simulation results with the 2.5D process in both simulation and measurement. Some discrepancy is noticed and further simulation calibration adjustments are required to match experimental Qsat and QE. As reviewed, the TCAD is suitable to investigate the pixel performance versus the process changes. For example, *V. Goiffon et al.* [32] published a study work concerning the pixel performance degradation due to the Total Ionizing Dose (TID) as shown in Figure 1.14.

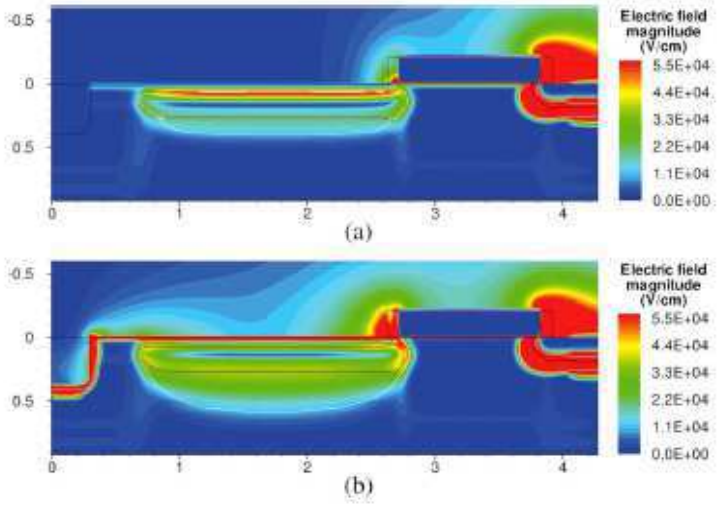


Figure 1.14. The TCAD transient simulation of Pinned photodiode [32]

For the CMOS image sensor process study, the software vendor *Synopsys* has developed a 3D simulation tool. The STMicroelectronics has adopted the Synopsys Sentaurus TCAD tool to study pixel performance, and the simulation results is in good agreement with real measurement.

1.2.2 CMOS image sensor pixel ECAD simulation

The analog design is done in transistor level, and the pixel transistor level simulation is performed in the EDA platform such Cadence, Mentor Graphic. This is a common approach of predicting image sensor behavior in pure design perspective. As the CMOS technology development, the CMOS image sensor pixel pitch continuously shrinks for meeting the market, much higher resolution CMOS image sensor is required to obtain better imaging performance. Commonly, the CMOS image sensor matrix contains tens of millions of pixels. For this big matrix simulation in classical level with conventional SPICE simulator, it needs large simulation time and computer memory. Although this matrix level simulation takes too long time, the SPICE transistor level simulation is still necessary and important for the circuit design. The SPICE level accurate simulation will be more important when the transistor scales to deep sub-micro, more much parasitic effect should be analyzed and thus be able to aware its impact to the high level performance metrics. Thus, from the point of view of whole design flow, a more efficient way should be explored to aware the pixel matrix performance. For accurately representing the MOSFET, the transistor bsim3v3 model involves 300 low level parameters in 0.35um technology. In our test, a typical simulation of 100x100 3T-APS matrix, it lasts 8h. For a matrix of 256x256 pixels, it lasts 2.5 days on the Intel Xeon server running at 2.4GHz with 4GB RAM. Apart from the time consumption problem, we also meet the memory issues when the sensor pixels exceed 512x512. For speeding up the spice simulation time, some new techniques are studied, for example using Look-up table model in the simulation, adopting event-driven algorithm or multi-time steps algorithm to achieve less computation for inactive sub-circuit. The parallel computation method is also studied to speed up the spice simulation. For

example, the Fast-Spice (e.g. Hierarchical Storage and Isomorphic Matching: HSIM) is developed to simulate the circuit with many identical cells, such as memory, it increases simulation efficiency by eliminating redundant calculations, by solving each cell just once for all isomorphic instances. The HSIM can speed up the circuit simulation while sacrificing a little accuracy caused by partitioning.

1.2.3 Modeling CMOS image sensor

For facing the simulation time and accuracy issues, modeling languages are adopted to perform a system level simulation including various modules. These years, for integrating image sensor into a large system, researchers and engineers try to build the image sensor model in higher level modeling language or hardware description language (HDL), such as verilog-AMS, VHDL-AMS, SystemC, etc,. HDL came into design starting from the digital circuit, and a mixed-signal package was developed to extend its description ability to the analog circuit. With this extension, complex mathematical equation which represents time dependent non-linearity effect of device could be integrated into circuit. This achieves an accurate performance prediction.

A VHDL-AMS passive pixel model for Medical Imaging is presented in 2001 by *K.S.Karim*, the leakage current has been taken into account, sensing node capacitance and pixel area is properly modeled in this model, but this model did not integrate the parasitic effects and thus hard to be used to analyze performance variations in the pixels [33]. In 2002, *F. Dadouche* presented a VHDL-AMS Spectral model of photodiode for active pixel sensor [34], a phototransistor model was implemented by VHDL-AMS language by *A. Alexandre* from the same team in 2004. *A. Alexandre* presented that the spectral response of phototransistor model was in good agreement with usual results [35]. This is the first step to elaborate a 2D model of phototransistor which will have probably a large response from near ultraviolet to near infrared by combining both spectral response of each structure, the work towards developing system on chip for imaging. In 2006, *F. Dadouche* reported APS and PPS sensor pixel models based on VHDL-AMS. The presented models got a better time consumption performance than ELDO spice

simulation with nearly equal accuracy [36]. A system level simulation with high level simulator can be achieved after intensively studying and modeling of photodiode and pixel from 2002 to 2006, this approach can simulate image sensor matrix, but it did not take pixel variability into account. In 2005, A VHDL-AMS active pixel model for heterogeneous system design was presented by D. Navarro [37]. It gained a 35% faster than SPICE in the simulation of the same matrix 100x100. In his work, a 0.35μm technology based parameterized pixel model was developed, and this model enables scale the technology down to 0.18um and 0.12um. The approach moved towards matrix level and can accept an image as the input signal, but a limitation was found due to the internal error occurring when the matrix size (pixel numbers) was too large. The company *Desert Microtechnology* [38] published an application note to report the mixed mode capability of SMASH which is a mixed-mode, mixed languages and multi-level simulator. They talked about the complete simulation of single chip camera, sensor model and functional module is implemented in Verilog and Verilog-A language. They reported that more than 10 hours were needed to run SPICE-level simulation of 63 pixels in their article [39]. Although this approach is complete and easy to be performed, it does consume too much time. *F. Cenni* proposed a model of CMOS video sensor based on *systemC* in 2011. The work was focused on the system level integration, all necessary parts including Bayer filter, lens, timer, pixels, ADC are all simply modeled. The work is dedicated to develop a complete approach, and the suitability of SystemC AMS for the virtual prototyping is demonstrated in this work [40]. The accuracy and some non-linearity of pixel response will be considered in their future work.

Although these approaches can simulate image sensor matrix, they are difficult to be integrated into classical analog design flow, this is not convenient for sensor development. Another point is that, they did not solve the time consumption problem in big sensor matrix simulation.

1.2.4 CMOS image sensor algorithm level modeling

For system level image sensor performance evaluation, some function and algorithm using mathematic equation to represent the sensor behavior has been studied. *T. Chen* worked on digital camera system simulator (vCam) in Stanford University in 2003 [41], he introduced a complete simulation procedure from optical signal to the final digital numbers, he physically modeled optics pipeline based on the lambertian light source for image acquisition, and the parameters extracted from 3T-APS on the various technologies (0.35μm, 0.25μm, 0.18μm) are used in the simulator. This vCam is capable of optimizing pixel size through achieving a better tradeoff between the sensor performances (dynamic range, etc.), sensor die size, optics characteristics and imaging constrains. He also investigated the methodology of multiple captures for achieving high dynamic range imaging. The approach is very complete, but for sensor performance prediction it needs an accurate model, normally, this accurate model is not easy to get. *Joyce E. Farrell* presented Image Systems Evaluation Toolkit (ISET) in 2004 [42]. The ISET Digital Camera Simulator simulates the complete digital camera reproduction pipeline. D. Navarro presented a model based on Matlab-Simulink in 2007, via a valid model with 5% error compared to spice simulation, the 100x100 pixels matrix simulation time could be reduced largely from hours to seconds [43]. *Pixpolar* introduced an on-line image sensor simulator for evaluating the sensor performance [44] in 2009. It provides some parameters including quantum efficiency, dark current, exposure time, and pixel size which affect the sensor performance. The standard deviation of point spread function (PSF) is used to represent the crosstalk. To keep the generality, the *pixpolar* used a general pixel structure to represent the sensor matrix, and more, the simulator did not consider the system performance changes caused by process variation. *J. Chen* presented a digital camera simulator based on ISET framework in 2011, it took more noise components model into account and optical crosstalk is also included in the simulation [45]. *R.J. Woodworth* have designed a Verilog VPI, this VPI co-simulate the image sensor with some external tools, such as C/C++, they can read in an image and

display the simulation result in images, it could be potentially used for developing image processing algorithm in high level [46].

1.2.5 Conclusion

For studying the CMOS image sensor, TCAD simulation has been performed to investigate the impact coming from the CMOS process. The TCAD image sensor simulation can give guidance for pixel device optimization, especially from the process aspect. For image sensor electrical performance study, the pixel is structurally modeled in CMOS transistors. The pixel SPICE level simulation can give a reliable performance prediction versus transistor dimension size and aspect ratio changes. It allows achieving an optimal image sensor pixel in electrical layer. For image sensor system integration, a relative higher level description language (e.g. *VHDL-AMS*) is commonly adopted. This description modeling language provides the flexibility of building a big sensor matrix. As the key parameter extraction strategy is always applied to simplify the image sensor model in this approach, some parameters in the netlist (e.g. oxide layer thickness) will not be included in the high level model any more. This will bring some constrains to study sensor performance in high level. The image sensor can also be modeled mathematically based on the theory and experimental data, this mathematical model is normally used to represent the system performance or be integrated into a hybrid system as a functional part. From the aspect of analog design, a more complete design flow and possibility of simulating big matrix are more important. According to the discussion above, performing image sensor performance prediction in ECAD level is needed. The methodology which can be integrated in the classical analog design flow is more interesting.

1.3 Research Focus and challenges

As reviewed above, the TCAD simulation is for the process development and is capable of simulating the devices performance versus the process physical parameter

changes. ECAD simulation, especially for the SPICE like classical simulation, the large circuit can be simulated, it is capable of simulating circuit performance variation according to the circuit parameter changes, but the large time consumption limits its usage in very large circuit or system level simulation. In various modeling languages, such as VHDL-AMS, SystemC AMS, the simulation capability is greatly enhanced via modeling languages but the simulation accuracy is strongly dependent on the model. For achieving high accuracy and high agreement with transistor model (BSIM) based simulation, lots of work and effort need to be done for validating the model. For algorithm level modeling of image sensor in Matlab or C language, a mathematical transfer function is usually used to represent the image sensor. This can give out an expression of sensor's behavior in a short simulation time, but it is at the expense of accuracy and reliability. Even if the noise, parasitic effect could be extracted and added into the sensor algorithm level model, it is very hard to handle the simulation and predict accurately pixel electrical performance.

So, for a better tradeoff between the simulation accuracy and simulation speed, a new approach which can handle the accuracy within the reasonable time consumption should be explored on electrical level in classical design environment. This allows for studying sensor matrix performance (high level) versus design low level parameters (w, l), further more, the sensor matrix response variation (such as Fixed Pattern Noise) caused by process parameter can be studied in electrical level. The new simulation methodology is dedicated to improve the simulation capability and efficiency in classical design environment.

1.3.1 Accuracy & Time consumption

As the CMOS technology evolves from generation to generation, the CMOS transistor feature size continues to shrink, this brings new challenges to the CMOS integrated circuit design. The parasitic effects results from semiconductor material and fabrication process is becoming a more significant issue in modern circuit design. To predict accurately transistor and circuit performance, it needs a much more detailed

model and effective Computer Aided Design tool with large computation cost. The low level circuit design platform, such as Cadence, Mentor Graphic, etc, they integrate SPICE like simulator with supporting transistor *BSIM* models. Although this classical ECAD simulation methodology gains adequate accuracy, it is time consuming when facing very large scale circuits (a big netlist). Owing to the complexity of circuit and huge numbers of transistors, the classical ECAD is facing the new challenge of predicting performance of large scale circuit in a short time. For example, a testbench composed of a 120x120 3T-APS pixels matrix, 120 row select signal generator, 120 row reset signal generator, and a 120x120 photocurrent source is built in *Cadence with 0.35um technology*. It took long time to accomplish the simulation of image sensor testbench with Spectre simulator on the Intel Xeon server running at 2.4GHz and with 4GB RAM. As shown in Figure 1.15, the classical SPICE simulation time increases drastically as increasing the pixel numbers indicated by the red line with yellow mark, such as 1.5 days for 120x120 pixels, while as indicated by the predicted data (gray line with black circle), it will consume 50 days to complete simulating a sensor matrix containing 1024x1024 pixels. Nowadays, along with the evolving of CMOS technology, the simulation accuracy is becoming more and more critical, further more, the imager resolution is becoming higher and higher (4096 x 4096 soon after), for maintaining the simulation accuracy in spice simulation is an issue.

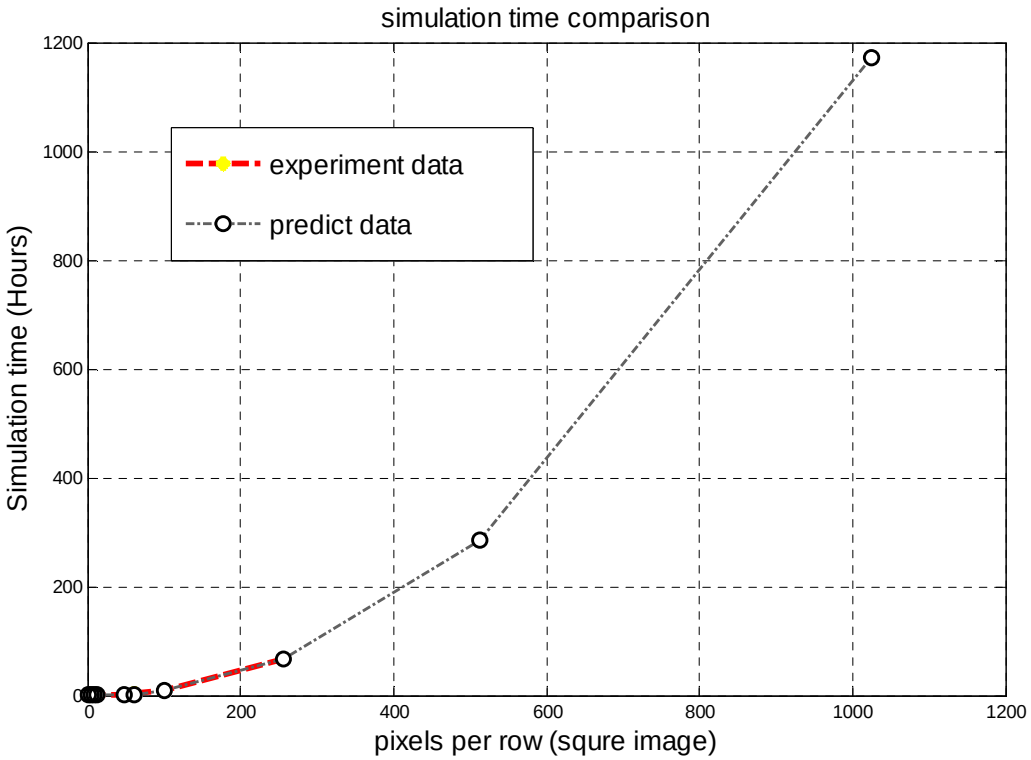


Figure 1. 15. The time consumption of classical SPICE simulation

1.3.2 Pixel matrix response variability

In the CMOS pixel matrix, each pixel is identically designed to get the uniform response when exposed to the same luminosity, but owing to the small variation in the process, the identical response can't be achieved. The photon response non-uniformity (PRUN) is an issue in CMOS image sensor and this is caused by the light distortion, CMOS process variation and fabrication defect. For example, the doping variation exists between the wafers, which will bring the pixel response variation in different dies; the etching variation in each individual pixel during the fabrication leads to different characteristics and performance among pixels on the same die. The leakage current in each individual photodiode is slightly different and CMOS transistor dimension size is with little difference caused by the etching variation, all of these will induce performance variation in pixels. Although Correlated Double Sampling (CDS) has been applied to

suppress some aspects, some part of FPN caused by photodiode leakage current, variations in photodiode size and variations in photodiode capacitance [47] still exist in the output.

The second focus of this thesis work is to explore a new methodology for helping analyzing noise and variability.

1.4 Key contribution of this work

This thesis work explores a novel approach of simulating image sensor matrix. The new proposed simulation methodology is developed on the 3T-APS architecture. Its portability is checked through applying it on the other pixel architectures. This simulation methodology is proved to be an alternative of parametric classical simulation.

For the sake of improving simulation speed and maintaining the accuracy, a scalable simulation method is explored in this work. It combines the low level classical SPICE simulation with high level parameter abstraction and high level algorithm. The simulation precision is reserved and the scalability is extended. This methodology is used to predict the CMOS image sensor matrix performance, and it improves the capability of Classical EDA tool to handle large scale circuit simulation.

1.5 Thesis Organization

This thesis is organized into 5 chapters. In Chapter 2, fast scalable and variation awareness methodology is detailed. It is based on the SPICE simulation and higher level parameters abstraction strategy. A Look-Up Table (LUT) is used in the methodology for reducing the computational cost, an approximation method is adopted in the whole approach for generating high level parameters. A User Graphical Interface implemented for connecting the low level design parameter with high level circuit performance is presented.

In chapter 3, the 3T APS pixel architecture and performance metrics related parameters are introduced and studied, the pixel matrix simulation with the proposed methodology is presented. The performance, such as accuracy, time consumption, memory consumption, and scalability are talked in this part.

In chapter 4, the methodology is applied on other image sensor architectures to prove its portability. The pixel structures such as PPS, log-APS, 4T, 2T5, 1T75 and CNTFET based 3T-aps are introduced and simulated using the proposed methodology. All the related simulation results are presented and discussed.

Finally, in chapter 5, the contribution of this work is summarized and directions of the future work are suggested.

CHAPTER 2 CMOS Image Sensor Design & Fast Simulation Methodology

A series of simulation methodology have been developed in the past decades for developing image sensor. TCAD simulation is dedicated to investigate sensor performance versus process and parameters which belongs to physical domain. The classical ECAD simulation can give a prediction of sensor electrical performance. The modeling language, such as VHDL, VHDL-AMS, is capable of simulating image sensor matrix with peripheral functional circuitry. Some explorations of sensor simulation have been studied based on Matlab and C++. People try their best to complete the design flow of image sensor, but it needs to study separately the pixel in each individual domain. For completing the design flow, a fast simulation methodology in electrical layer is explored. The pixel design, signal analysis, and signal processing are all included in the methodology. In this chapter, the fast simulation methodology will be introduced.

2.1 Pixel design

2.1.1 Photodiode

2.1.1.1 Photodiode photoelectric property

The photodiode is widely adopted in modern image sensor design and imaging system development. The photons injecting on the active area of the photodiode will excited electron hole pairs which is potentially generated as the photocurrent. The parameter Responsivity $R(\lambda)$ is used to characterize the capability of converting the light into photocurrent, expressed in practical units of ampere of photodiode current per watt of incident illumination as refer to equation [2. 1].

$$R(\lambda) = \eta \frac{e}{h\frac{c}{\lambda}} \qquad [2.\ 1]$$

Where, e is the electronic charge, η is the quantum efficiency (Q.E.), λ and c is the wavelength and velocity of incident light, respectively, h is the Planck's constant. The responsivity increases as the wavelength becomes longer, for example, when η=80% and at the 430nm, the responsivity is equal to 0.28A/W, whereas at 900nm with the same quantum efficiency, the responsivity is 0.58A/W. It is worthy of noticing that the cut off at long wavelength (1.1μm) will occur for a silicon photodiode due to the photon absorption decrease largely and photon energy is just sufficient for transferring the electron across the silicon band cap. As shown in Figure 2. 1, the photon responsivity of photodiode varies with the light wavelength, it increases over the whole visible light spectrum range (380nm to 720nm), and this end at 1.1μm approximately.

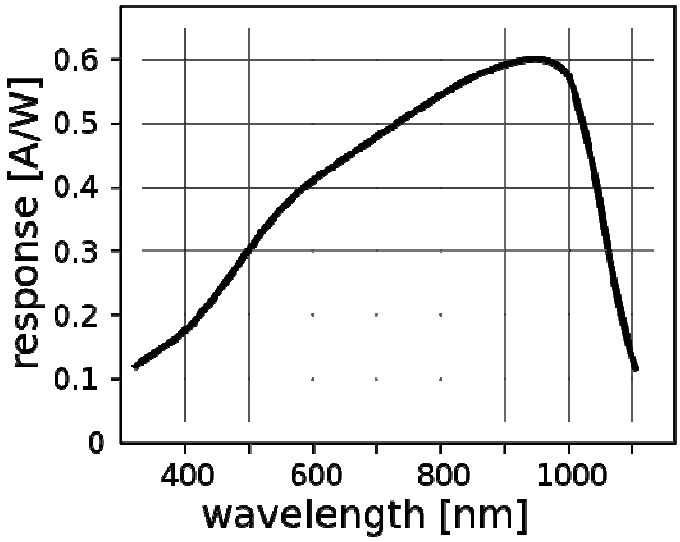


Figure 2. 1. The responsivity of silicon photodiode

2.1.1.2 Photodiode electrical model

The photocurrent increases with the light intensity when the photodiode is reversely biased at the photoconductive mode, and the photocurrent nearly does not increase with the reverse biased voltage increasing. As shown in Figure 2. 2, the illumination intensity E_3 is higher than the other three E_2, E_1, and E_0. There is small current flowing through the photodiode when it is under non-illumination condition, this small amount of current is usually called leakage current or dark current, as shown in red line.

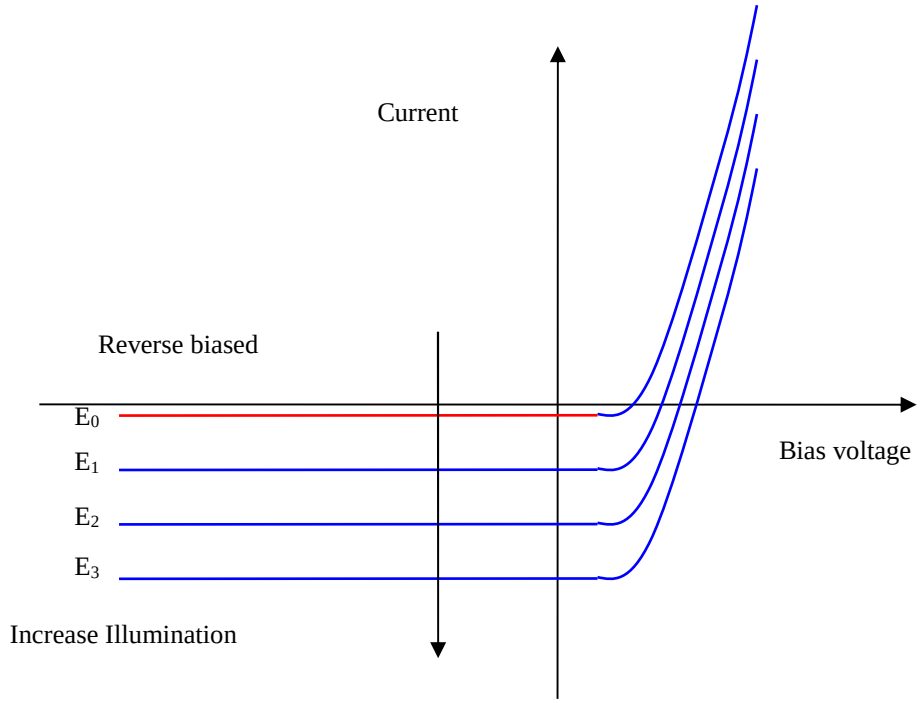


Figure 2. 2. Photocurrent light intensity characteristic of photodiode

As indicated in the Figure 2. 3, the photodiode can be represented by its equivalent circuit shown on the right hand.

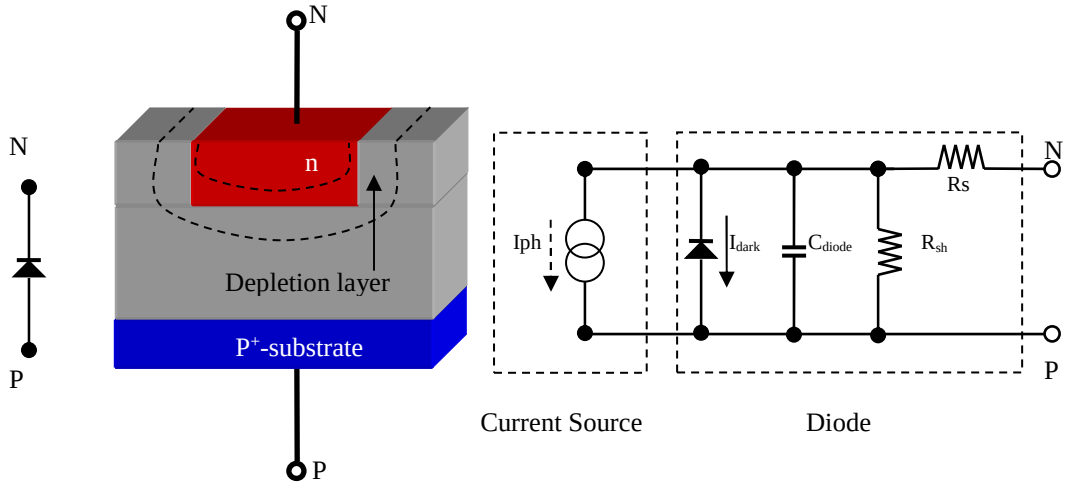


Figure 2. 3. The symbol of photodiode (left) and the equivalent circuit of photodiode (right)

The photodiode equivalent circuit is adopted in this work because its electric schematic can be simulated with the electrical simulator. The photodiode can be modeled as a current source connected in parallel with a common substrate diode. The photocurrent I_{ph} is proportional to the incident light intensity, and I_{dark} represents the leakage current under non-illumination condition which is highly dependent on the photodiode shape and the ambient temperature.

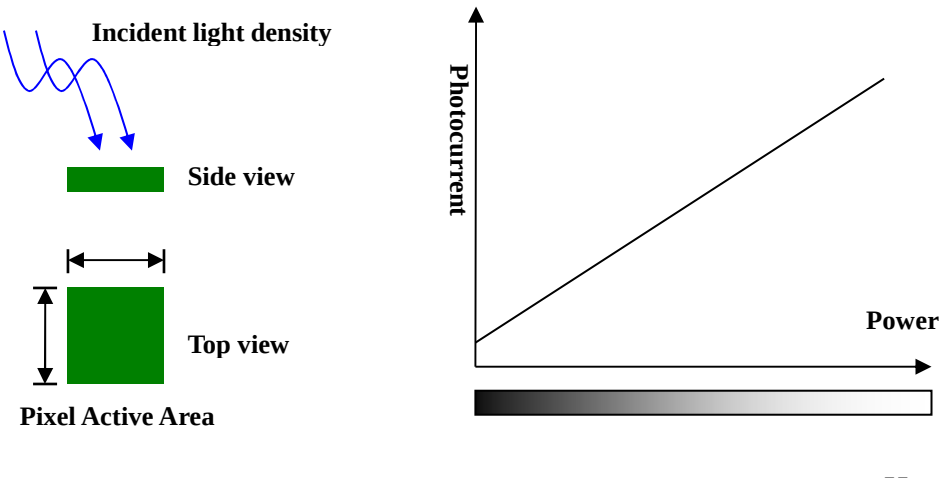


Figure 2. 4. Photodiode and Photocurrent converter

As shown in Figure 2. 4, the light injected on the sensor focal plane (pixel active area) has a dependence on the pixel active area. The photocurrent as a function of light power is given by equation [2. 2].

$$I_{ph} = (P_{mean} \times PD_{area} \times Responsivity) \times Grey \qquad [2.\ 2]$$

Where, P_{mean} stands for the mean power density on the sensor focal plane, PD_{area} represents the photodiode dimension size, R is the responsivity of the photodiode, *Grey* is the grey value of the image pixel ranging from 0 to 255. In the converter, the photodiode responsivity is set to 0.6 and P_{mean} is assumed to be $1 mW/m^2$.

2.1.2 CMOS transistor

2.1.2.1 MOSFET threshold voltage

The threshold voltage of MOSFET transistor is the value of the gate-source voltage when the conducting channel is formed and just begins to connect the source and drain contacts of the transistor [50]. The MOSFET threshold voltage can be expressed as [2. 3]:

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \quad [2.\ 3]$$

Where, V_{th0} is the MOSFET threshold voltage when the bulk-substrate is at zero bias condition, ϕ_F is the strong inversion surface potential. γ is the body effect parameter. Due to the threshold voltage is sensitive to the CMOS process, and its variation will cause the performance degradation, for example, induce noise to the sensor matrix. This key parameter is critical when studying sensor matrix response variability.

2.1.3 CMOS 3T-APS Structure Model

A CMOS 3T-APS pixel as represented by its equivalent circuit in Figure 2. 5, the pixel is constructed by 3 CMOS transistors M1, M2, M3 and a CMOS photodiode. The M1 is in charge of resetting the photodiode before the photon integration. The integration begins when the reset transistor M1 is turned off, and the generated electrons will be accumulated on the node PD after a certain time (exposure time or integration time). The electrons form a voltage on the PD node due to the associated capacitance on it (C_{PD}) and cause a voltage drop down from the initial reset level, and the voltage on the node PD is buffered by the pixel inner amplifier M2 through the switch transistor M3 to the column BUS. The transistor M4 located at the bottom of each column is commonly used as the current source, and it work as the active load of the amplifier M2. The bias voltage ensures the M4 to be operated in the saturation region, and it determines the signal foot level as well.

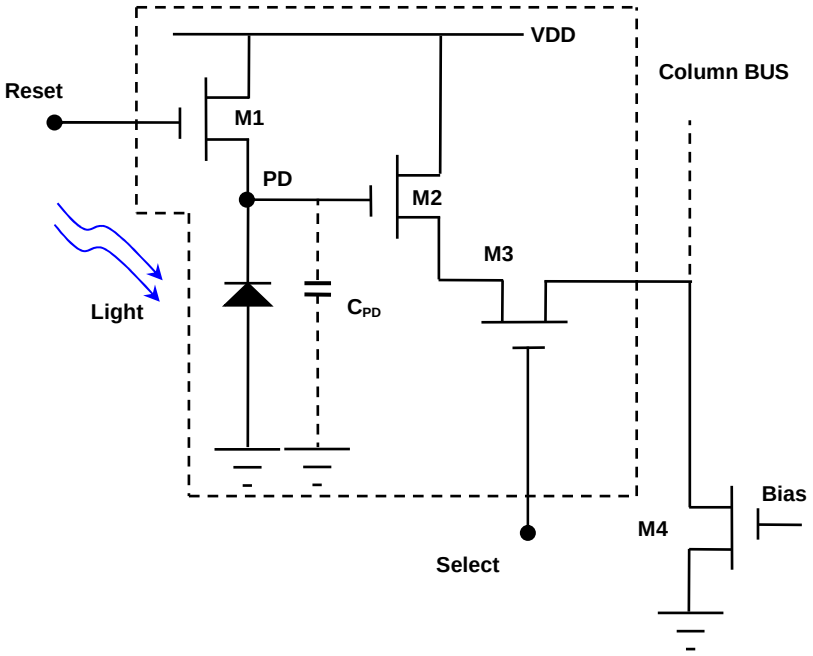


Figure 2. 5. The 3T-APS pixel schematic

2.2 CMOS Image Sensor Simulation methodology

In a CMOS image sensor *3T-APS* pixel, there are 3 transistors and 1 photodiode. On an imager matrix of 256x256 pixels, there are 196608 *MOSFET* transistors and 65536 photodiodes. For the prediction of this whole sensor matrix's performance, the SPICE simulator has to solve 130K equations [52] in classical simulation. Millions of on chip transistors make the SPICE simulation hard to be setup and performed, and too much computational cost is needed. For example, days are needed for a simulation of 512x512 pixels matrix on the Intel Xeon server running at 2.4GHz and with 4GB RAM. The large time consumption is a problem of sensor matrix classical simulation with using the SPICE simulator. The main reason is that: firstly, the transistor model (BSIM) is adopted for accuracy, the more parameters in the model, the more complexity of equivalent circuit and much more computational cost would be, secondly, the circuit scale determines directly the simulation time as well (e.g. the transistor numbers).

For overcoming the time consumption problem of image sensor matrix simulation in Cadence design environment, a fast scalable simulation methodology is explored. The new simulation methodology is fully implemented and integrated in Cadence circuit design platform.

2.2.1 Developing language & Simulator

2.2.1.1 SKILL Description Language

SKILL is a script language owned by Cadence Design Systems [53]. The SKILL programming language provides the possibility of customizing and extending the Cadence circuit design environment. The advantages of using SKILL are summarized as follows:

- Capability of integrating user define function
- Capability of communicating between various Cadence tools
- Easy to be understand for its C like Syntax

2.2.1.2 Spectre Simulator

Simulating the circuit with *SPICE* is the common way to verify circuit operation at the transistor level before committing to manufacturing an integrated circuit.

SPICE was developed at the Electronics Research Laboratory of the University of California, Berkeley by Laurence Nagel. *SPICE1* was first presented at a conference in 1973 [5]. There are several new private versions of *SPICE* have been developed, such as *Spectre* (Cadence), *Eldo* (Mentor Graphics), *ADS* (Agilent), *HSPICE* (Synopsys) now. The Cadence built in simulator “Spectre” is adopted in this thesis work.

2.2.2 Fast Simulation Methodology

The fast simulation methodology is based on the transistor low level *SPICE* simulation and high level modeling algorithm, it is intended as an alternative of classical simulation methodology when simulating big netlist (e.g. matrix configuration). The main idea is that only few times of low level *SPICE* simulation are performed firstly and then the detail information from low level simulation will be extracted and pumped up to the higher level modeling algorithm. The extracted data will be used to generate a higher level model for accelerating the whole simulation. Thus, the simulation time is reduced and the high accuracy could be achieved in the final simulation results. As shown in Figure 2. 6, the design flow starts with a single pixel specification, the *stimulus sampling* function will sample the possible photocurrent into an input table, and the length of table determines the numbers of low level SPICE simulation, then pixel level parametric transient simulations are performed to get the pixel output voltages table for all the sampled photocurrents. In this way, a sampled input-output database is obtained by performing low level simulation, and the sampled database is stored as a reference of fast calculation. The work principle of LUT is introduced in the following subsections. For an 8 bit gray level image, there are 256 ($=2^8$) gray levels and thus the fast method requires 256 low level simulations, for a 10 bits image, the number is 1024 ($=2^{10}$). A table between the input photocurrent and output voltage is established after these classical transient simulations. Then, the table works as a transfer function which can estimate output voltage when giving an input photocurrent.

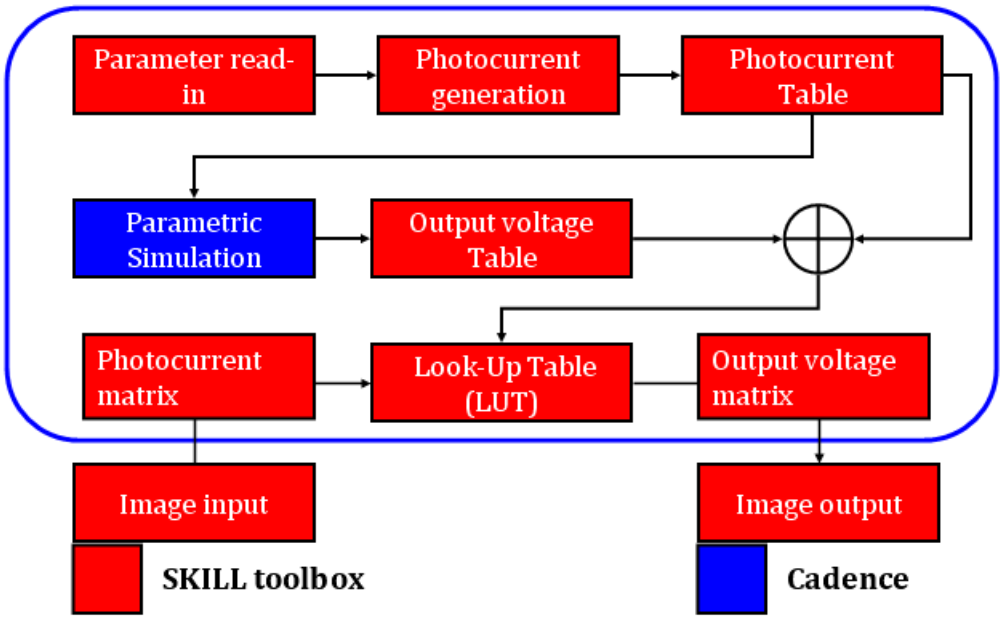


Figure 2. 6. Design flow of fast simulation methodology

2.2.3 Parameters & Pixel simulation

In the electrical simulation, the common solution is to use the pixel equivalent circuit rather than an analytical model based on physics. In a sensor matrix 100x100, there are 10^4 pixels (3 transistors and 1 photodiode in our case). A large netlist representing the sensor matrix module and stimuli (photocurrents) is needed for performing the real sensor matrix level classical simulation. Owing to the complex interconnection, it is difficult to get this big netlist in Cadence Analog Design Environment. Besides this netlist problem, assigning photocurrent to each pixel is a problem as well. In this thesis work, for solving the netlist problem, a single pixel based simulation methodology is studied, and it is called “classical method” at the reset of this thesis. For solving time consumption problem, a simulation speed improved approach is proposed and explored, and it is called as Fast simulation.

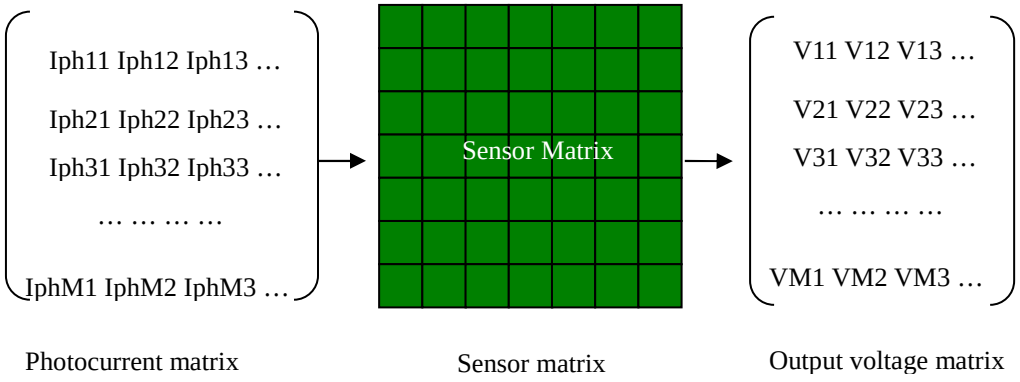


Figure 2. 7. The scheme of sensor matrix stimuli and response

Normally, a photocurrent is needed to represent the pixel associated luminosity in simulation, so the number of photocurrent should be equal to the pixel numbers in the matrix as shown in Figure 2. 7, and for coding scene luminosity, the equal numbers of output voltages are required. For reducing the circuit complexity and hence reducing the time consumption, a specified pixel equivalent model is simulated instead of the whole matrix as shown in Figure 2. 8. If treated the sensor as a special box, then we get that the box outputs (voltage) is a function of its input (photocurrent). How to design this box, how to generate the input parameters and how to attain the output parameters is the main work of this thesis.

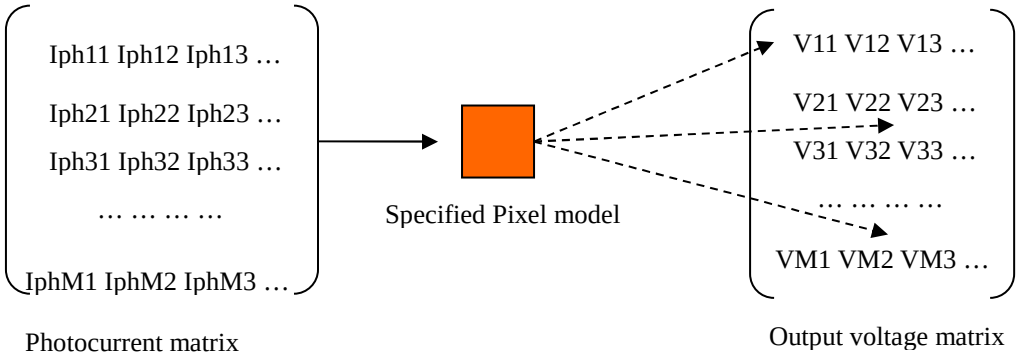


Figure 2. 8. The image sensor matrix simulation methodology

2.2.3.1 Input parameter: Photocurrent

The simulation data flow starts from an input picture, the intensity of the input picture is read out and converted into a gray level image. The gray level image is processed and converted into a light intensity (photocurrent) matrix. All the photocurrents are stored in the memory and work as the stimuli in the matrix level simulation. After setting the pixel structure and parameters, the classical spice simulation is performed using the photocurrent matrix and the simulation results are sampled and saved in curves and images.

The true color uncompressed *bmp* image is used to generate the photocurrent source as the stimuli in the simulation. Normally, in a color image, the primary colors (Red, Green, and Blue) are used to represent the color information of a captured scene. Each primary color is divided into 256 (=2^8) levels represented by the integer value from 0 to 255 in a 8 bit color image, so there are totally 2^{24} (=2^8*2^8*2^8) combinations to represent the whole color space. It is believed that any color can be generated by mixing these three primary colors. For example, the black color can be achieved if the R=G=B=0 and the white color can be achieved if R=G=B=255, a pure red color can be represented by R=255, G=B=0, etc. In grayscale image, there are just two colors, black and white. There are many shade of gray between black and white, for example, in an 8 bit gray image, the value (0 to 255) is used to represent the intensity of light.

Note: red, green and blue is abbreviated as R, G, and B, respectively.

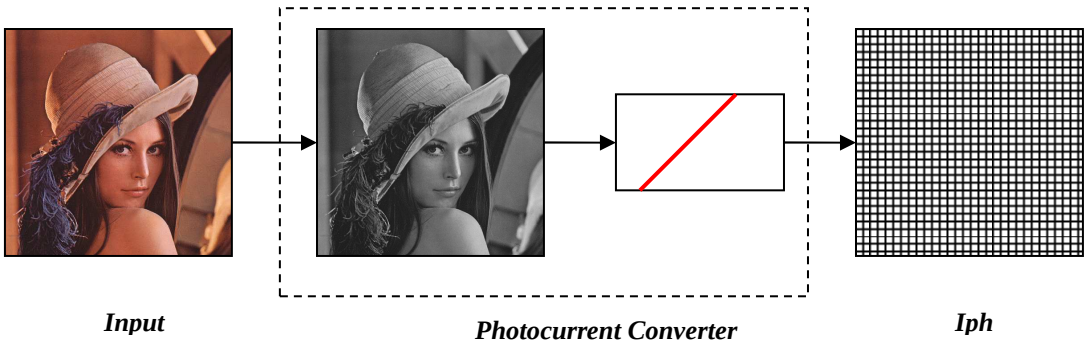


Figure 2. 9. The dataflow of input signal

As shown in Figure 2. 9, an input color image can be converted into the grey level image by extracting its *R*, *G*, *B* value and processed by equation [2. 4].

$$Grey = 0.29R + 0.6G + 0.11B \quad [2.\ 4]$$

A conversion operation (*refer to section 2.1.1*) is applied to the grey values to generate the photocurrent matrix. In the simulation each pixel in the original image has a correlated photocurrent in the stimuli, such as Iph0_0 presenting the photocurrent correspond to the pixel value located in the coordinate (1, 1) in the original image, this order shift is caused by the *SKILL* language syntax.

2.2.3.2 Pixel simulation

The Simulation environment is set up in the Cadence platform with AMS 0.35μm design kit. As shown in Figure 2. 10, in the pixel test bench, a current source is added in the pixel structure to represent the photocurrent. The "*reset*", "*select*" terminal is driven by the pulse generator, and the column is biased by a constant voltage source.

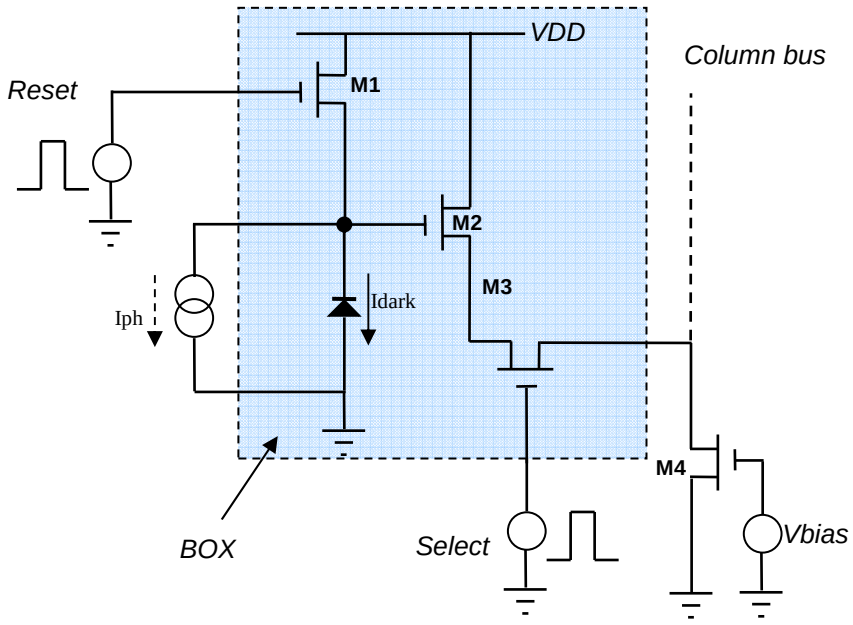


Figure 2. 10. The single pixel simulation schematic

In photodiode based 3T-APS case, because there is no "*memory*" in the pixel, so it is not allowed to implement a real correlated double sampling technique. In this thesis

work, a select window is used to sample the pixel output signal (“*Vout_sample”*) at the end of integration. Because the “*select*” transistor is driven by pulse generator, so “Vout” remains “0” before the “Vout-sample” sampling front edge arriving as shown in Figure 2. 11, and it is not allowed to sample the real reset voltage (“*Vout_reset”*) during the reset phase, by modifying the timing of pulse generator during the simulation, an effective sampling before the end of reset phase is achieved. For sampling the pixel reset voltage (“*Vout_reset”*) and pixel signal voltage (“*Vout_sample”*), the simulation needs to be performed once for each sampling. According to the double sample technique and the work principle of photodiode, subtracting the sample voltage from reset voltage, the CDS voltage 0.8025 (=1.588 - 0.7854) is obtained for coding luminosity. The 0.7854 is the average value of output voltage restricted by select window, and 1.588 is the output voltage at 1us before the end of reset phase.

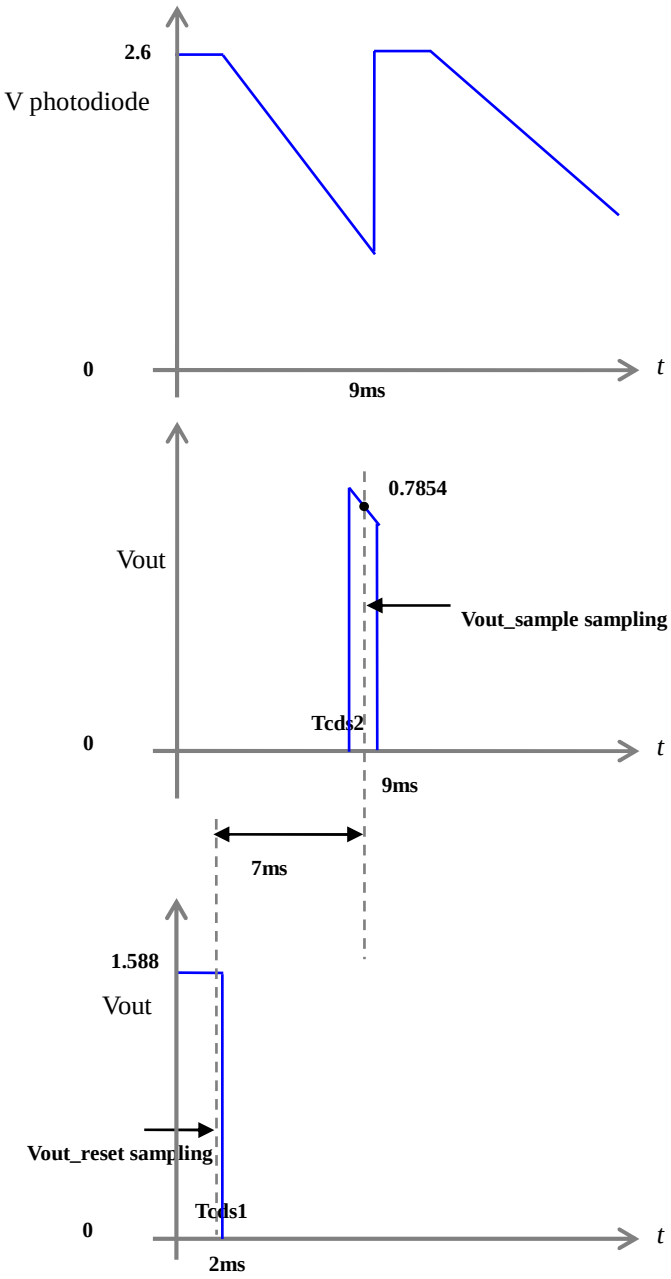


Figure 2. 11. 3T APS pixel discharge curve in photocurrent 10pA

2.2.4 Capacitance consideration

On the pixel matrix level, the pixels can be considered into columns and rows. The column structure is shown in Figure 2. 12. All the output nodes from each pixel located on the same column are connected parallel to the same output line. P11, P21, PM1 represent the first, second and the M^{th} pixel in the first column, Vout1 is the column output node of the first column. The pixel response of this column structure is listed in the Table 2. 1. V1, V100, V200, V300, V400 represent output voltage of the first, hundredth, two-hundredth, three-hundredth and four-hundredth pixel in the same column.

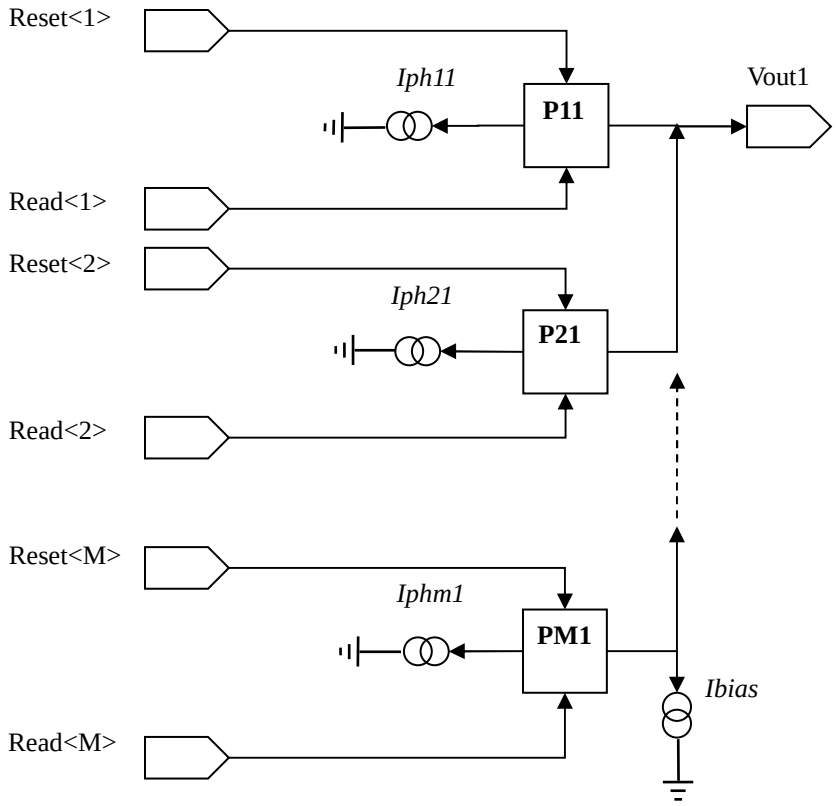


Figure 2. 12. Testbench of column pixels

Table 2. 1. Output voltage comparison of column structure and single pixel on schematic at non-illumination condition (volt)

V	V1	V100	V200	V300	V400	Single pixel
Vp_reset	1.6110035	1.6110035	1.6110035	1.6110035	1.6110035	1.6109666
Vp_out	1.3402704	1.3402704	1.3402704	1.3402704	1.3402704	1.3402585
Vcds	0.2707331	0.2707331	0.2707331	0.2707331	0.2707331	0.2707081

Where, the Vp_reset is the pixel output node voltage after pixel reset operation, and Vp_out is the voltage on the output node after photon integration. The Vcds is the correlated double sampling output voltage which is obtained by subtracting Vp_out from Vp_reset. All the pixels have the same output voltage in the column structure (in red color), but comparing with single pixel structure (in black color), a small voltage difference is observed. This difference is caused by the column capacitance which increases the capacitive load of pixel inner source follower, and this column capacitance lowers down the sensor speed by reducing the effective bias current which is mainly caused by leakage current passing through the C_{GS} of switch transistor (M3) in the neighboring pixels. Due to existence of leakage current in photodiode, the Vcds under non-illumination is not 0 volt as expected. As indicated in the Table 2. 1, this small leakage (dark current) current will discharge the sensing node during the whole integration and cause a 0.27v offset.

The column capacitance affect the pixel performance, so for better simulation accuracy, the capacitance should be included in the simulation. In order to identify and investigate the capacitance effect, the following consideration is taken into account in the image sensor simulation methodology.

2.2.4.1 No column capacitance

When considering using the single pixel to represent the sensor matrix and neglecting the cross talk from the neighbouring pixels, all the pixel on the matrix share the same pixel model and there is no consideration of the impact from the other pixels

on the chip. A closer view of the pixel model without parasitic capacitance from neighbouring pixels is shown in Figure 2. 13.

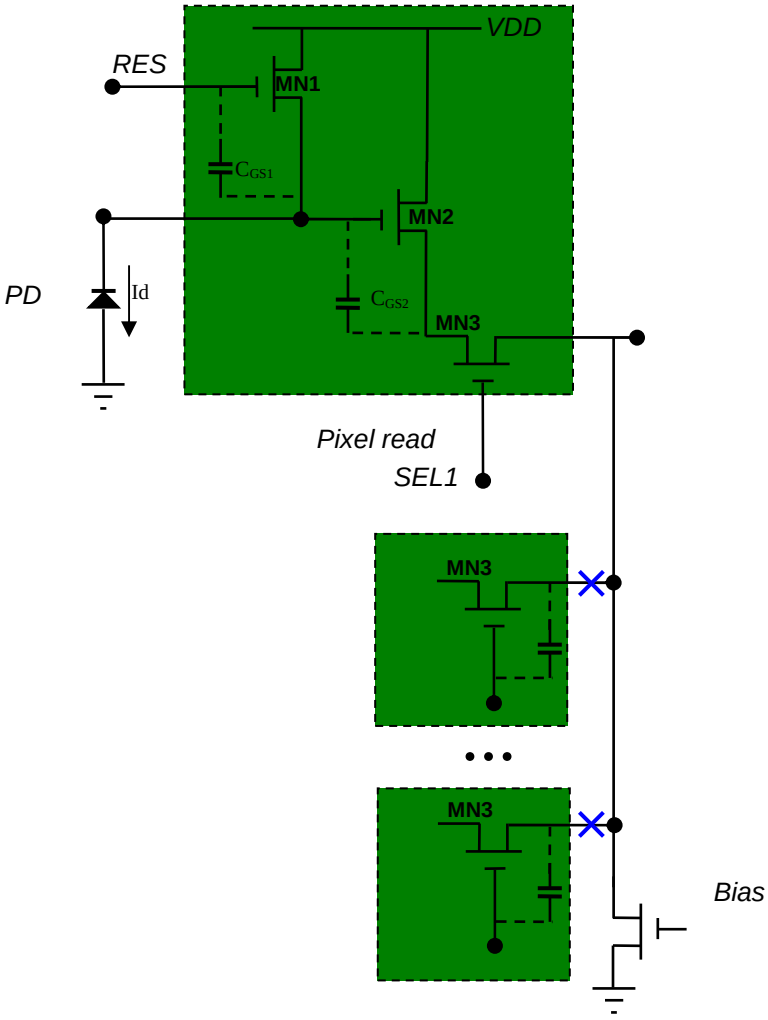


Figure 2. 13. Pixel model with no column parasitic capacitance

2.2.4.2 Equivalent parasitic capacitance

Considering the impact of parasitic capacitance on the matrix, the column parasitic resulting from the common connection of each pixel output node in the same column is taken into simulation, a closer view of the column structure is shown in Figure 2. 14.

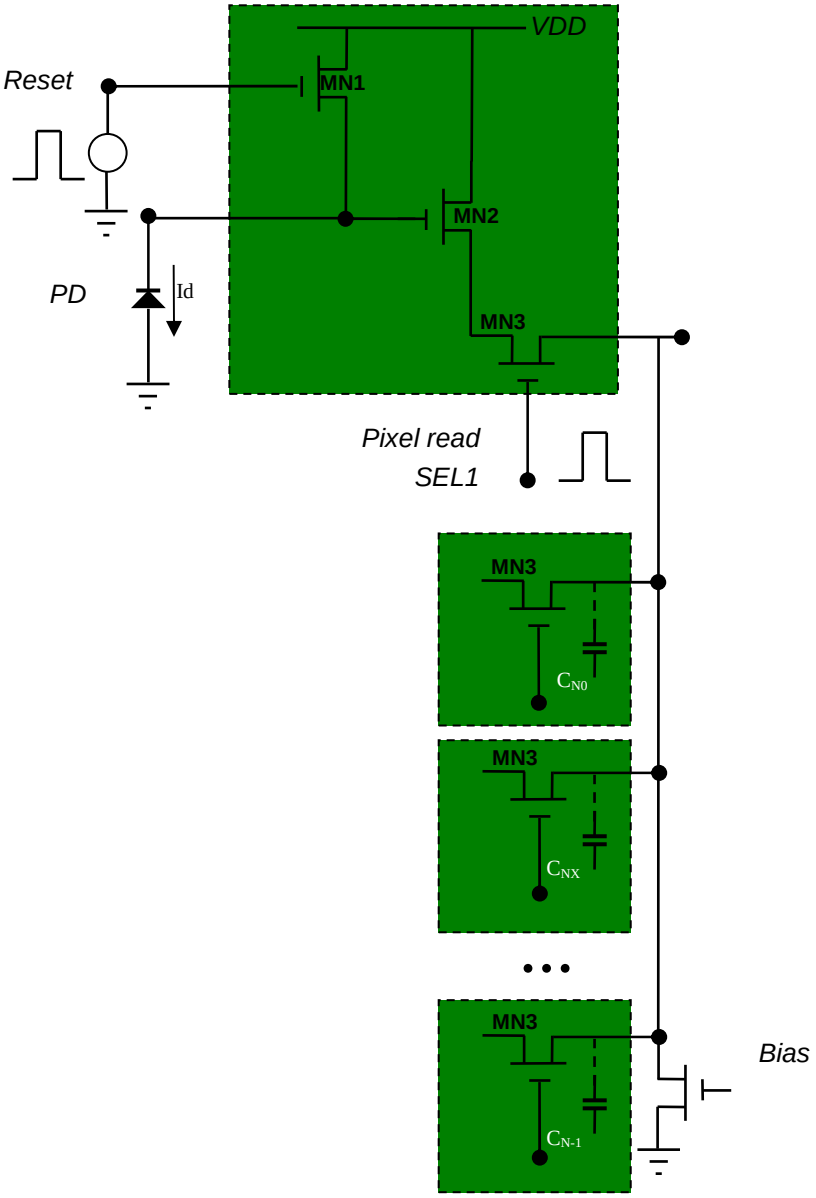


Figure 2. 14. Pixel column structure and parasitic capacitance

Each pixel located on the same column will contribute a MOSFET source capacitance to the column bus, the equivalent capacitance load can be expressed by:

$$C_{eq} = (M-1) \cdot C_{off} \qquad [2.\ 5]$$

Where, the C_{eq} is the total parasitic capacitance from neighboring OFF pixels (whose *select* transistor is connected with ground) in the same column, M represents the matrix

row numbers, and C_{off} stands for the parasitic capacitance in MOSFET source region when it is switched off in each pixel. For getting the C_{off}, a series of simulations are performed. In the first simulation, only the active pixel is taken into simulation, in the second and following simulation, one off pixel and more off pixels is regularly added in simulation as shown in Figure 2. 15.

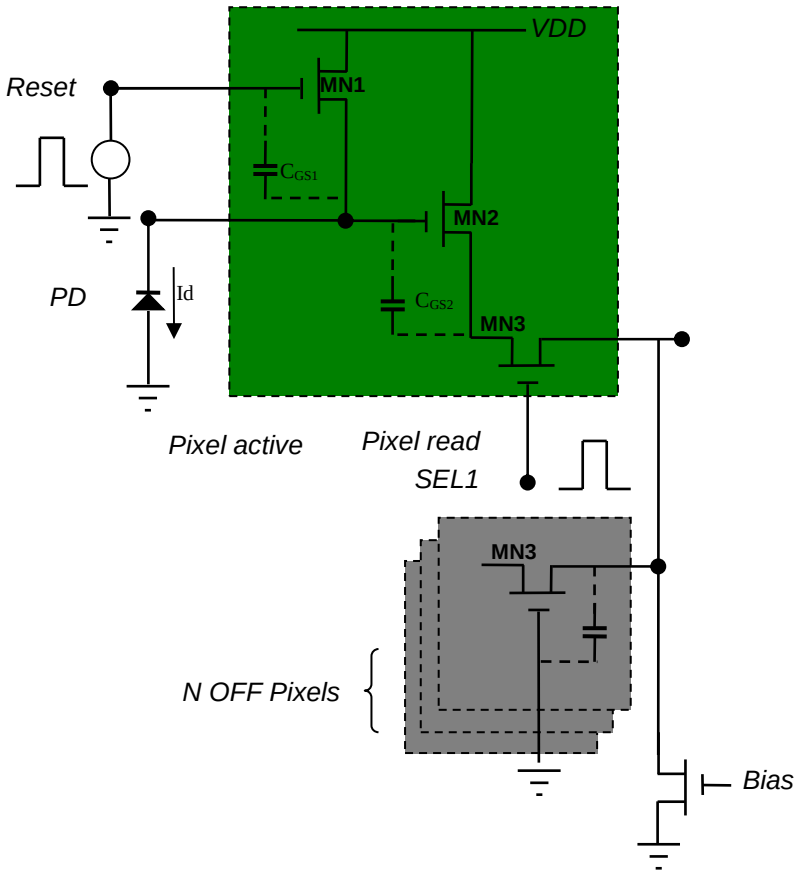


Figure 2. 15. Active pixel with off pixels

For example, if N=100, there will be totally 101 simulations, in the fourth simulation, there are one active pixel and three off pixels in the netlist. Thus, we can get data table containing 101 column capacitances (such as, C1, C2… C101) corresponding to 101 simulations, by solving these equations, the average C_{off} and C_{active} are obtained.

$C1 = C_{active}$

$C2 = C_{active}+C_{off}$

$C3 = C_{active}+2*C_{off}$

$\ldots = \ldots$

$CN+1 = C_{active}+N*C_{off}$

Figure 2. 16. Column capacitance data table

For including the column parasitic capacitance into simulation, an equivalent capacitance is added into the simulation netlist. The final equivalent circuit of including column parasitic capacitance is shown in Figure 2. 17, the Ceq represents all the capacitance of the neighboring off pixels.

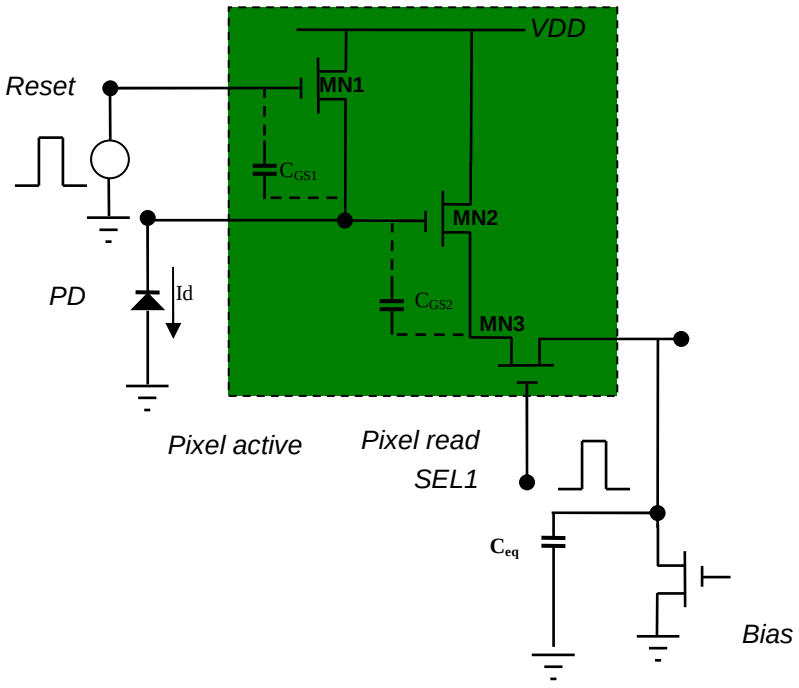


Figure 2. 17. The schematic including equivalent column parasitic capacitance

2.2.4.3 All extracted parasitic capacitance

Apart from the parasitic capacitance from the MOSFET output node, the overlap and routing capacitance of metal layers will also affect the column load as indicated in the Figure 2. 18.

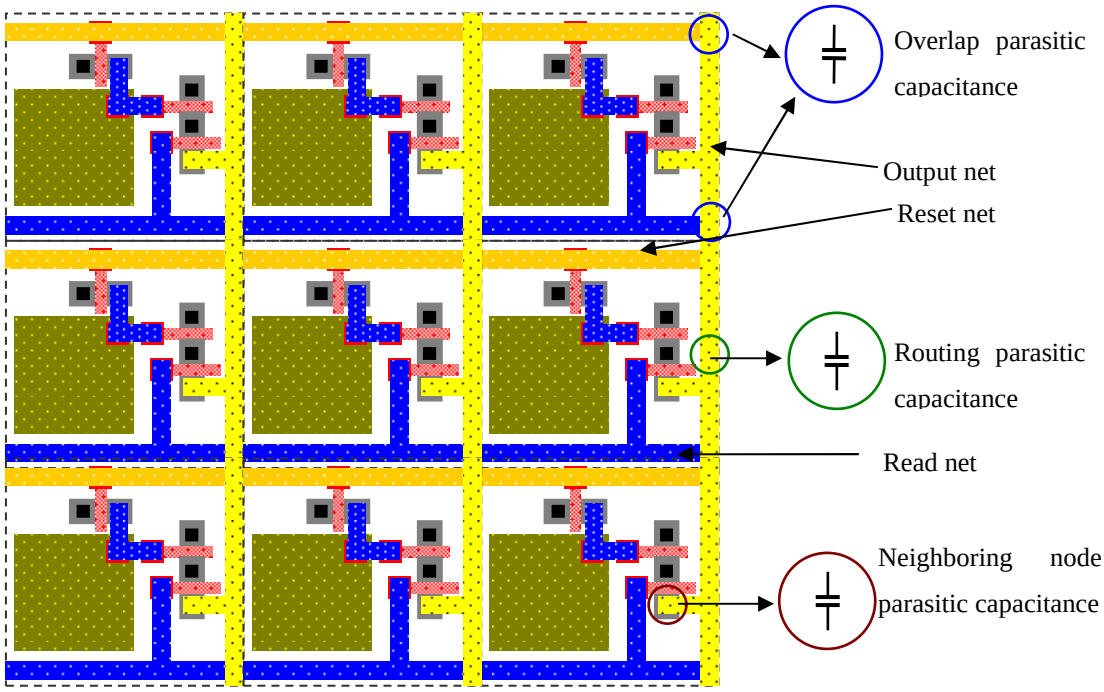
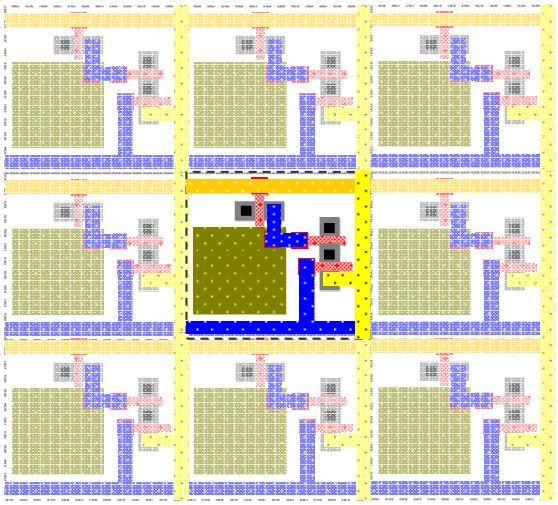
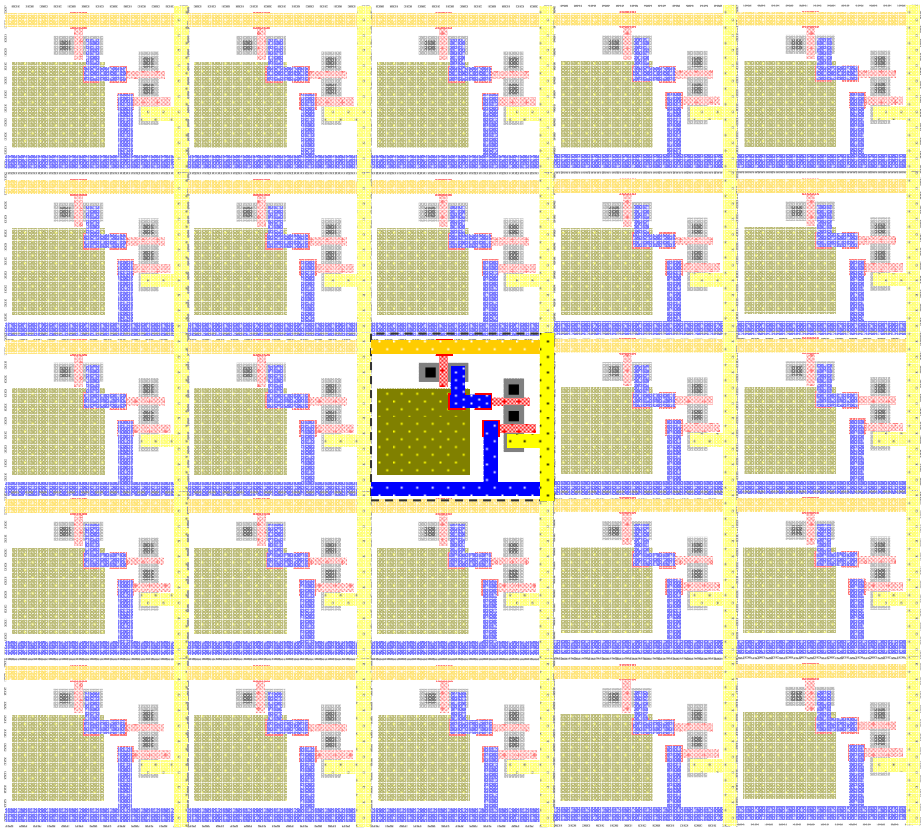


Figure 2. 18. The pixel matrix layout and parasitic capacitance

For getting accurately the parasitic capacitance and impact of the OFF pixels, a special simulation structure is configured as shown in Figure 2. 19, the bright pixel stands for the active pixel and blurry pixels are the OFF pixels. The active pixel locates at the center of pixel matrix and it is surrounded by 8 or 24 OFF pixels, which is able to make sure all the parasitic capacitance and impacts can be included. The output line capacitance is extracted from the matrix 3x3 and matrix 5x5, and the output capacitance of OFF pixel in the middle column is obtained by the same method as equivalent capacitance extraction. The parasitic capacitance on the *reset* line and *read* line is extracted by this structure as well, see the middle row.



Matrix 3x3 (1 active pixel, 8 off pixels)



Matrix 5x5 (1 active pixel, 24 off pixels)

Figure 2. 19. Simulation structure for extracting layout parasitic capacitances

These capacitances are added as the term of a capacitor to the netlist when performing an equivalent post layout matrix simulation as shown in Figure 2. 20. The total capacitance of OFF pixel on the output column can be given by:

$$C_{ex} = (M-1) \cdot C_{offlayout} \qquad [2.\ 6]$$

Where, C_{ex} represents the total parasitic capacitance seen from the column bus, $C_{offlayout}$ is the parasitic capacitance caused by routing and overlap of layers in each pixel.

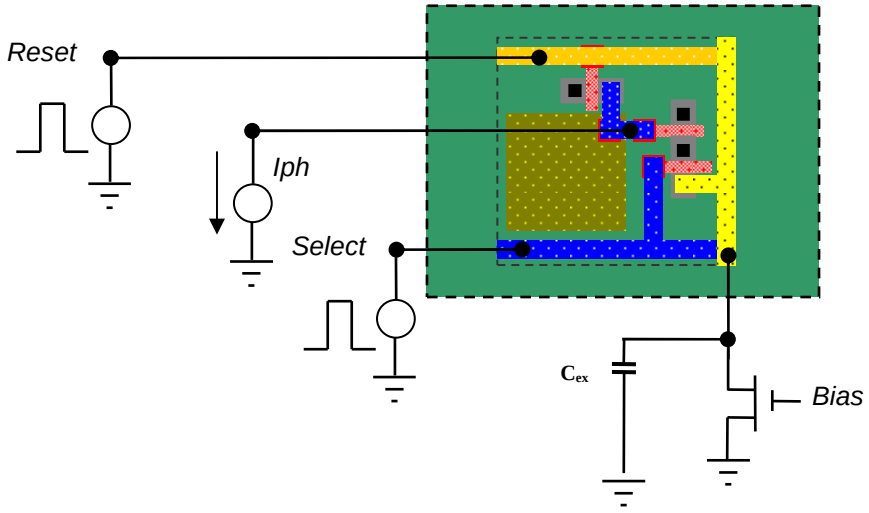


Figure 2. 20. The equivalent schematic of matrix post layout simulation

2.2.5 Look-Up Table (LUT) approach

The main idea of the LUT approach in fast simulation methodology is to build a bridge between stimulus input and output results. The stimulus input table is sampled to cover the full range of input intensity and the output results table will cover all the possible output voltages. The length of these two tables is determined by the output requirement, for example, for a 8 bit gray level output image, there are 256 (=2^8) gray levels and it requires 256 levels of output voltage, thus the input table should cover 256

different intensity levels. For a 10 bits output image, the required table should contain 1024 (=2^{10}) elements. As shown in Figure 2. 21, the pixel output voltage V1, V2, V3, V4 can be represented by the gray intensity value in the final output images.

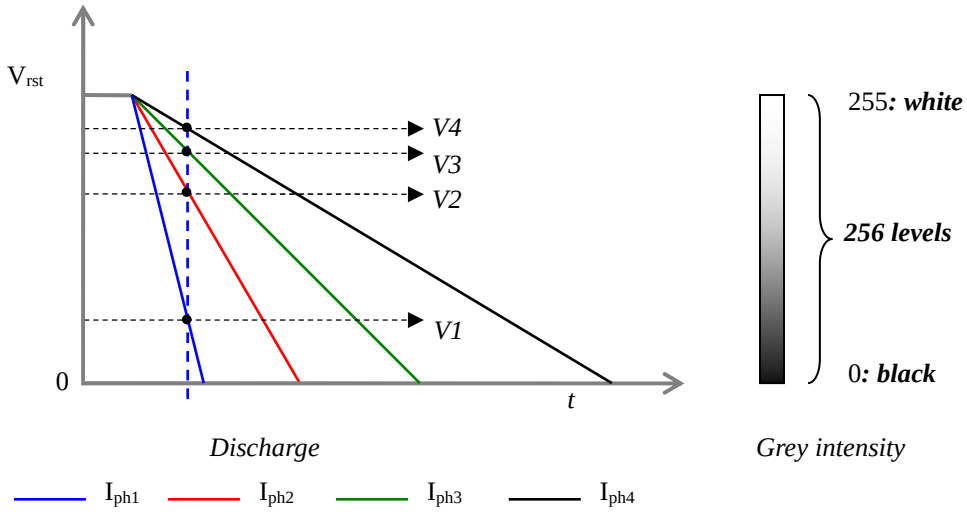


Figure 2. 21. Pixel response represented by grey levels.

With the help of these two tables, we can get the output value directly without simulating all of the input values one by one. It just needs to judge input value by looking through the input table and find the coordinate in the table, and then the corresponding simulation result can be estimated directly. In the case of 8 bit image, the whole input light intensity range is divided averagely into 256 blocks and the *interval* can be given by the equation:

$$\text{interval} = \frac{P_{\max} - P_{\min}}{256} \qquad [2.\ 10]$$

Where: P_{max} and P_{min} is the maximum and minimum of the injecting light intensity (photocurrent). As shown in Figure 2. 22, there are many input values in Block 10 as indicated by the black points between Iph x and Iph y, for reducing the simulation time, all of input values in the Block 10 will be collected as the same input set, and this set is represented by its average photocurrent value which is equal to (Iph x + Iph y)/2. Following this procedure, all of the photocurrent in these 256 blocks can be sampled

into a table which contains 256 photocurrent elements named Iph B_1, Iph B_2, …, Iph B_256.

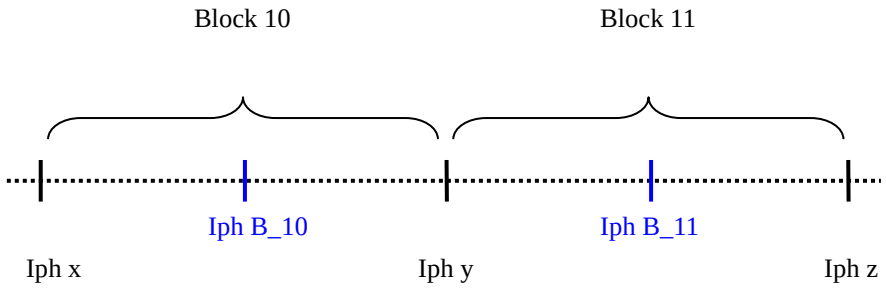


Figure 2. 22. The input photocurrent sampling

For creating the output voltage table, 256 times pixel transient simulation are performed with the photocurrent values stored in the stimulus input table (Iph B_1---Iph B_256). Then a correlated output voltage table is established with the voltage elements named V1, V2, …, V256. The principle of LUT generation is shown in Figure 2. 23.

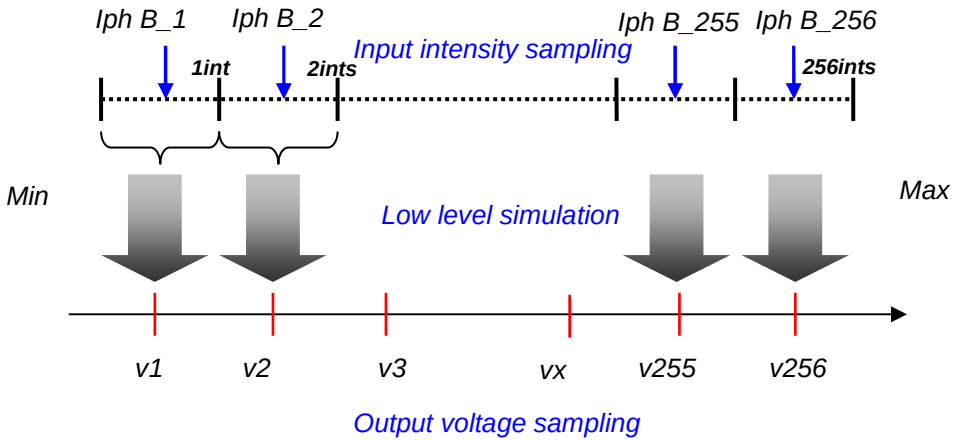


Figure 2. 23. The LUT table generation method

For completing the fast simulation, a mapping function is integrated in the module *judgment* for predicting the simulation results. The photocurrent stored in the photocurrent matrix I[m, n] will be sent to the module *judgment* one by one, and the module *judgment* will calculate its coordinate in the table T_Iph, then the correlated

output voltage in table T_V will be selected and passed to the Vout matrix V[m, n]. The mapping function can be logically expressed as the following codes:

if photocurrent Iph ∈ *Block*(1)

then output voltage = V1

For example, when sending photocurrent I[2, 1] to the module *judgment*, its coordinate in the table T_Iph is 3 after calculating, so the output voltage in Vout matrix V[2, 1] is equal to V3, the whole data flow is indicated by the dash line in the Figure 2. 24.

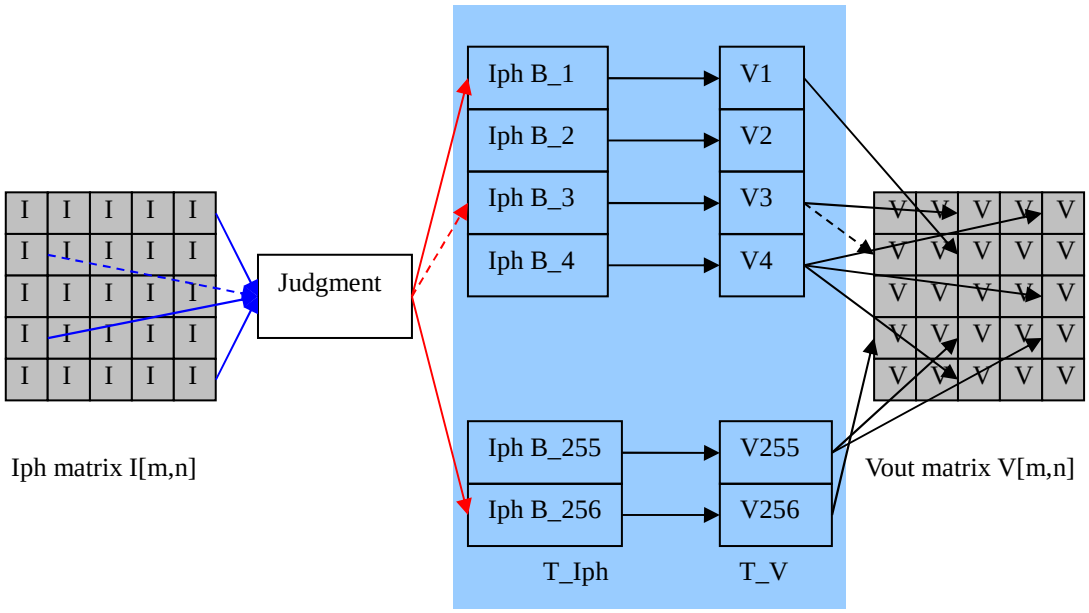


Figure 2. 24. The mapping function in LUT approach

The time for generating the LUT table is the main part of time consumption, and the two dimensional *loop* operation for mapping all the input to the output does not cost too much time, normally the mapping can be finished in seconds.

In classical method, the number of SPICE simulation depends on the matrix size (pixel numbers), and in fast simulation approach, the number of SPICE simulation is reduced largely down to 256 even if the matrix size is very big, such as 1600x1200.

2.2.6 Pixel output matrix and image generation

The pixel output voltage is transferred to the amplifier and analog-to-digital converter for digitalizing, the ADC output digital number (DN) is processed by the image processor integrated with color interpolation and compression method to form the final images. For virtually observing the pixel output voltage and studying the impacts from the circuit low level design parameters on the sensor matrix electrical performance, three image generation methods which are referred to *relative*, *raw* and *absolute* are used in the simulation, as illustrated in the Figure 2. 25.

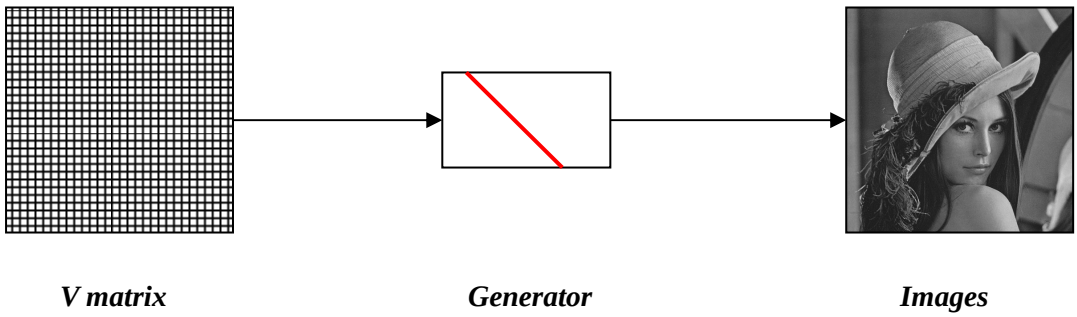


Figure 2. 25. The dataflow of output and response

$$grey\_raw = 255 \times \frac{V_{os}}{V_{DD}} \quad [2.7]$$

The raw method is for viewing the pixel output voltage versus system power supply, the power supply voltage VDD is set as the reference voltage which stands for maximal digital code (255 in 8-bit resolution). As shown in equation [2.7], the pixel original output voltage is reserved in the final grey values. There is no any amplification and extension in the image processing.

$$grey\_abs = 255 \times \frac{V_{os}}{V_{rst}} \quad [2.8]$$

Absolute coding uses the pixel output at reset stage (V_{rst}) as the reference voltage. The pixel output grey value is potentially greater than the raw coding method. This

reflects the real optical signal amplitude. Equation [2. 8] gives the equivalent calculation as the pixel output voltage is processed by CDS circuit.

By finding maximal and minimal CDS output voltages ($V_{o\text{-}max}$ and $V_{o\text{-}min}$) in the pixel output voltage matrix, and setting them to maximal and minimal codes, equation [2. 9] gives the equivalent calculation in relative coding. It is used by an imager signal processor for optimizing image dynamic range and image enhancement.

$$grey\_relative = 255 \times \frac{V_{o-\max} - V_{os}}{V_{o-\max} - V_{o-\min}} \qquad [2.\ 9]$$

Note: the V_{os} is referred to the CDS output voltage, $V_{o\text{-}max}$ and $V_{o\text{-}min}$ is the maximum and minimum of V_{os}. The Raw and Absolute method allow analyzing result at signal level.

2.2.7 CMOS Image sensor matrix response variability

In CMOS image sensor, the small variation σv_{th} in reset transistor M1, source follower M3 and column current source M4 will lead to the output swing changes among pixels, the variation of charge mobility $\sigma\mu$ will affect the transistor voltage current characteristic and then cause source follower gain variation, which also make contrition to the pixel level mismatch and performance nonuniformity. Additionally, the gate oxide thickness variation σT_{OX} causes the transistor gate capacitance variation, such as gate capacitance variation of the source follower M3. At the point of view of the matrix level, the variability included response matrix can be expressed as:

$$v_{oi,j} = TF_{i,j} \times Iph_{i,j} \qquad [2.\ 11]$$

Where, the $v_{oi,j}$ is the response of pixel located at the cross of row *i* and column *j* on the matrix, $TF_{i,j}$ is the correlated transfer function which reflects the pixel characteristic, and $Iph_{i,j}$ stands for its photocurrent. If we fix the $Iph_{i,j}$ and let $Iph_{i,j} = I$, the pixel response is dependent on pixel transfer function. So if v_o is the nominal value of pixel output voltage and all the pixel output voltages are stated as $v_{oi,j}$ for $1 \leq i \leq M$ and $1 \leq j \leq M$, then the total noise is the set of values:

$$v = \sum_{i=1}^{M}\sum_{j=1}^{M}(v_{oi,j} - v_o) \qquad [2.\ 12]$$

For obtaining the pixel output matrix $v_{oi,j}$ and nominal output voltage v_o, a Monte Carlo method based simulation methodology is explored. As shown in the Figure 2. 26, A, B, C represents 3 physical parameters, if the Monte Carlo simulation is set to perform m1 times, there are m1 random variations of each parameter, such as A_{11} to A_{m1}, B_{11} to B_{m1}, thus there are m1 combinations of these three parameters, such as A_{11}, B_{11}, C_{11}. Normally the parameter variation of A, B, C follows some distribution, such as gauss distribution, and the set of A_{11} to A_{m1} is generated following this distribution. Each combination is sent to the simulator to perform a transient simulation, and the output is sampled as a set of Response, such as R_1 to R_m.

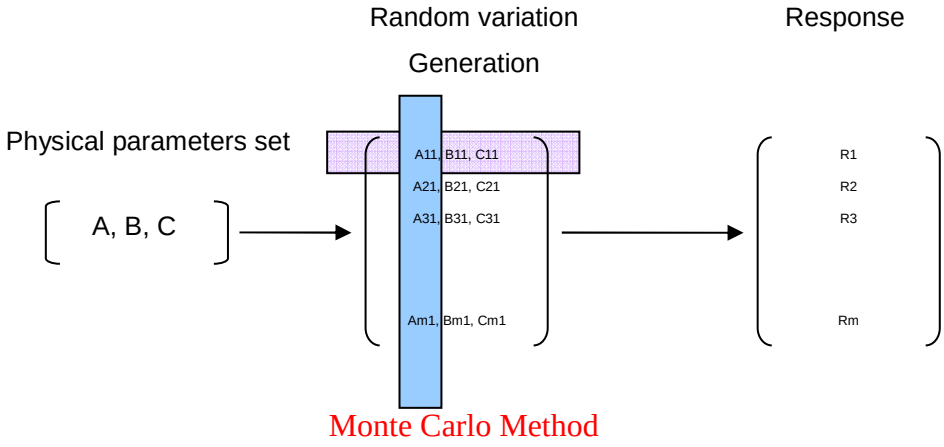


Figure 2. 26. Monte Carlo random combination generation

The numbers of run is a potential limitation of Monte Carlo simulation, because the m1 determine directly the simulation time consumption. If the m1 is bigger than 100 Mega, then this Monte Carlo simulation method will meet trouble because it will cost too long time. So a compatible simulation methodology is explored which can perform classical Monte Carlo simulation and fast simulation as shown in Figure 2. 27, the classical Monte Carlo simulation goes directly from “pixel design” to “results” following the black arrow. The fast simulation is performed following the blue arrow, and by applying an “estimator” in the data flow, the numbers of run in Monte Carlo

simulation is reduced. The difference of classical Monte Carlo simulation and fast simulation is how to use the response R, in classical Monte Carlo simulation the set R is directly the output result, and in fast simulation method it is a data base which is used by "estimator" to extract the response statistic information. The classical Monte Carlo simulation and fast simulation method is switched by a threshold value 1000. The fast simulation method is triggered and adopted when the pixel numbers exceeds 1000.

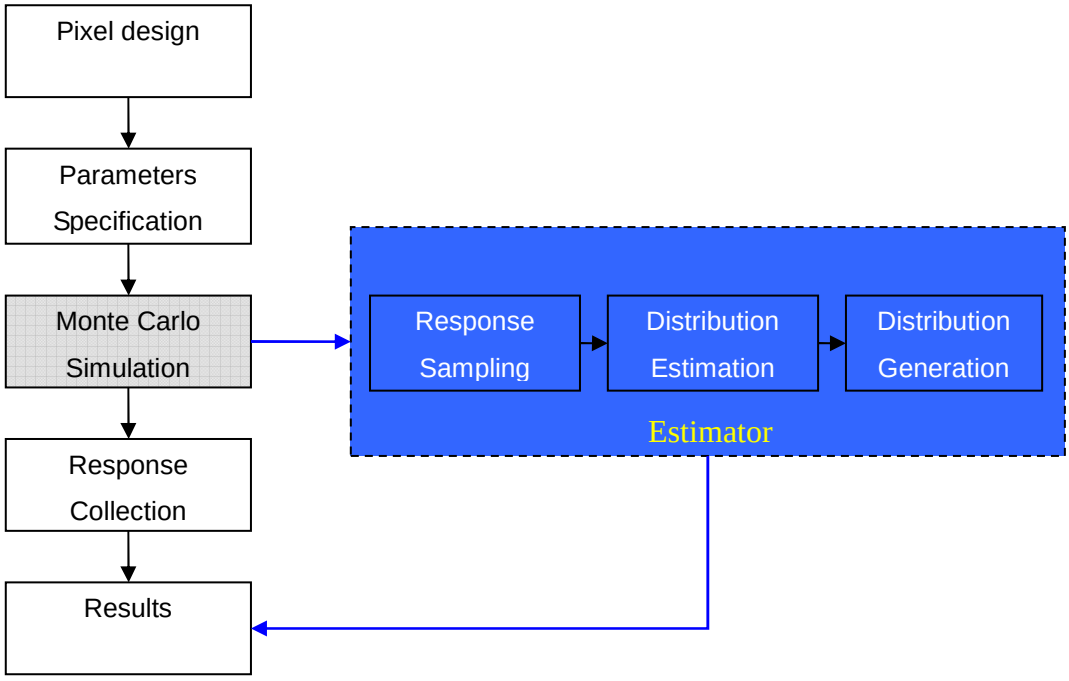


Figure 2. 27. The data flow of studying sensor matrix response variability

2.2.7.1 Classical Monte Carlo simulation in studying CMOS imager response variability

For a sensor matrix containing M x M pixels, there are M^2 responses corresponding to the sensor stimulus (M^2), and the Monte Carlo simulation is performed M^2 times to get the response matrix v[M, M]. As shown in the Figure 2. 28, in a 2 parameters classical Monte Carlo simulation, a random parameter set containing M^2 combinations is firstly

generated, and each combination will be send to the simulator to perform the classical transient simulation.

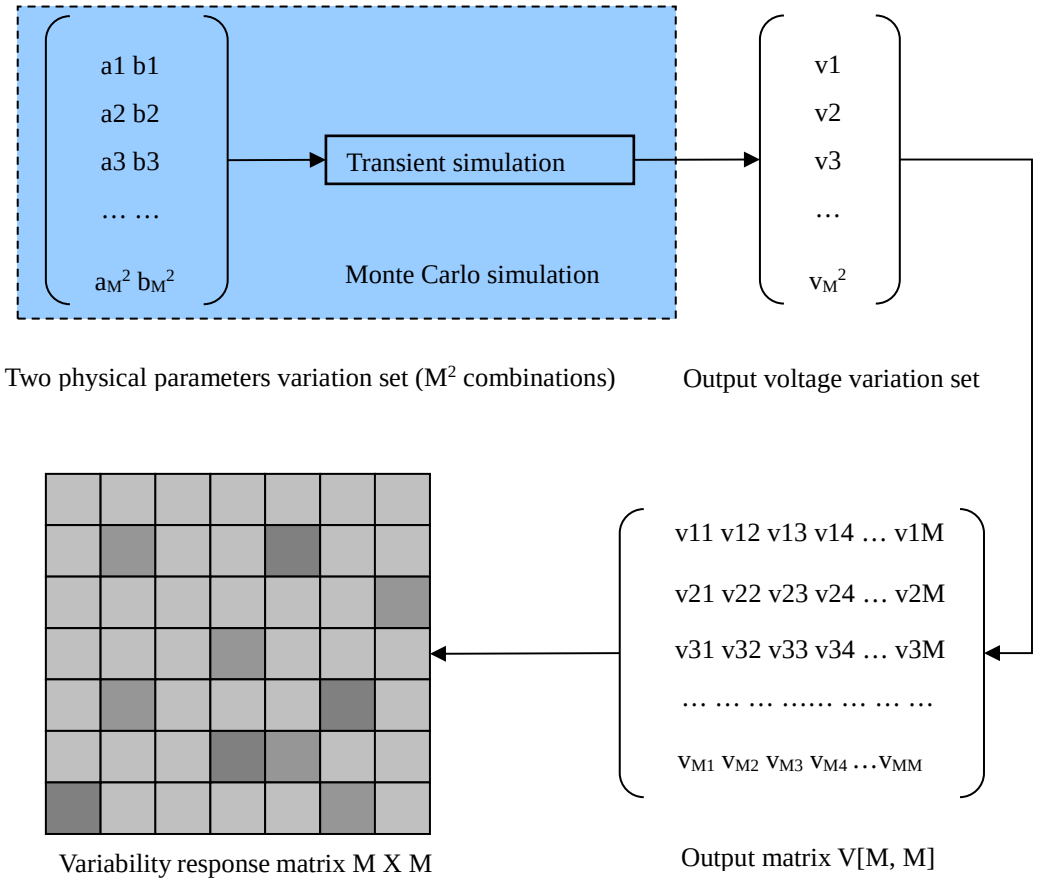


Figure 2. 28. Image sensor matrix variability analysis

After Monte Carlo simulation, a set of pixel output voltage is sampled and is processed into a voltage matrix v[M, M]. The v[M, M] is virtually represented by an gray image to state the response variability caused by the variation of physical parameters, such as charge mobility μ and thickness of oxide layer t_{ox}.

2.2.7.2 Fast simulation method in studying CMOS imager response variability

As stated in the section 2.2.5.1, the numbers of Monte Carlo run are equal to pixel numbers in classical method. For example, if the matrix contains 3000x5000 (= 15 Mega) pixels, the simulator will run 15 Mega times, and this simulation will cost a very long time. For solving this problem, a distribution estimator is added. As shown in Figure 2. 29, a set of parameter combinations is used to generate a sampled response set v[x] through L^2 times of Monte Carlo simulation, L is normally smaller than M. The Monte Carlo simulation result is processed and the statistic is extracted, such as the mean value μ and standard deviation value σ.

$$\mu = \overline{v} = \frac{1}{L^2} \cdot \sum_{i=1}^{L^2} v_i \qquad [2.\ 13]$$

$$\sigma^2 = \frac{1}{L^2} \cdot \sum_{i=1}^{L^2} (v_i - \overline{v})^2 \qquad [2.\ 14]$$

Where, v_i is the output voltage of each run, and L^2 is the number of simulation. $\overline{v}$ is the average value of the v[x].

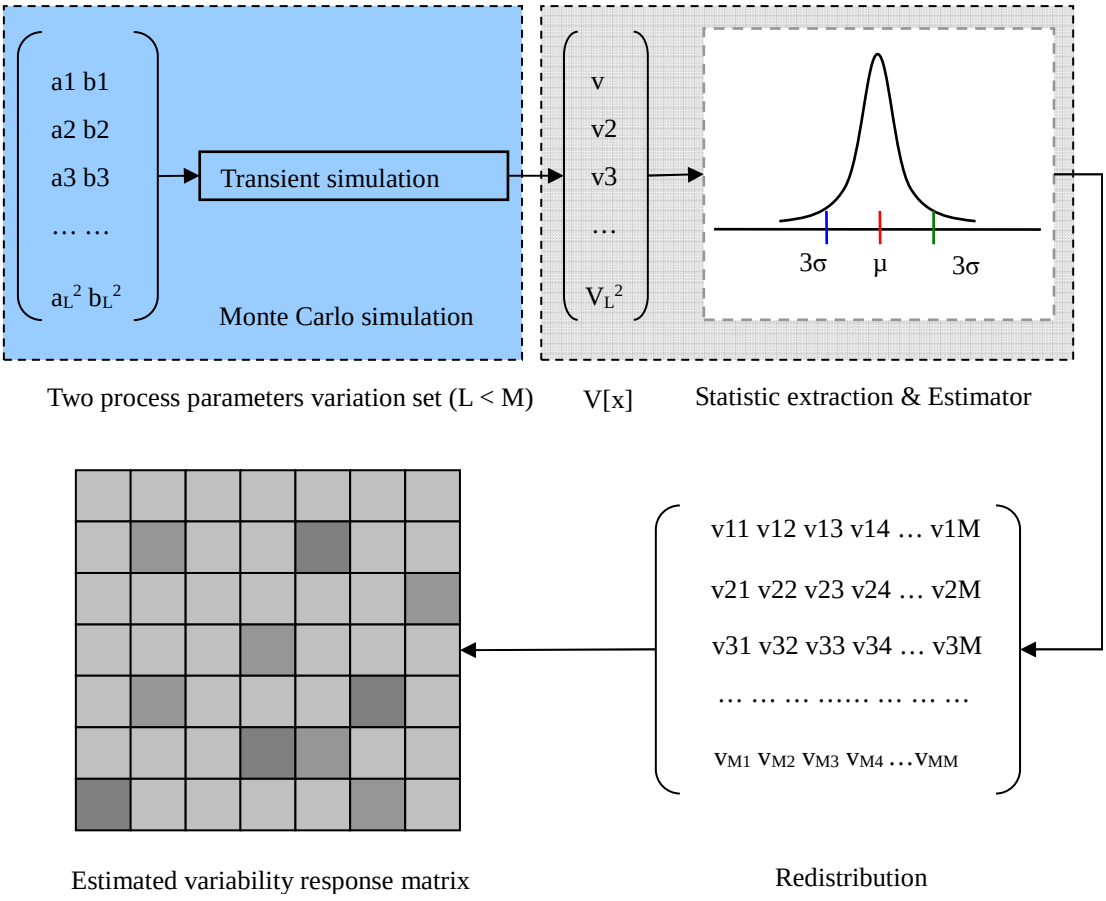


Figure 2. 29. The Fast Variability aware methodology

The response matrix estimation is carried out after obtaining the μ and σ. In the Fast simulation methodology, the Box-Muller method is adopted to generate the random number which follows the standard normal distribution *N (0, 1)*.

$$u, v \sim U(0,1) \quad [2.15]$$

$$z = \sqrt{-2\log u} \cdot \cos(2\pi \cdot v) \sim N(0,1) \quad [2.16]$$

$$\mu \cdot z + \sigma \sim N(\mu, \sigma) \quad [2.17]$$

Following the equation [2.15-2.17], an identically distributed response voltage matrix can be randomly generated by applying (μ, σ). The voltage in the matrix v[M, M] follows the same distribution of the voltage in data base v[x]. Then the estimated response

voltage matrix is represented by an image to view virtually the response variability. This help to study and represent salt and pepper like noise.

2.3 Fast simulation GUI

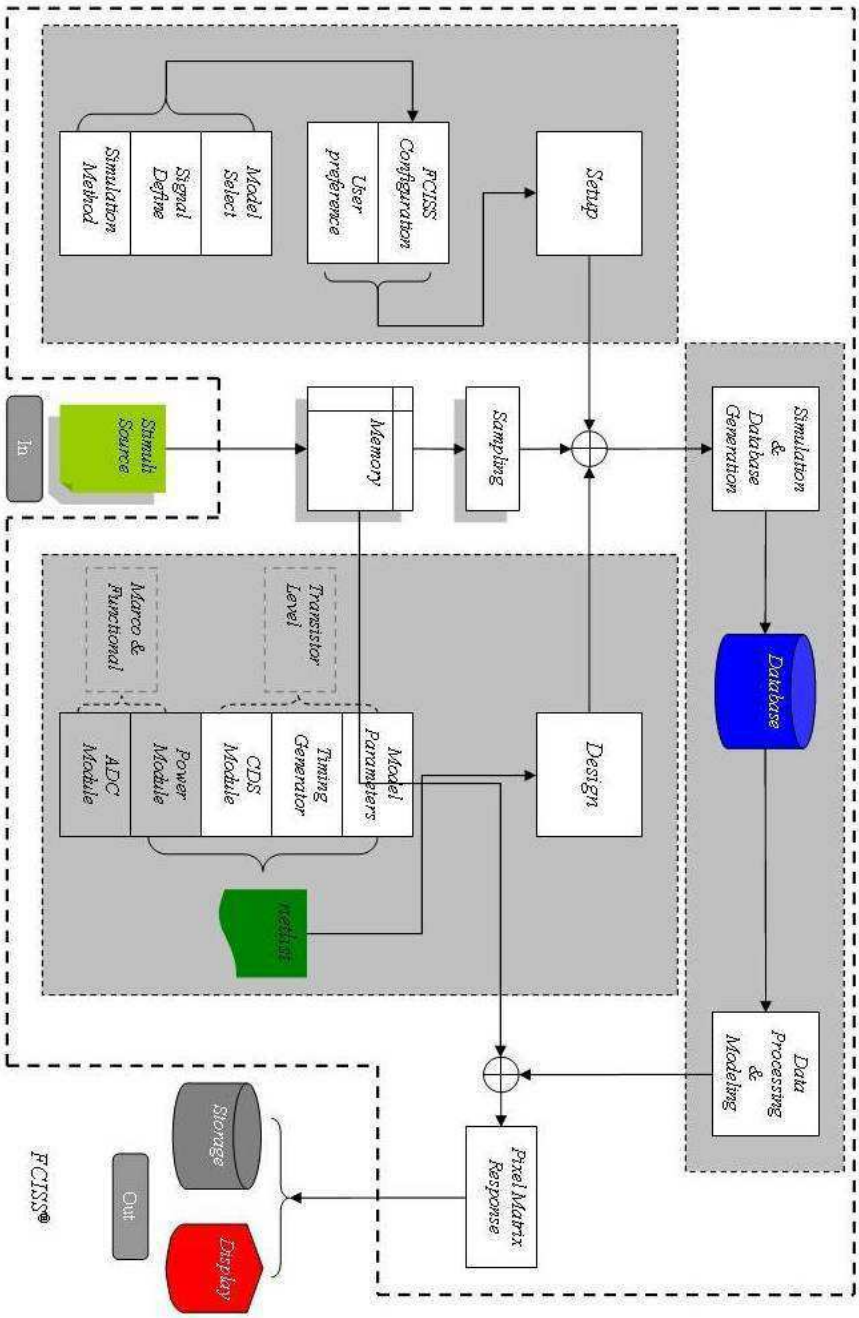


Figure 2. 30. The data flow of fast simulation

The dataflow of fast simulation is shown in Figure 2. 30. For facilitating the application of the fast simulation methodology, a GUI composed of user menus, stimuli input and generation, simulation specification, results generation and display interface is developed as shown in Figure 2. 31. There are 3 main parts containing "*input*", "*simulation*" and "*output*".

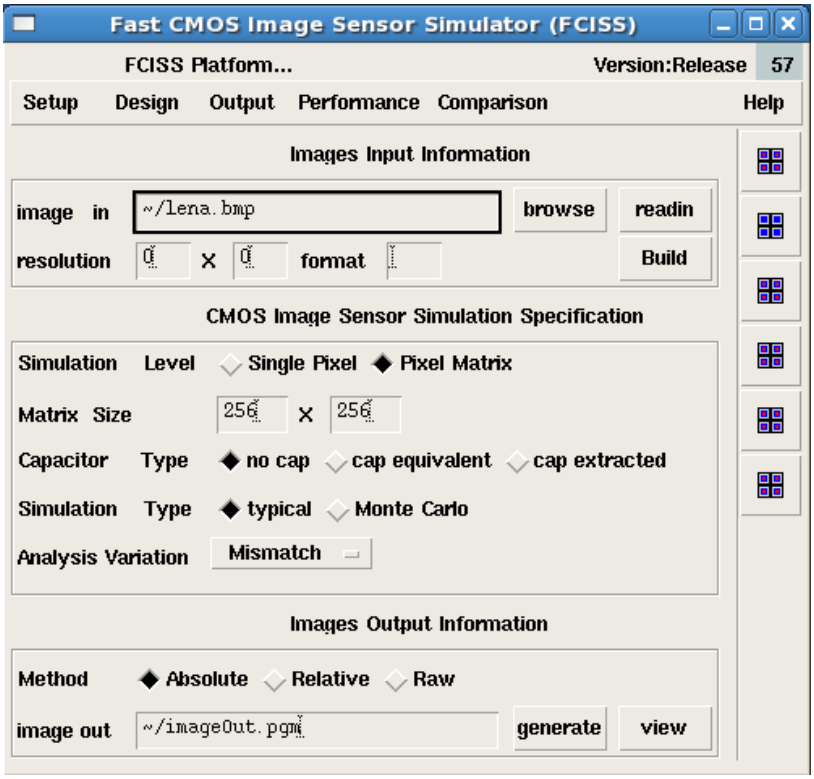


Figure 2. 31. Fast simulation methodology GUI

2.3.1 Fast simulation main framework

The Fast simulation main framework can be divided into three parts, as "images input", "CMOS image sensor simulation" and "images output".

2.3.1.1 Image input information

As shown in Figure 2. 31, the *"image in"* field indicates the path of input image. By typing in the absolute path of a local image, or by using "*browse*" button to locate an image on the local hard disk. The *"readin"* button can load a *skill* function to judge the image format and pick out the image pixel values, and all the image pixel values will be stored temporarily as a *skill* variable matrix. The image information, such as format and resolution will be shown in the "*resolution"* field after image has been completely read in.

2.3.1.2 CMOS image sensor simulation specification

In this frame, the pixel level simulation or matrix level simulation can be specified through triggering the "*simulation level*" option. The field "*matrix size*" is used to specify the real matrix size which you want to simulated, the default value is set equal to the input image resolution, this "*matrix size*" will affect the column capacitance in pixel classical simulation. There are three options of parasitic with extracted capacitance, such as "no cap", "cap equivalent" and "cap extracted". No parasitic capacitance will be included in the simulation when the "no cap" option is activated, the parasitic capacitance from the neighboring pixels will be taken into simulation if the "cap equivalent" is specified. With triggering the "cap extracted", all the parasitic capacitance related to the pixel layout will be taken into the simulation.

There are two choices of the simulation type, one is typical simulation and the other is Monte Carlo simulation. In the typical simulation, all the parameters in CMOS transistor are set to the typical value. This simulation is applied to estimate the sensor matrix response in ideal case. The Monte Carlo simulation help investigating the sensor matrix response variability versus the CMOS process, this simulation gives a prediction of the sensor performance when considering the process parameters variations. In the Monte Carlo simulation, both the process variation and mismatch variation are available. The process variation analysis is used to study the response variability among the

different chips, while the mismatch variation analysis is used to investigate the response variability among all the pixels on the same chip.

2.3.1.3 Image output information

In the "*image out*" information frame, there are three image generation methods named "absolute", "relative" and "raw". The image generation procedure will adopt different equation for processing the voltage data into digital numbers. The "*view*" button can start the "image viewer" to view visually the simulation results.

2.3.2 User menus

The user setup function provides designers with two possibilities: preference "*setup*" and "*Fast simulation method configuration*". These parameters are necessary for the Fast simulation and post signal processing.

2.3.2.1 Setup

2.3.2.1.1 User preference setup

The parameters "*image viewer*" and "*text viewer*" are used to view the simulation results which are stored in the output archive files. They are set up under the "setup" menu in the user preference form as shown in Figure 2. 32. The "*image viewer*" helps the designer to identify the performance improvement or degradation after modifying the design, such as changing the dimension size of inner source follower, the changes in output can be visually viewed by image viewer.

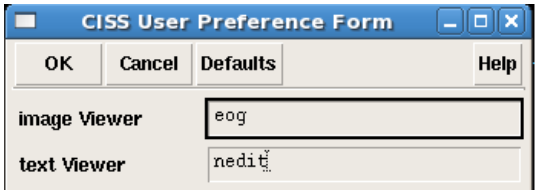


Figure 2. 32. The user preference form

2.3.2.1.2 Fast simulation configuration

For configuring and initialing Fast simulation method, user needs to define some parameters as indicated in the Figure 2. 33.

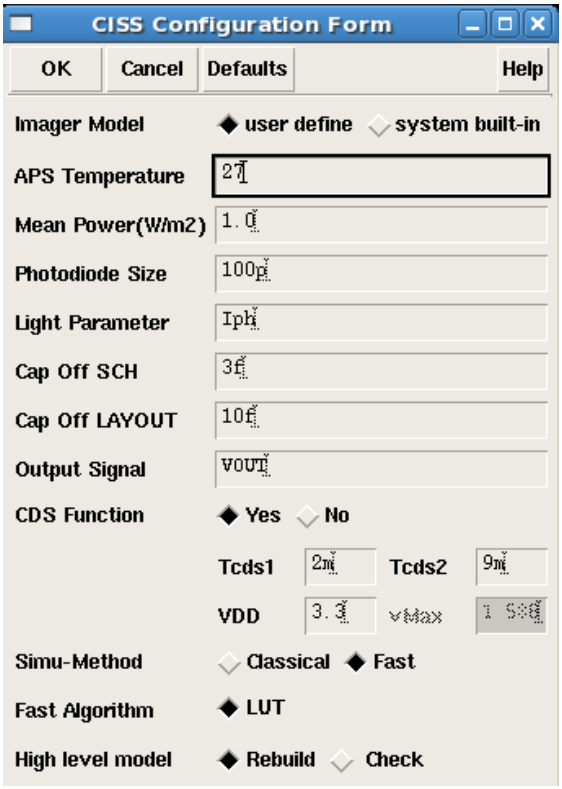


Figure 2. 33. FCISS configuration form

An internal signal set including *light parameter, pixel output signal* is specified for collecting and extracting the low level data from the *SPICE* simulator. The *light* parameter and mean power will be transferred to the photocurrent converter for calculating the equivalent photocurrent, the *reset* signal, *select* signal and *output* signal are used as the interconnection line on the pixel matrix, the parasitic effect along these lines will be extracted by the low level *SPICE* simulation, such as the output column parasitic capacitance which is a key factor affecting the pixel response and signal read out time. The CDS function enables apply correlated double sampling technique in the signal read out processing. Tcds1 and Tcds2 point out the exact time when the output signal is sampled. The VDD and vMax is used as the reference voltage for generating the

final images. The whole simulation approach includes two simulation methods and levels: Classical SPICE simulation and Fast simulation. User can switch the simulation method by trigger this option. The high level mapping model can be rebuilt or re-used in the next simulation via configuring properly in the setup form.

2.3.2.2 Design

Under this menu, user can specify the ADC parameters, such as “gain” and “resolution”. In this thesis, the “gain” is set to “1” and the resolution is set to 8 bits as shown in Figure 2. 34. The ADC resolution parameter will affect the number of low level simulation in LUT approach, for example, if the ADC is set to 10 bits, the classical low level simulation will be performed 1024 (2^{10}) times. This module is potentially integrated to emulate the ADC converter behavior, and this macro model can be enriched by adding the other parameters.

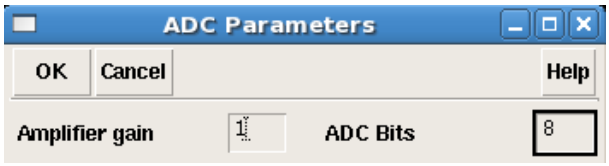


Figure 2. 34. The ADC parameters

2.3.2.3 Output

The output data format can be specified under this menu, two options are available as “scalar data” and “curve”. The sampling data points can be saved in a scalar file or the sampling data points can be plotted as a curve.

2.3.2.4 Comparison

For evaluating the FCISS accuracy performance, the comparison tool which can extract and compare images in pixel value level has been investigated. It is potentially

used to compare the results from classical simulation and fast simulation. As indicated in Figure 2. 35, the maximum grey level error in pixel and the average error on the whole matrix can be calculated.

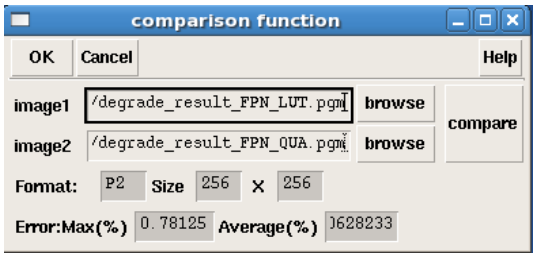


Figure 2. 35. the interface of results comparison method

The comparison method can be given as:

$$Error_{\max} = Max\frac{P^{1}_{i,j} - P^{2}_{i,j}}{P^{2}_{i,j}} \qquad [2.\ 18]$$

$$Error_{average} = \frac{\sum(P^{1}_{i,j} - P^{2}_{i,j})}{M \cdot N} \qquad [2.\ 19]$$

Where, $P^{1}_{i,j}$ and $P^{2}_{i,j}$ presents the pixel grey level located in the row *i* and column *j* in the image *1* and image *2*, respectively. The total number of pixels is equal to *M* x *N*. The max error is used to investigate the simulation accuracy when considering the pixel response as a function of its coordinate on the matrix. The overall average error is dedicated to study the pixel matrix simulation accuracy, especially for investigating the pixel matrix performance when taking CMOS process variation into account.

Conclusion

Fast Scalable simulation methodology is fully implemented in *SKILL* language. It co-works with *Spectre* circuit simulator under Cadence Analog Design Environment (ADE). It provides the following functionalities:

- Help understanding CMOS image sensor characteristics.

  -- The designer can model the CMOS image sensor in Cadence ADE, the fast simulation methodology can help understanding the pixel matrix corresponding

to the current design, for instance, how does the pixel model affect the final image quality.

- Accelerate the CMOS image sensor matrix simulation.

  -- The CMOS image sensor matrix is composed of millions of pixel cells, and this makes the whole pixel matrix simulation quite difficult. The methodology is capable of gaining the high simulation accuracy within reasonable time consumption, and it enables predict the pixel sensor matrix performance in the early stage of the design cycle.

- Help to study sensor response variability.

  -- CMOS image sensor matrix suffers from Photo Response Non-Uniformity (PRNU) which related to the CMOS process variability. The response non uniformity is seen as the variation in the pixel responsivity. It is caused by the non-uniformity of the pixel geometry, pixel doping profile and its location. Besides the optical signal variation due to the lens distortion, the response non-uniformity is caused by the sizing variation and dark current variation among the pixels on the chip as well. The methodology provides a way of estimating pixel response variation caused by transistors and photodiode characteristic variation.

- The fast simulation methodology is an alternative approach in accelerating big circuit simulation, instead of using a high speed computer or high speed simulator, it lower down the system resource requirement. Nowadays, the array-based circuit, such as, CMOS image sensor, memories, brings difficulties to the circuit simulation method, and this new method can be well used to simulate matrix like circuit.

Chapter 3 results on 3T pixel architecture and performance

The well known 3T-APS structure is adopted in this thesis and this chapter is mainly focused on its results of fast simulation methodology. Three kinds of simulation are discussed by taking capacitance into account in this work. In schematic level, the neighboring pixel capacitances are included, and in layout level, all the parasitic capacitances are included in the simulation.

3.1 Nominal response of 3T pixel sensor matrix

As discussed in chapter 2, due to the difficulty of simulating the image sensor matrix mainly caused by the large netlist and large calculation burden to the simulator, the fast scalable simulation methodology is applied to simulate the image sensor matrix, for checking the impacts from different design considerations on the sensor matrix performance in ideal and real case, the sensor matrix typical simulation on schematic level is performed.

3.1.1 Results of sensor matrix with no capacitance on schematic level

The Simulation environment is set up in the Cadence platform with AMS 0.35μm design kit. In image sensor schematic level, all the pixels are represented by the same model. With the assumption that all the single pixel on the matrix have the same characteristic and will not be affected by its neighbours. As shown in the Figure 3. 1, the up-left one is *lean.bmp* (original bmp image with 256 x 256 pixels) and up-right one is the raw output image, the bottom left is a relative result and bottom right is for presenting the absolute result.

The histogram under each picture shows the difference between different image generation methods. For example, in the raw result, the pixel intensity value is restricted between 30 and 120, it means that ratio of the output voltage compared with the power supply is low, and it indicates that almost half (≈120/255) of the voltage swing is lost in output range. The shapes of the four histograms are quite similar, the histogram of raw output is compressed comparing with the original one (input image), and the histogram of absolute output is shifted on right. The relative result looks quite similar with the input image and the range of intensity is extended to cover 0 and 255. The relative result gives a clearer image comparing with the raw output and absolute output.

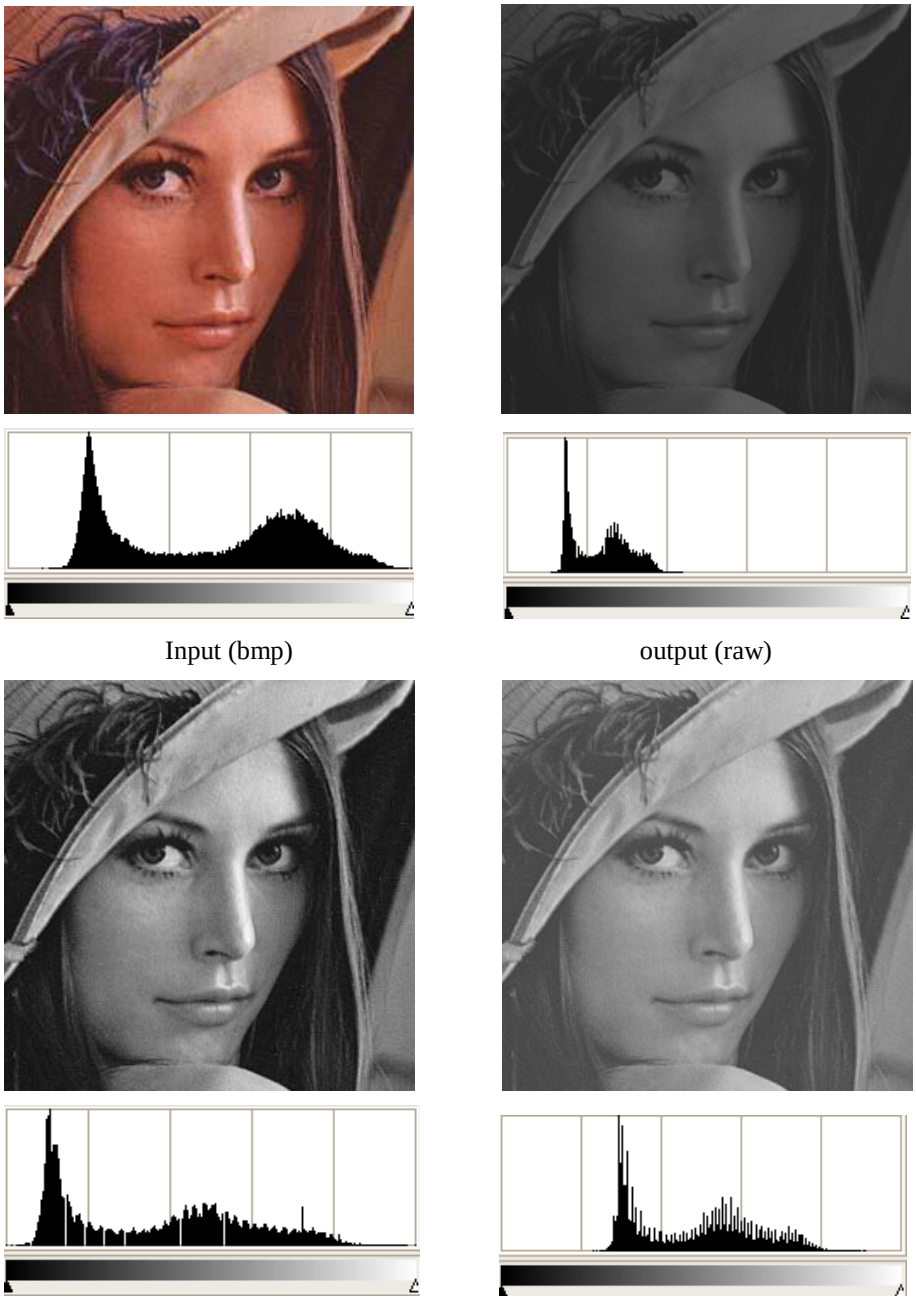


Figure 3. 1. The simulation results of LUT approach (no cap)

In a gray level image, the mean (μ) value presents the average intensity value, it standards for the average lightness of the image. The standard deviation (σ) represents the range of intensity value, it can express the dynamic range of image. Median value

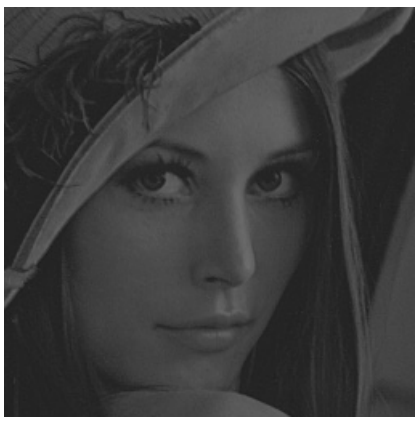
represents the threshold numerical value which separates higher half and lower half of the pixel intensity values. As shown in Table 3. 1, the relative results posses the highest dynamic range which is proved by its σ = 57 whereas σ = 18 and 38 for raw images and absolute result.

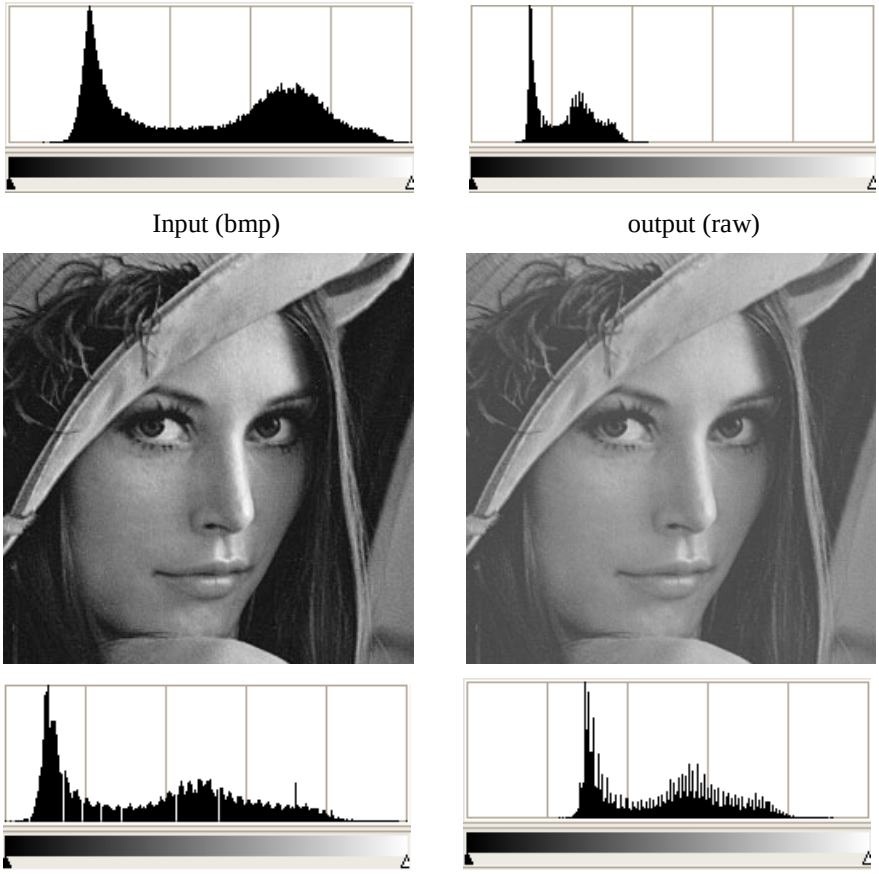
Table 3. 1. The statistical information of LUT approach results (no cap)

images	Mean (μ)	Standard (σ)	median
input	89.4	45.5	92
Raw	58.4	18.5	60
Relative	93.6	57.1	98
Absolute	121.3	38.8	124

3.1.2 Results of sensor matrix with equivalent capacitance on schematic level

Considering the capacitance from the neighboring non-active pixel, the equivalent capacitance is added to the netlist. The final output images in LUT approach are shown in the Figure 3. 2, and the statistical information is indicated in the Table 3. 2. It is observed that the capacitance of neighboring off pixels will not affect the final output images in this matrix size (256x256).





Input (bmp) output (raw)

Output (relative) output (absolute)

Figure 3. 2. The simulation results of LUT approach (cap equivalent)

Table 3. 2. The statistical information of LUT approach results (cap equivalent)

images	Mean (μ)	Standard (σ)	median
input	89.4	45.5	92
Raw	58.4	18.5	60
Relative	93.6	57.1	98
Absolute	121.3	38.8	124

A further comparison is shown in the following Table 3. 3.

Table 3. 3. The comparison of results within and without considering neighboring capacitance

Images		256x256 (μ,σ)	512x512 (μ,σ)	1024x768 (μ,σ)	1600x1200 (μ,σ)
Input		(125.7, 60.5)	(135.1, 57)	(142.9, 52)	(103.2, 56.9)
Raw	No cap	(58.4, 18.5)	(60.9, 17.7)	(70.3, 19.5)	(58.8, 19)
Relative		(93.6, 57.1)	(103.1, 51.4)	(127.2, 54.5)	(101.1, 50.9)
Absolute		(121.3, 38.8)	(126.7, 37.2)	(146.5, 41.2)	(122.2, 40)
Raw	Cap CEQ	(58.4, 18.5)	(60.9, 17.7)	(70.3, 19.5)	(58.8, 19)
Relative		(93.6, 57.1)	(103.1, 51.4)	(127.2, 54.5)	(101.1, 50.9)
Absolute		(121.3, 38.8)	(126.7, 37.2)	(146.5, 41.2)	(122.2, 40)

Note: the results with considering neighboring capacitance are indicated in red color, and the data written in blue color represents the results without considering neighboring capacitance.

Table 3. 4. The voltage comparison between no cap and equivalent cap results in LUT (mV)

Images	256x256	512x512	1024x768	1600x1200
No Cap	802.515	802.515	802.515	802.515
CEQ	802.515	802.514	802.513	802.511

As indicated in the Table 3. 4, the voltage difference caused by neighboring capacitance is within 0.1mv, this voltage will not affect the final output images.

3.1.3 Results of sensor matrix with capacitance extracted from layout

The 3T APS pixel layout is implemented in AMS 0.35um 4 metal layers technology. As shown in Figure 3. 3, for example, the pixels in small pixel matrix 2x2 are identically designed to achieve uniformity response when exposing to the same light intensity. The overlap between different metal layers will induce the parasitic capacitance which degrades the sensor performance, and also these parasitic capacitances will affect the sensor response speed and sensor signal readout time. For instance, the colBus1 and Reset1 has a reset overlap capacitance $C_{reset}1\_1$ in pixel 11 as surrounded by the blue

circle, and has the reset overlap capacitance $C_{reset}2\_1$ with Reset2 in pixel 21. $C_{reset}M\_N$ presents the reset overlap capacitance corresponding to the pixels located in the row M and column N. Meanwhile, the read overlap capacitance caused by the cross of read line and column bus will increase the column bus load capacitance too, these capacitances have the same distribution as the reset overlap capacitance in the whole matrix, $C_{read}M\_N$ represents read overlap capacitance located at the cross of row M and column N on the matrix. These two kinds of parasitic capacitance cause the increasing of column load capacitance.

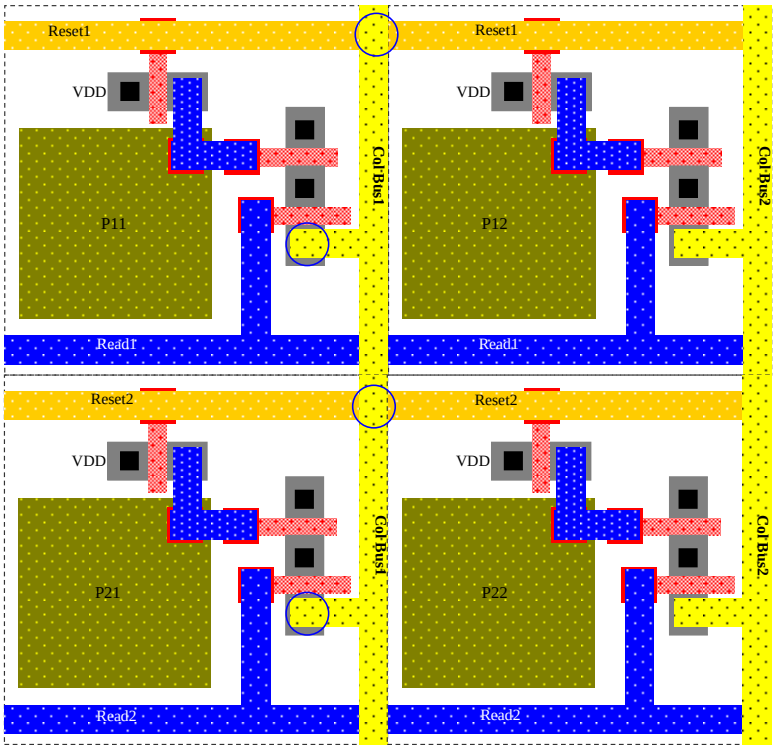
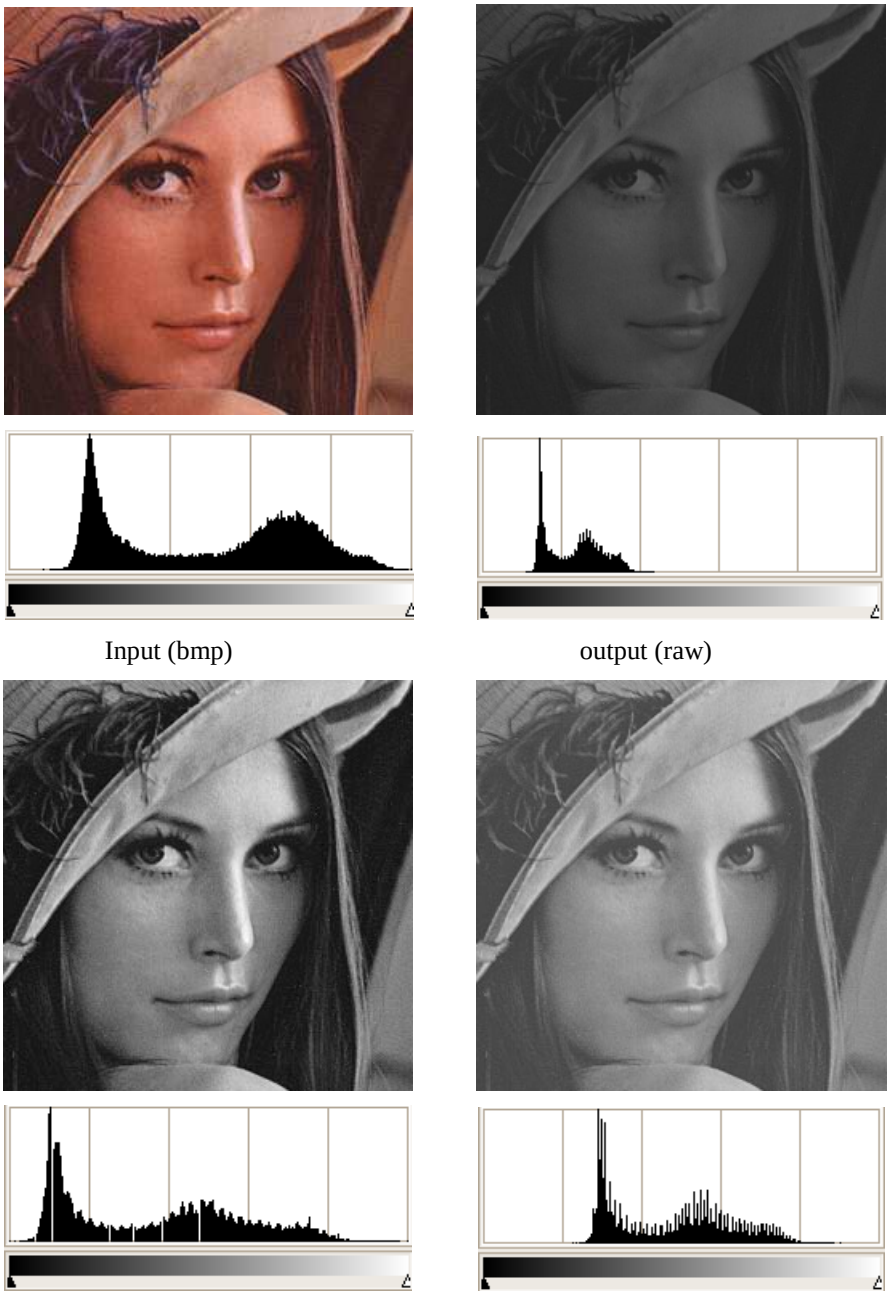


Figure 3. 3. Layout of pixel matrix 2x2



Input (bmp) output (raw)

Output (relative) output (absolute)

Figure 3. 4. The simulation results of LUT approach (cap extracted)

Table 3. 5. The statistical information of LUT approach results (cap extracted)

images	Mean (μ)	Standard (σ)	median
input	89.4	45.5	92
Raw	57.6	18.2	59
Relative	93.1	56.9	98
Absolute	119.7	38.4	123

The simulation results of considering all parasitic capacitance is shown in Figure 3. 4, and the detail information is listed in the Table 3. 5. It is shown that the results with considering all parasitic capacitance will make the final image a little dark than the other two cases (no cap & equivalent cap), and it proves that the routing parasitic can affect the image sensor performance, even in the small matrix size. A detail comparison is listed in the Table 3. 6, it is indicated that there is a more apparent difference in the results of considering routing parasitic capacitance.

Table 3. 6. The voltage comparison in all cases in LUT (mV)

Images	256x256	512x512	1024x768	1600x1200
No Cap	802.515	802.515	802.515	802.515
CEQ	802.515	802.514	802.513	802.511
CEX	791.970	791.967	791.964	791.958

3.2.2 CMOS Image Sensor response variability

Due to the uncertainty in CMOS process, such as, the variation in the oxide layer thickness T_{ox} of the reset transistor, this results in the threshold voltage variation in transistors. The threshold voltage under zero bias condition can be modeled as the following normal distribution equation symbolized as *N*.

$$v_{th0} \sim N(\mu, \sigma) \qquad [3.2]$$

As shown in Figure 3. 5, 94% of the range is covered within the $\mu \pm 3\sigma$ according to the Gaussian Law.

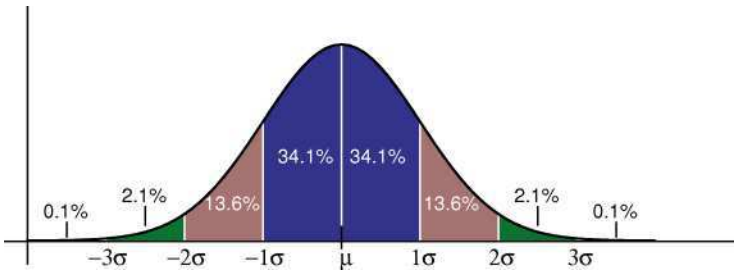


Figure 3. 5. The probability density function of normal distribution

The CMOS image sensor suffers from the Fixed Pattern Noise which is mainly induced by the variability in CMOS process, such as the variation in the oxide layer thickness T_{ox}. Another source of FPN noise is attributed to the variation in the photodiode size which is caused by the etching during the fabrication. This variance existing in transistors will spread randomly among the pixels across the sensor matrix. In the test case of a small pixel matrix 20x20, each pixel column has an output voltage distribution as shown in Figure 3. 6. Ten times of matrix Monte Carlo simulation result demonstrate that the output voltage of each column varies in every simulation.

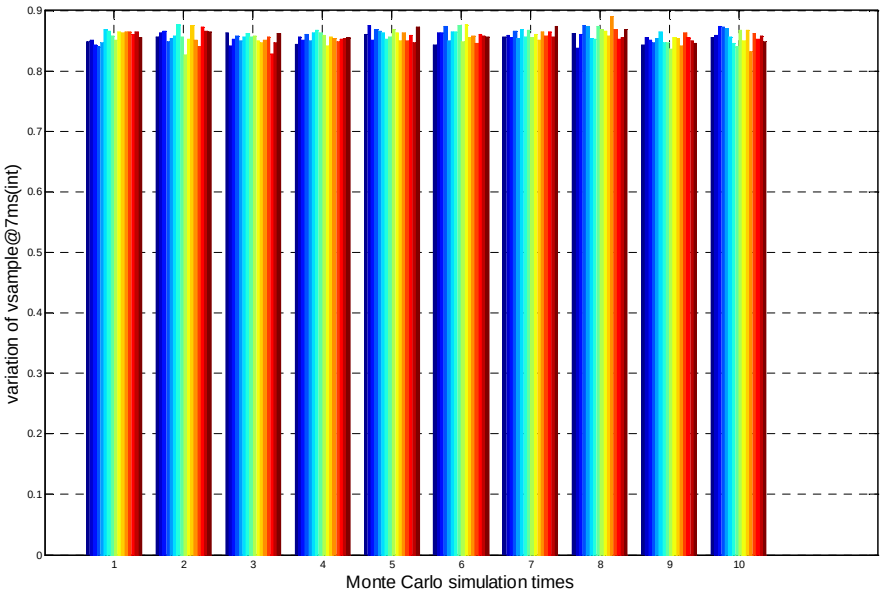


Figure 3. 6. Output voltage varies on the 3T-APS pixel matrix 20x20

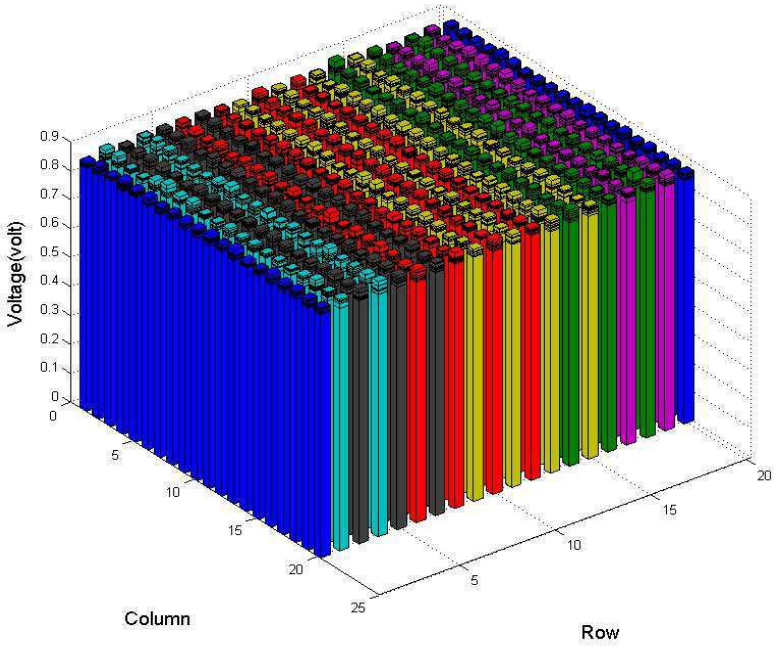


Figure 3. 7. Matrix 20x20 pixel response variation

A closer view of matrix response variation is shown in Figure 3. 7, each bar represents an output of a single pixel located on the matrix, a small variation in each bar can be observed among the whole matrix 20x20. As shown in Figure 3. 8, in 7ms integration case, the pixel output voltage varies from 750mv to 820mv. The output nominal value (μ) is 782mv with the standard deviation (σ) 10mv.

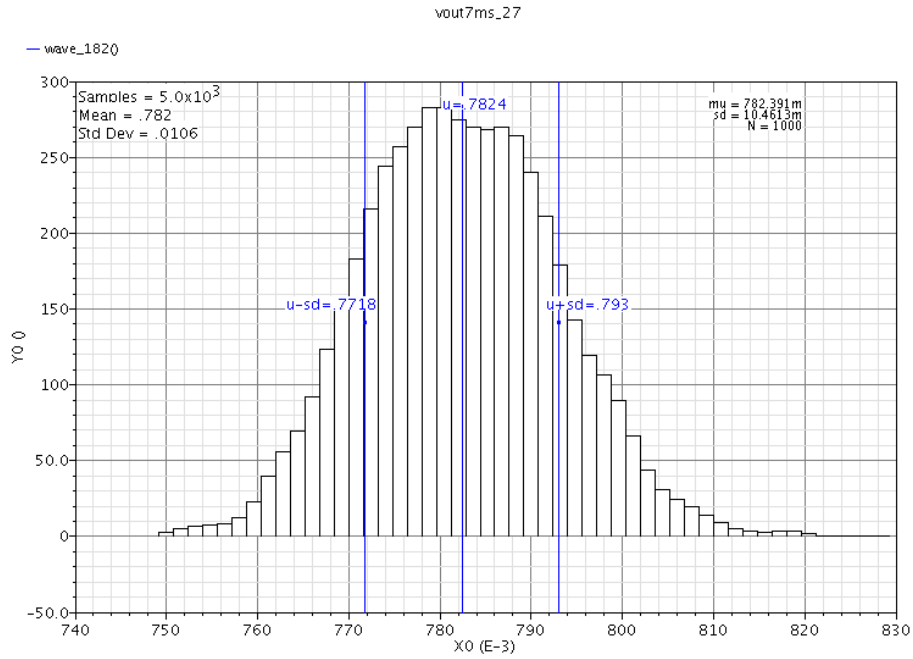
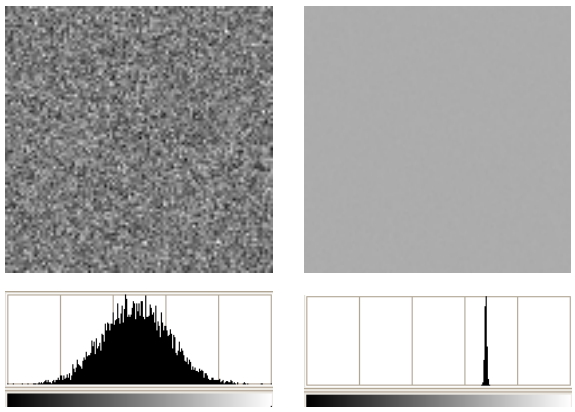


Figure 3. 8, single pixel output voltage variation (1000 times)

For observing apparently the response variability, a unique light intensity source (image) is applied to investigate the sensor matrix response variability versus the process parameters, as shown in Figure 3. 9, the up-left part is the original input image with 92 x 92 pixels, the up-right part is the raw results, bottom-left part is the relative results and the bottom-right part is the absolute result.

Input output (raw)



Output (relative) output (absolute)

Figure 3. 9. The sensor matrix response versus process variability (MC)

As indicated in the histogram of absolute result, the response is not unique comparing with the unique input, and this variation is caused by the variability in CMOS transistor, especially from the CMOS process parameter, such as t_{ox}.

Table 3. 7. The images statistical information of MC approach

images	μ,σ
input	(150, 0)
Absolute	(172.6, 1)
Raw	(83, 0.2)
Relative	(123.9, 32.3)

Table 3. 7 gives out the detail information of output images, it can be proved that a higher image generation reference voltage (e.g. VDD = 3.3, Vreset ≈ 1.588) will lower the output image pixel intensity value (DN: digital number), but it can help suppressing the pixel response variation in output images.

In Fast estimator approach, the number of run of classical Monte Carlo simulation is set to a constant value. With adding the probability estimator, the statistical information of response variability is extracted from finite sampling data and the correlated data following the identically distribution is generated and re-distributed in the final outputs. As shown in Figure 3. 10 and listed in Table 3. 8, there is no difference in raw result between classical Monte Carlo approach and Fast estimator approach. The

difference mainly exists in the relative result, this is because the 256 times Monte Carlo simulation provides just a finite data base for estimator, this difference (error) will be reduced as increasing the simulation times (sampling data points).

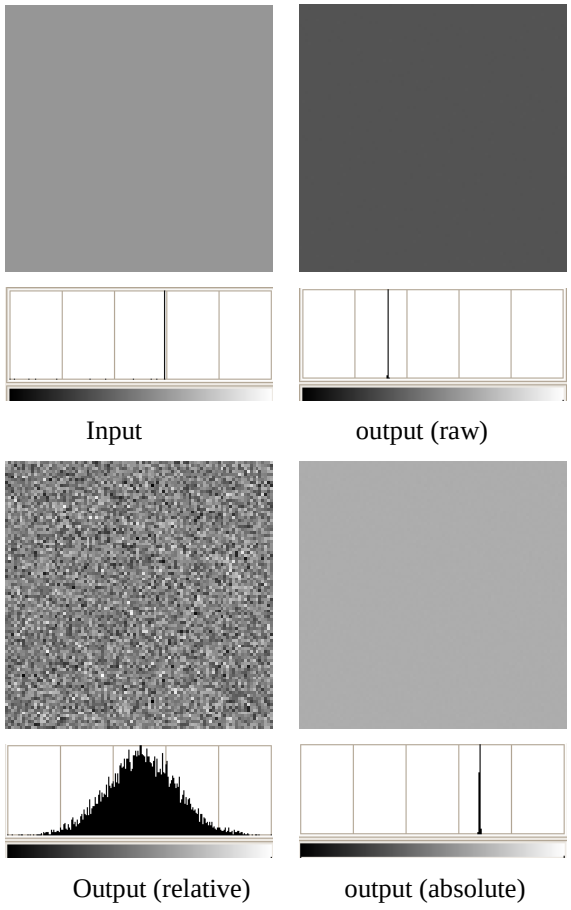


Figure 3. 10. The sensor matrix response versus process variability (Estimator 256)

Table 3. 8. The images statistical information of Estimator approach

images	μ,σ
input	(150, 0)
Absolute	(172.6, 0.6)
Raw	(83, 0.2)
Relative	(129.4, 33.7)

3.3 Performance of Fast simulation methodology

3.3.1 Accuracy performance

The Fast simulation methodology is dedicated to solve the time consumption problem encountered in the circuit classical simulation method. It is intended to improve the simulation efficiency and maintain the simulation accuracy. As indicated in the Table 3. 9, 4 test cases have been performed and the results have been listed below. In the case of considering all the pixel layout parasitic capacitance, 4 pixel matrix sizes are simulated in both classical method and fast method, the simulation result shows that error can be maintained within 2.7mv.

Table 3. 9. The accuracy performance of Fast methodology in CDS output voltage (mV)
(Photocurrent=3pA)

image	20x20	40x40	60x60	80x80
classical	431.44589	431.44577	431.44566	431.44553
LUT	428.72174	428.72162	428.72150	428.72138

The output reset voltage gets good approximation in LUT approach, as listed in the Table 3. 10. A 0.1mv voltage error level is achieved, and it proves that the LUT approach is stable.

Table 3. 10. The accuracy performance of Fast methodology in reset voltage (mV)
(Photocurrent=3pA)

image	20x20	40x40	60x60	80x80
classical	1601.0397	1601.0397	1601.0397	1601.0397
LUT	1601.174	1601.174	1601.174	1601.174

From the view of system level, the final outputs are images which stand for the output voltages in low level simulation in our approaches. The final output images in different resolutions are attained from our image generation methods. As indicated in the Table 3. 11, 1 gray level error is found in absolute result (ABS) of LUT approach

comparing with the classical method, this error is caused by calculating (round float into integer in our method, such as 68.7 to 69 and 68.2 to 68), and it's equal to 0.4% of intensity range (256 gray levels).

Table 3. 11. The accuracy performance in final images

image	20x20			40x40			60x60			80x80		
	ABS	REL	RAW	ABS	REL	RAW	ABS	REL	RAW	ABS	REL	RAW
classical	69	27	33	69	27	33	69	27	33	69	27	33
LUT	68	26	33	68	26	33	68	26	33	68	26	33

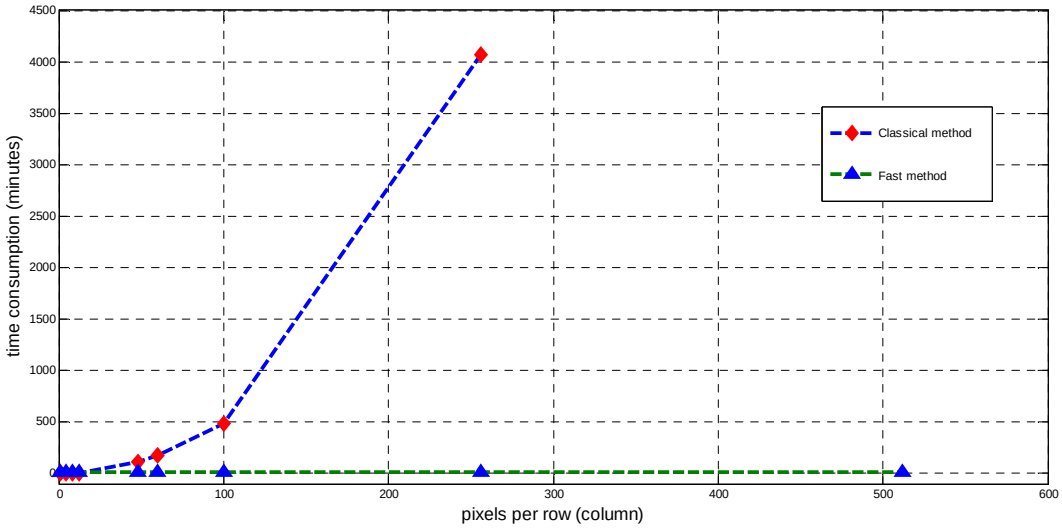
3.3.2 Time consumption performance

In classical simulation, the low level SPICE simulation is performed too many times and it takes too long time. In fast simulation, the time consumption is largely reduced benefiting from the LUT table. As shown in Figure 3. 11, it gives a comparison between classical simulation and LUT approach, the time consumption of classical method increases drastically with matrix size, whereas the time consumption of LUT approach increases slowly. For example, the time consumption of classical method is 70 hours for the matrix 256x256, and in fast method the time consumption is just 9 minutes, so the fast LUT approach can speed up 350 times. In LUT fast simulation approach, the classical low level spice simulation is performed 256 for generating the data table, this will cost almost 9 minutes, so it is not recommend to apply LUT approach when the input images is smaller than 16x16 (256 pixels). As indicated in the Table 3. 12, the Fast LUT approach takes much less time than classical method. The time consumption increases a little along with increasing the input image size (pixel numbers), whereas time consumption of classical method increases drastically.

Table 3. 12. The time performance of Fast methodology

image	20x20	40x40	60x60	80x80
classical	13′15″	1h1′10″	2h5′3″	3h4′5″
LUT	8′54″	9′01″	9′05″	9′07″

A global time consumption comparison is drawn in the Figure 3. 11, in the up part, following the trend we can conclude that the fast method approach consume much less time than classical method. In the bottom part, the time consumption increases within 1 minute of LUT approach when the matrix size increases from 8x8 to 256x256, but the time consumption increases to days in classical approach. The time consumption increasing in LUT approach is due to the task of mapping function, it needs just to match the input to the output, so the increasing is not very much. The fundamental time consumption of LUT approach is for building the inner table (Input to Output).



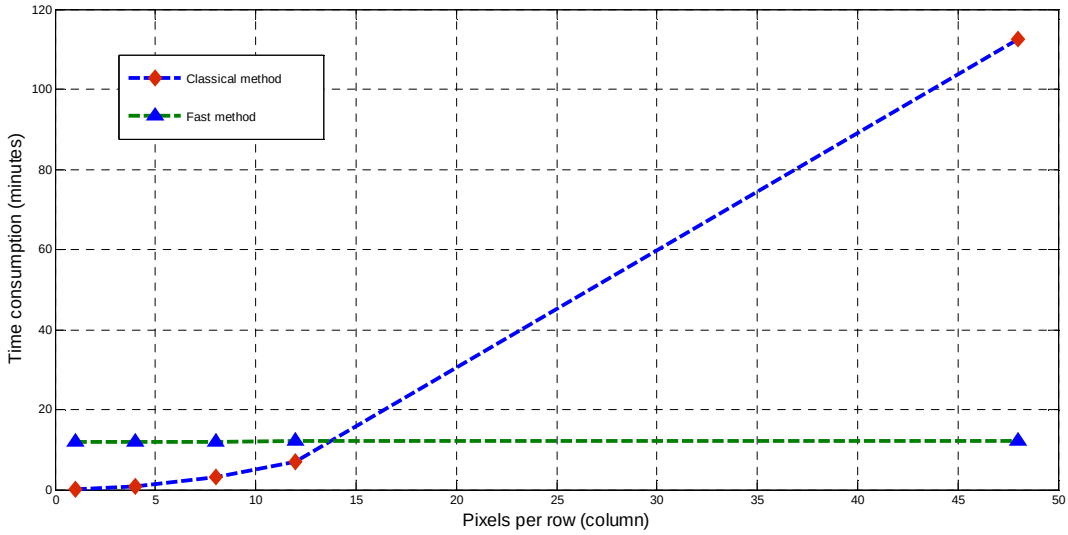


Figure 3. 11. Time consumption of Classical simulation and LUT approach

Conclusion

In this chapter, the image sensor simulation in different levels is firstly introduced, and then, the considerations concerning the pixel performance are listed and taken into the simulation. The nominal response which stands for the sensor's normal performance is classified into three types, such as pixels with no capacitance, pixels with equivalent capacitance and pixels with extracted capacitance from layout. For studying the image sensor response variability, the classical Monte Carlo method based approach and fast estimator included simulation approach are talked, and the correlated simulation results are given out. In classical simulation, the memory overflow occurs when the matrix size reach approximately 512x512 ($\approx 2.5*10^5$) pixels, and this limitation is overcome in fast simulation method, it can be used to simulate $15*10^6$ pixels, the simulation capability is extended 60 times. Time consumption performance of fast simulation methodology is studied and it is proved that the fast simulation method can improve largely the simulation efficiency. Hours of classical simulation can be reduced within several minutes, for example, in a small sensor matrix, the simulation speed is improved 20

times, and this value is much higher as increasing the imager pixel numbers. From the accuracy study, it is clearly that the fast simulation methodology keeps efficiently the precision in output voltage and intensity value of output images. The fast simulation methodology is quite suitable for the 3T-APS matrix level simulation.

Chapter 4 Results on Different pixel architectures and different technologies

Based on the 3T-APS pixel, other pixel architectures are simulated. The logarithmic 3T-APS aiming at high dynamic range is formed by operating the reset transistor as a forward biased diode. The high dynamic range is achieved benefiting from that the diode current grows logarithmically with voltage increasing in forward biasing mode. For achieving a higher performance, the 4T-APS was invented in separating the sensing node and charge storage node by inserting a transfer gate between the photodiode and charge storage node. The 2.5T-APS is implemented by adding another sensing-transfer branch to the charge storage node which forms two pixels sharing the same charge storage node. The sharing node pixel architectures gain a higher fill factor at the expense of more complex read out timing sequence and CDS circuit. As the MOSFET continuous scaling, its physical limit is approaching. The emerging technology, electronic devices with higher electrical performance in sub-micro and nano-scale are compromising candidate of implementing the new pixel, for example, the Single Electron Transistor (SET), Carbon Nanotube Filed Effect Transistor (CNTFET).

4.1 Different pixel architectures

4.1.1 4T APS

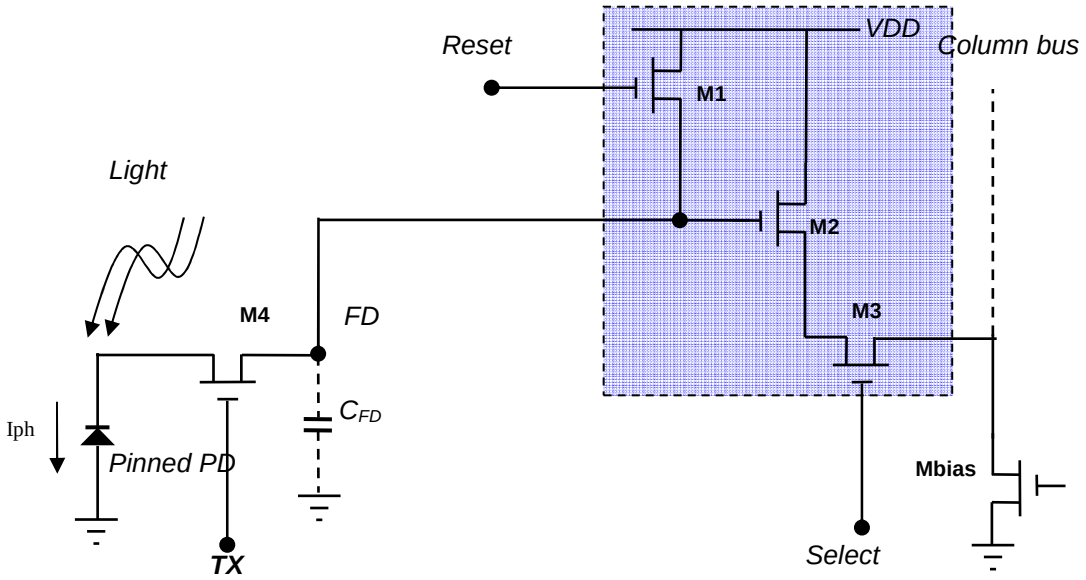


Figure 4. 1. The schematic of 4T-APS

As shown in Figure 4. 1, the charge to voltage conversion node (FD) is separated from the photodiode (sensing node) by inserting a transfer gate M4. The floating node FD is first reset to a reference voltage and this voltage is buffered to the column bus through the transistor M2, M3 and Mbias located at the bottom of the column line. This reference voltage is sampled by the CDS circuit and saved as Vcds1. In the second step, the photons starts integrating on the photodiode and generating photon-electrons, the generated electrons will be continuously collected on the photodiode inner capacitance in the whole exposure time (integration time), the electrons are shifted to the floating diffusion node by closing transfer gate M4, it charges will make a voltage drop on the CFD. Another sampling pulse arrives when this charges transfer procedure has been finished as shown in Figure 4. 2. The voltage on the floating node is sampled again by

CDS circuit and saved as the Vcds2. The difference of Vcds1 and Vcds2 is processed by the image generation methods to form the final images.

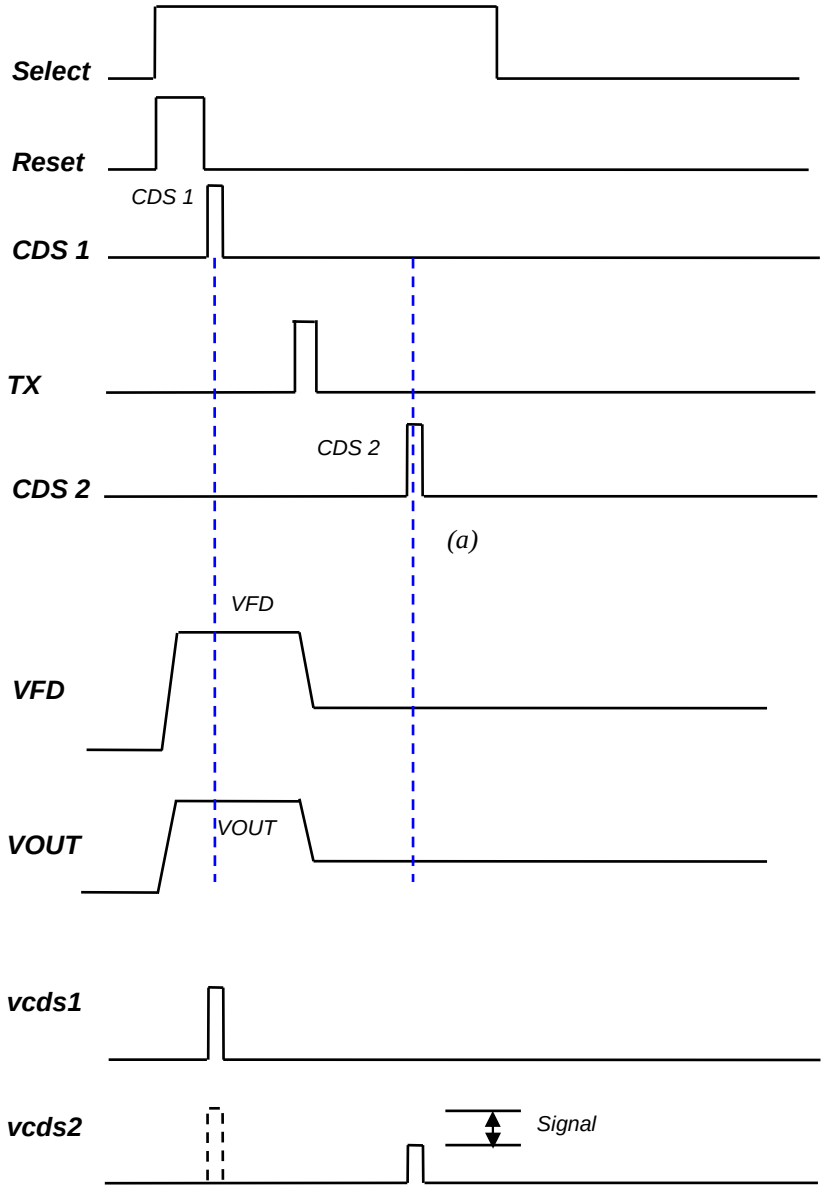


Figure 4. 2. The timing diagram of 4T-APS

4.1.2 2.5T APS

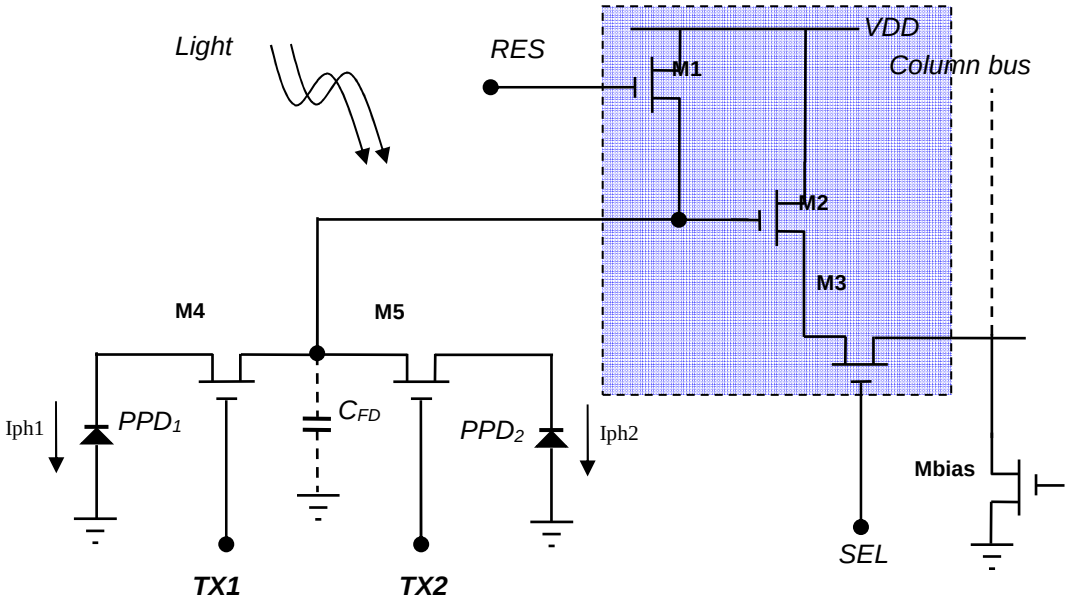


Figure 4. 3. 2.5T-APS pixel architecture

The idea of sharing floating node and pixel readout component brings new pixel architecture as shown in Figure 4. 3. Another branch of photodiode and transfer gate is attached to the FD and combined to the pixel architecture. The total number of transistors in the pixel is five (except for the column bias transistor Mbias), and the number of photodiodes (pixel) is two, so this architecture gives 2.5 transistors in each pixel and thus called as 2.5T-APS. The work principle of 2.5T pixel is almost the same as 4T pixel with different readout timing sequence.

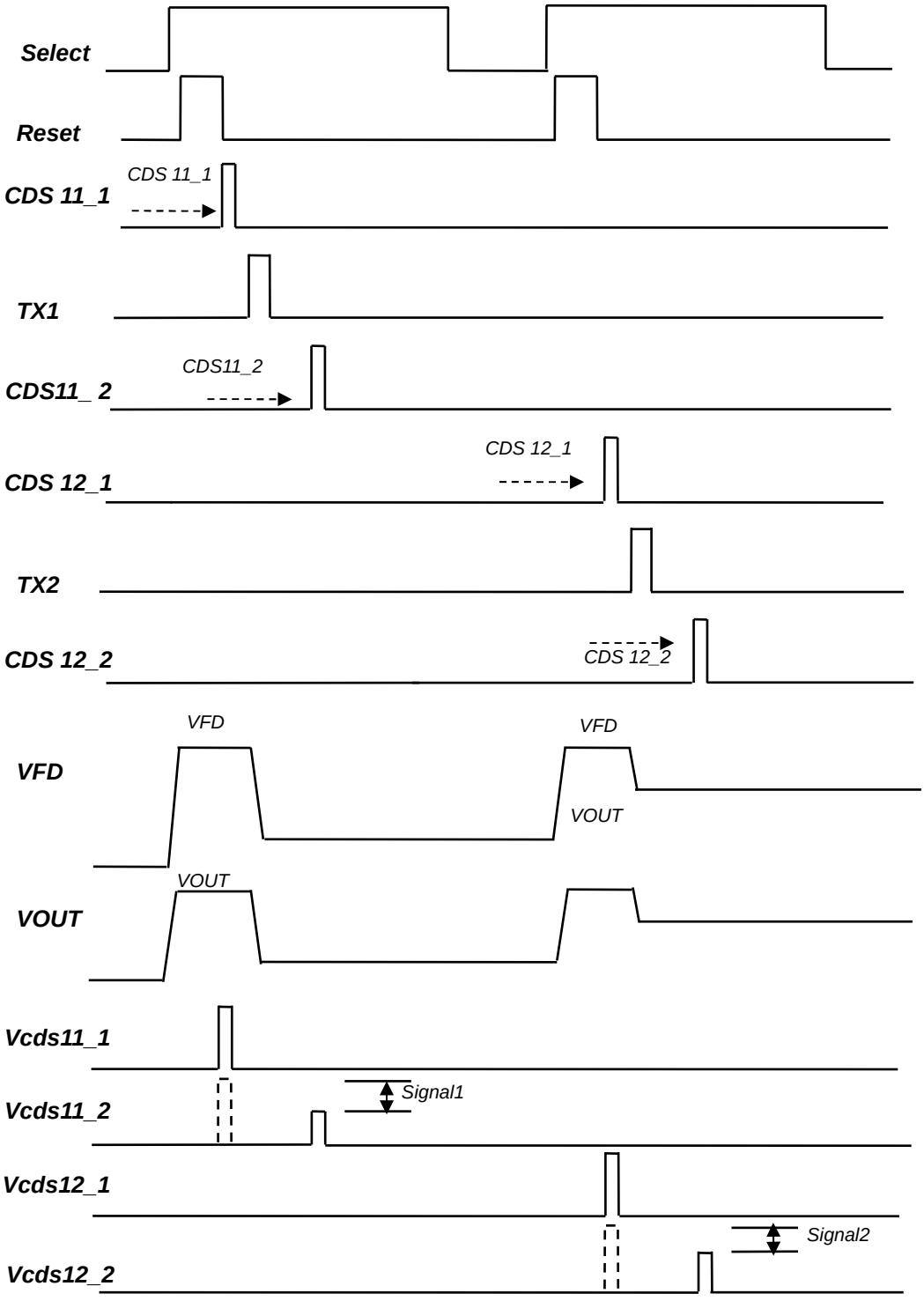


Figure 4. 4. The timing diagram of 2.5T pixel

As indicated in the Figure 4. 4, the two pixel output signals are readout and sampled by two different CDS branches. CDS11_X and CDS12_X represent the CDS timing sequence corresponding to the pixel_1 and pixel_2 in the 2.5T pixel architecture, respectively.

4.1.3 log-3T APS

By connecting the gate and drain region of a CMOS transistor, a diode connected MOSFET can be set up. Benefiting from the voltage-current characteristic of diode, a pixel whose output voltage increases logarithmically with the light intensity (photocurrent) was developed [64].

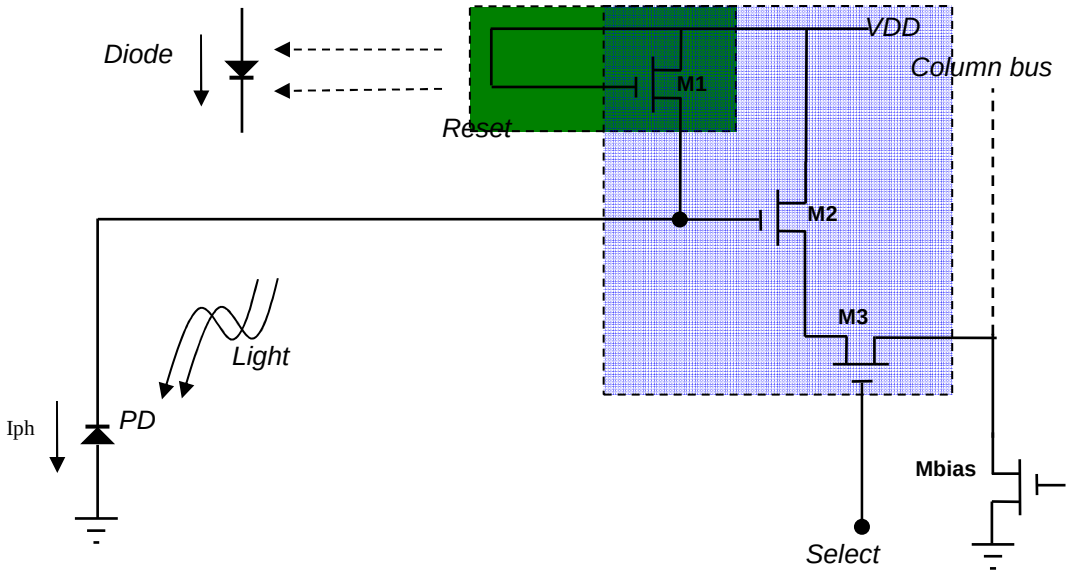


Figure 4. 5. Logarithmic 3T pixel architecture

As shown in Figure 4. 5, the voltage drop across on the diode is determined by the load current following the equation [4.1].

$$I = I_0 \cdot (e^{\frac{eV}{kT}} - 1) \qquad [4.1]$$

Where, I is the current through the diode, I_0 is the diode saturation current, e is the electron charge, V is the applied voltage, T is the temperature in Kelvin, k is the

Boltzmann’s constant. As shown in Figure 4. 6, a small voltage variation occurs when a large range of current flowing through the diode. This characteristic is adopted to extend the pixel’s imaging range and avoid saturation in large photocurrent range. The logarithmic 3T pixel can achieve a higher dynamic range compared to the conventional 3T pixel whose output voltage increases linearly with increasing the light intensity. As shown in Figure 4. 7, the photocurrent is increased 50x while the output voltage just decreases 0.05volt from 1.61 to 1.56, this characteristic is adopted to develop high dynamic image sensor.

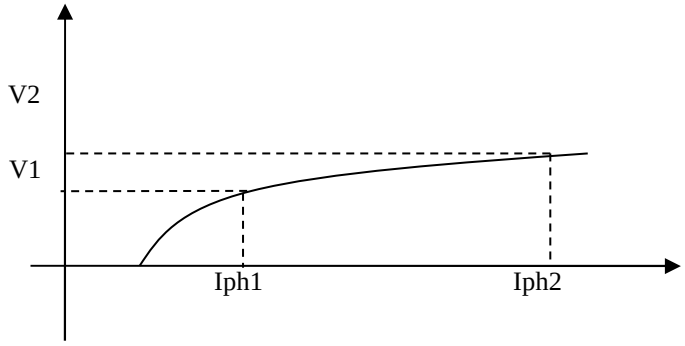


Figure 4. 6. The voltage current characteristics of diode

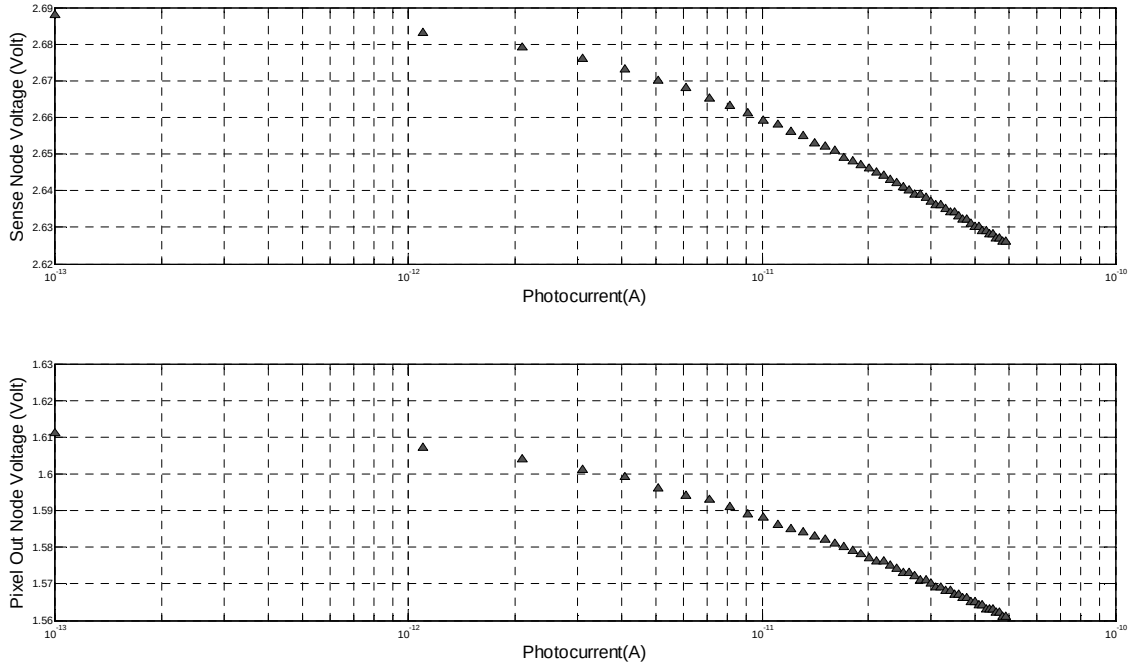


Figure 4. 7. Electrical performance of log-3T APS

4.1.4 CNTFET image sensor

A large part of success of the MOS transistor is due to its scalability, which permits a higher performance while scaling the transistor size. Although this trends still continues, the Silicon MOSFET is approaching its theoretical limits. The innovation is needed to circumvent barriers due to the fundamental physics that constrains the conventional MOSFET when its critical dimension size scales down to 50nm technological node. For continuing improvement in density and performance of electronics system, the common solutions are the high dielectric constant (high-K) gate dielectric, metal gate electrode, double gate FET, etc. In recent years, the new materials and devices are developed to complement or even replacing the CMOS transistor. Among the various new materials and structures, the carbon nanotube (CNT) gives the promising characteristics. The first report concerning CNT is proposed by *Ijima* in 1991[56]. The metallic, semi-conducting property and ability to carry high current bring

the CNT huge potential for applications in electronics. The cylinder CNT generated by rolling up the graphene sheet is used as the transport channel for getting higher current density in unit channel length. The first CNT based field effect transistor (CNTFET) was fabricated as a back gate transistor in 1998[57]. Although these CNTFET have a high I_{on}/I_{off} ratio (almost 10^5), the limitations of the high parasitic contact resistance, low drive current and transconductance were met. To overcome these limitations and get better performance, a top gate CNTFET was proposed by Wind et al. in 2003[58]. The lower threshold voltage, higher drain current, higher transconductance and higher I_{on}/I_{off} ratio over the back gate CNTFET were obtained. According to the electrodes used in connecting the channel with source/drain region, the CNTFET can be categorized as the Schottky-barrier CNTFET (SB-CNTFET)[59], Partially gated (PG-CNTFET)[60] and doped-S/D CNTFET[61].

The cylindrical CNTFET is shown symbolically as Figure 4. 8, when the gate voltage exceed its threshold voltage, the carbon nanotube channel is turned on for transporting the electrons or holes according the nanotube doping type.

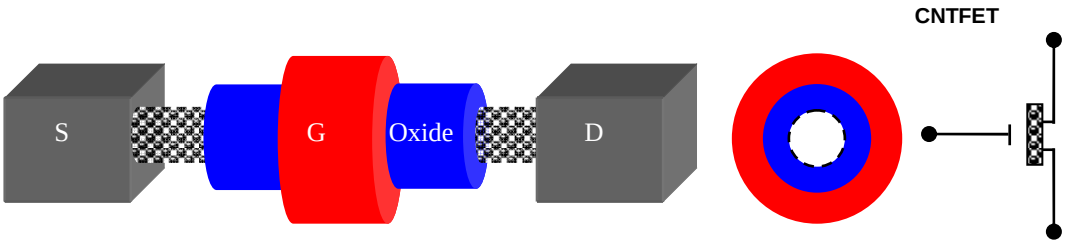


Figure 4. 8, the generic symbol of Wrap around CNTFET[62].

Recent years, an ambipolar double gate DG-CNTFET is reported, the device has two gates G and PG, the gate G turns the device on or off, as the regular gate of a MOSFET, while the polarity gate (PG) controls the type of polarity setting to p-type or n-type. If a large positive voltage is applied at PG, the device behaves as n-type transistor, while a large negative voltage applied at PG would set the polarity to p-type as shown in Figure 4.9.

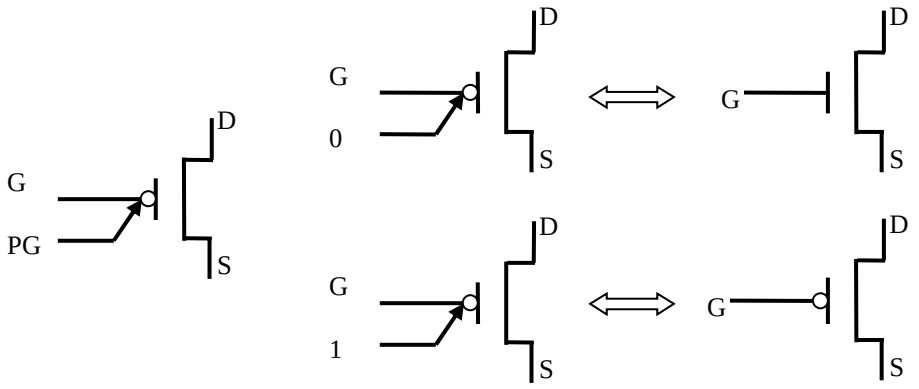


Figure 4. 9. The symbol of ambipolar double gate CNTFET

The property of working as a p-type or n-type transistor makes DG-CNTFET an emerging alternative for complementary circuit design. Compared to the CMOS transistor, the DG-CNTFET has the lower threshold voltage and higher charge mobility, these characteristics make DG-CNTFET more suitable for high integration density and high speed applications. A DG-CNTFET based image sensor pixel as shown in Figure 4. 10, is simulated in this work, the DG-CNTFET is modeled by verilog-A language and the photodiode is modeled as the current source connecting parallel with a sub-diode.

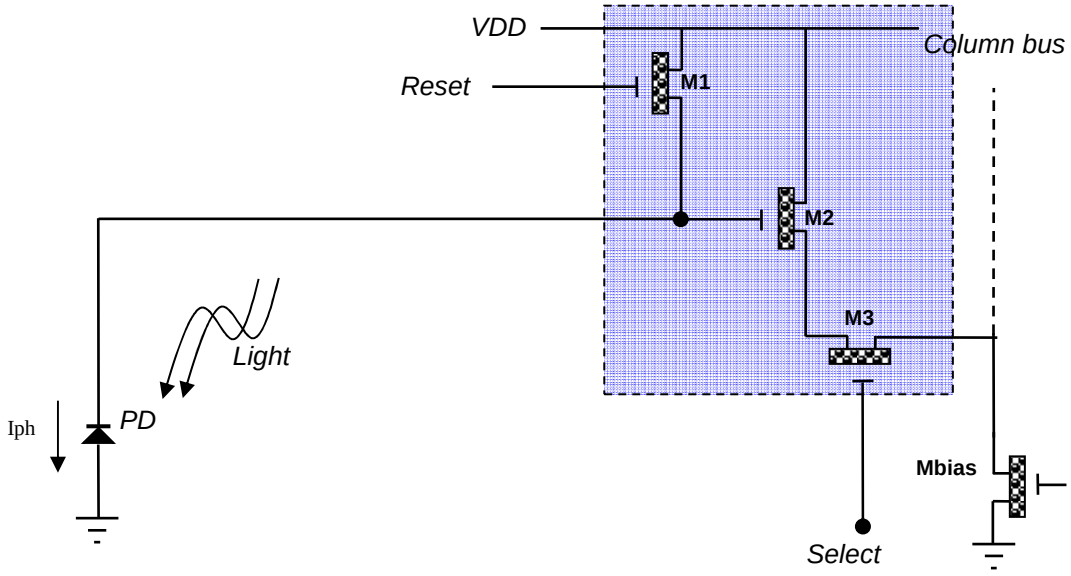


Figure 4. 10. The DG-CNTFET 3T APS schematic

4.2 Results and performance on CMOS 4T APS considering neighboring pixel capacitance

Various test case results of considering neighboring pixel capacitance are listed in the following Table 4. 1, for example, in the matrix 40x40, the classical method output voltage is 1.6256 volt and the fast LUT method outputs a voltage 1.6274 volt, the voltage error is 1.8mv. As indicated in the table, the voltage errors in each matrix size of these two methods are all within 2 millivolt.

Table 4. 1. The output voltage accuracy of 4T APS architecture (unit mV)

image	20x20	40x40	60x60	80x80
Classical	1625.6921	1625.6921	1625.6921	1625.6921
LUT	1627.3591	1627.3591	1627.3591	1627.3591

After data processing, the final image intensity values (digital numbers: DN) are listed in the Table 4. 2, it is found that the final outputs of these two methods are closed. It proves that the fast simulation methodology is effective in simulating 4T APS.

Table 4. 2. The digital number (DN) accuracy of 4T APS architecture

image	20x20			40x40			60x60			80x80		
	ABS	REL	RAW	ABS	REL	RAW	ABS	REL	RAW	ABS	REL	RAW
classical	233	241	126	233	241	126	233	241	126	233	241	126
LUT	233	241	126	233	241	126	233	241	126	233	241	126

The time performance is listed in the Table 4. 3, it can be seen that the classical simulation takes much more time when comparing with the LUT method, for example, three hours time consumption of simulating matrix 80x80 in classical method is reduced largely from 3 hours to 10 minutes, the time performance in LUT method is predominant.

Table 4. 3. Time consumption of various methods in 4T APS architecture

image	20x20	40x40	60x60	80x80
Classical	13′40″	54′42″	1h10′11″	3h40′29″
LUT	8′53″	8′59″	9′03″	9′27″

4.3 Results and performance on CMOS 2.5T APS

The selected shared pixel architecture in this thesis is 2.5T APS. A close view of simulation results comparison is listed in the Table 4. 4, the different sensor matrices are given the same light intensity, and the column capacitance resulting from the interconnection is taken into account. For example, the output voltage of matrix 60x60 in classical method is 457.5mv, and in LUT method this value is 455.84mv, the voltage error is 1.8mv. It is can be noticed that the pixel neighboring capacitance in small matrix size do not affect seriously the pixel output voltage, and the LUT method is accurate and stable.

Table 4. 4. The output voltage accuracy of 2.5T APS architecture (mV)

image	20x20	40x40	60x60	80x80
classical	457.51473	457.51473	457.51473	457.51473
LUT	455.84005	455.84005	455.84005	455.84005

This voltage error will be reflected in the final output images as indicated in the Table 4. 5. In all test cases, the same input light intensity can get the same output digital number, thus it proves that the fast simulation method is compatible with the 2.5T APS architecture.

Table 4. 5. The digital number (DN) accuracy of 2.5T APS architecture

image	20x20			40x40			60x60			80x80		
	ABS	REL	RAW	ABS	REL	RAW	ABS	REL	RAW	ABS	REL	RAW
classical	68	26	35	68	26	35	68	26	35	68	26	35
LUT	68	26	35	68	26	35	68	26	35	68	26	35

The time consumption performance of these two methods in simulating 2.5T-APS image sensor is shown in Table 4. 6, and it proves that the LUT method is effective on accelerating image sensor matrix simulation.

Table 4. 6. Time consumption of various methods in 2.5T APS architecture

image	20x20	40x40	60x60	80x80
classical	7′15″	29′42″	1h04′11″	1h54′29″
LUT	9′14″	9′8″	9′16″	9′56″

4.4 Results of log3T APS image sensor

When applying the fast simulation methodology to logarithmic 3T-APS [65] image sensor, a randomly selected output voltage list is achieved as indicated in the Table 4. 7, it is found that the error among these two methods is within 0.1 millivolt. This is because the output voltage of logarithmic APS increases logarithmically with the photocurrent, and the interval of the sampled intensity table do not affect seriously the computing precision.

Table 4. 7. The output voltage accuracy of log-3T-APS architecture (mV)

image	20x20	40x40	60x60	80x80
Classical	1531.3346	1531.3346	1531.3346	1531.3346
LUT	1531.3845	1531.3845	1531.3845	1531.3845

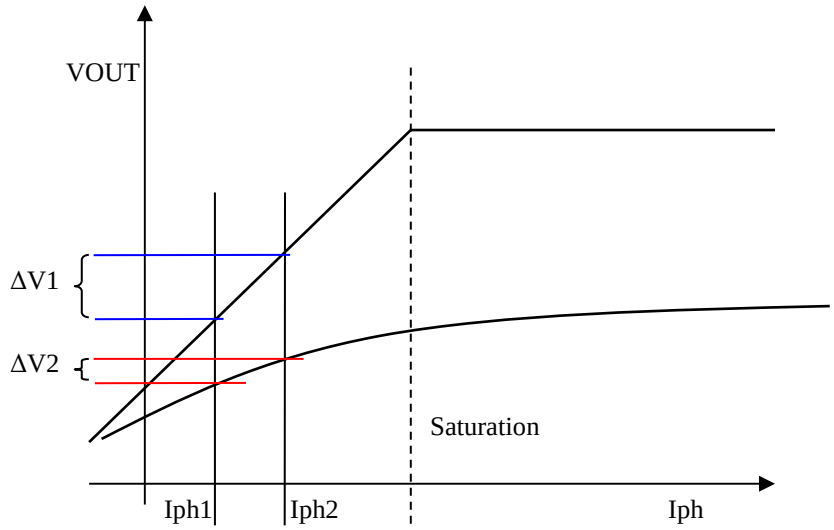


Figure 4. 11. The comparison of Linear APS and Logarithmic APS

Table 4. 8. Time consumption of various methods in log3T APS architecture

image	20x20	40x40	60x60	80x80
classical	13′51″	55′7″	2h09′43″	3h41′8″
LUT	8′55″	8′40″	9′51″	8′47″

4.5 Results of CNTFET image sensor

A CNTFET modeled in *veriloga* language is adopted in this thesis work, and it is used to build the typical 3T APS structural model. In the model, the diameter of nanotube is set to be 3.0nm and the total number of contacting bands is 6.

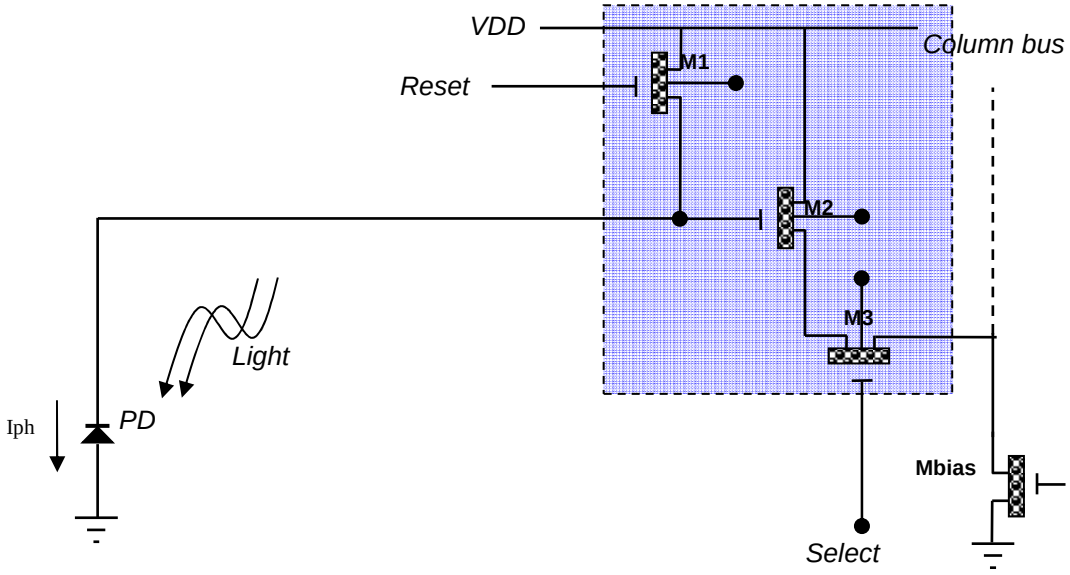


Figure 4. 12. The DG-CNTFET 3T APS schematic (configurable back gate)

The result in output voltage proves that the LUT approach is effective in accelerating sensor matrix simulation, because as shown in Table 4. 9, the LUT keeps the consistency with classical simulation in results. The voltage error between classical method and fast method is caused by sub-sampling (the full photocurrent range is quantified as 256 points in fast method), and the voltage varies along the row is caused by the column load capacitance resulting from the interconnection.

Table 4. 9. The output voltage accuracy of CNTFET 3T APS architecture (mV)

image	20x20	40x40	60x60	80x80
classical	652.963	652.518	652.001	651.514
LUT	652.961	652.516	651.999	651.512

As indicated in the Table 4. 10, 1 digital number (DN) error is found in test case 20x20 pixels, this is caused by “round” function in the signal processing, from voltage to digital numbers. In all of the test cases, the LUT simulation gets a good agreement with the classical simulation. In the Double Gate CNTFET pixel, the pixel response linearity is quite well and voltage loss is smaller comparing with classical CMOS technology. The time consumption reduction in LUT simulation method is shown in the Table 4. 11.

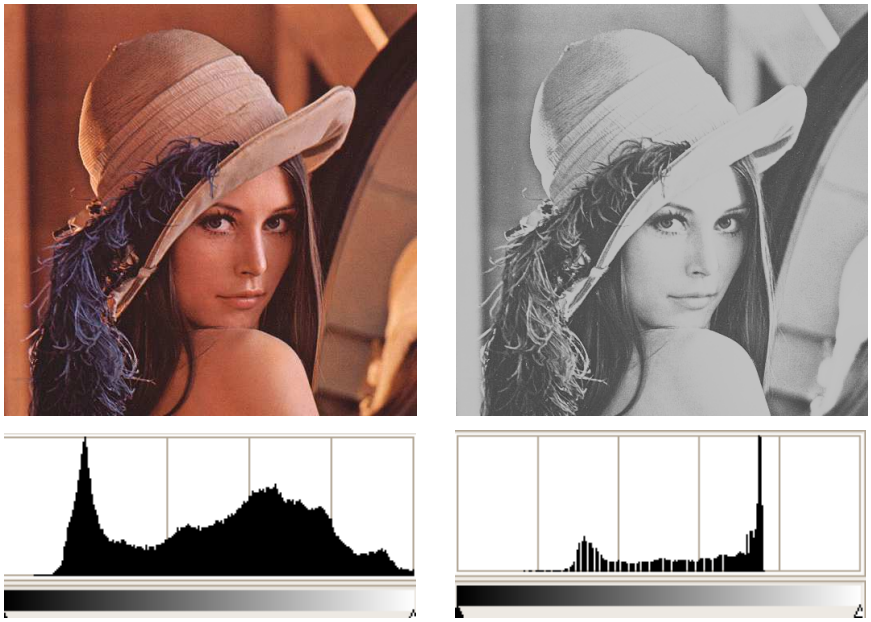
Table 4. 10. The digital number accuracy of CNTFET 3T APS architecture

image	20x20			40x40			60x60			80x80		
	ABS	REL	RAW	ABS	REL	RAW	ABS	REL	RAW	ABS	REL	RAW
classical	170	221	50	169	210	50	169	210	50	169	210	50
LUT	170	221	50	169	210	50	169	210	50	169	210	50

Table 4. 11. Time consumption of various methods in CNTFET 3T APS architecture

image	20x20	40x40	60x60	80x80
classical	13′51″	54′53″	2h03′22″	3h44′10″
LUT	8′57″	9′01″	9′05″	9′12″

The input and output images are listed in the Table 4. 11, there are small difference in the raw output result and absolute output result, it is because that the voltage drop (drain to source) in CNTFET reset transistor is very small. This makes the pixel reset level achieve nearly the VDD, according to the image generation equations, the raw output image is almost the same with absolute output image. This proves that the image sensor loss less voltage swing in CNTFET technology comparing with CMOS technology.



Input output (raw)

Output (relative) output (absolute)

Figure 4. 12. The input and output image of CNTFET 3T-APS sensor

Conclusion

In the chapter 4, kinds of active pixel architecture are introduced. The fast simulation methodology is applied to simulate 4T-APS matrix, 2.5T-APS matrix, and 3T APS in nanotube technology. After comparing simulation results in different pixel architectures, it can be concluded that the LUT approach is stable in accelerating image sensor simulation. It should be pointed out that the new simulation methodology could support the other pixel architectures (5T, 7T), the rolling shutter mode read out scheme is used in the current work, and another read out scheme (e.g. global shutter mode) is not used in the current work, but it could be supported. Further more, although the time consumption in LUT approach increase along with the pixel numbers, it is very slow. The scalability of LUT approach is greatly improved comparing with classical method, and the memory overflow error can be avoided in LUT approach. The LUT method is potentially used to solve large memory consumption, large time consumption problems in parametric simulation.

The simulation result of all cases shows that the LUT approach is reliable, and this benefits from the unfixed form model (LUT). This implies that the LUT is effective in solving problem in massive computing.

Chapter 5 Conclusion & Discussion

This thesis work starts with reviewing the state of the art of image sensor in technology aspect and the pixel architecture aspect as well. For aiding the development of CMOS image sensor, although kinds of CAD tools have already been developed, the current circuit simulation method faces the challenge of simulating image sensor matrix, such as high time consumption requirement, this thesis is dedicated to explorer a novel approach for solving this issue.

The main contributions are talked in this part, and some perspectives and future work are discussed below.

5.1 Fast simulation methodology

The developed fast simulation methodology is intended to gap the simulation accuracy and simulation time consumption in electrical level. The sensor matrix level simulation consume too much time in classical simulation for achieving the high accuracy, however, in the domain of CAD, the simulation accuracy and time consumption is always an conflict, and it needs to be treated carefully while aiming at a better compromise. The thesis studies the simulation accuracy and time consumption in image sensor simulation and proposes a fast scalable simulation methodology. The Look-Up-Table based simulation methodology is intended to improve the simulation efficiency while maintaining the accuracy. It builds a bridge between the simulation input and output. Generally, this LUT can be viewed as an informal and non-fixed model in high level. The accuracy of LUT approach is directly related to database (Table) which is generated from the input image through photocurrent converter.

The Monte Carlo method is suitable for studying the system response versus multiple uncertain factors via large computing, and it can help estimating the response variability. The advantage of Monte Carlo simulation is that it is able to cover the random cases if the simulation times are enough. The Monte Carlo method is adopted to study the pixel matrix response variability in this thesis. In typical simulation, performing once M x N pixels simulation takes a long time, in Monte Carlo simulation, it needs to perform R times (random numbers, e.g. 1000 or 10000) of M x N pixels simulation, the simulation time increases drastically with increasing the simulation numbers, but the simulation accuracy is improved as well. The more the simulation random numbers are, the more accurate statistical information can be extracted and reserved in the final output. In the fast estimator approach, times of original classical simulation are performed for extracting the statistical data, such as the nominal response value (μ), the standard deviation (σ), and these two parameters are related directly to the collecting database, the more simulation times (random numbers) are, the more accurate

the original database is. These two parameters (μ,σ) are used to generate an independent and identically distributed data (estimated response), this fast estimator is intended to achieve the simulation accuracy when reducing the simulation times by applying the Maximum Likelihood Estimation (MLE) to the original extracted data.

5.2 Fast simulation GUI

For the purpose of circuit design and development aid, the whole fast simulation methodology is implemented via *skill* language which enables it can be integrated in circuit design platform, such as Cadence. The GUI can help collecting the circuit netlist (pixel and testbench), the user defined variables, the top level signals, and it can help performing the sensor simulation in both matrix and single pixel level, and it can be help designer to study pixel matrix response variability caused by process parameter variation. The GUI can output the simulation results according to the simulation level, a voltage file for single pixel simulation or an image for matrix level simulation. A scalar data file which contains the time consumption, light intensity, pixel output voltage will be generated automatically after the simulation. The GUI is able to give out a performance comparison of various design specifications, it can help comparing the simulation results in voltage level and in final image level. The difference of two images which helps to examine and fix the low level transistor parameters (*w, l*) can be given out by GUI. A CDS technique option is integrated for identifying the FPN, and it helps to determine the reasonable integration time.

5.3 Simulating various pixel architectures

We show in this thesis that the fast method is able to study/simulate various pixel architectures, such as the typical 3T active pixel (3T-APS), 4T active pixel (4T-APS), 2.5T active pixel (2.5T-APS) and logarithmic pixel (log-APS). The characteristic of various pixel architectures is listed in Table 5. 1, the technical process for 3T-APS is simple and this pixel architecture gains a relative high Fill Factor among the various

pixel architectures. The 4T-APS is dedicated to achieve higher dynamic range with linear readout. The logarithmic APS maintains the high Fill Factor, and it increases the dynamic range with sacrificing pixel's linear response which brings the issue for signal readout and processing. The shared pixels architectures such as 2.5T, 1.75T, increase the Fill Factor and achieve higher resolution. They get a better trade-off between pixel performance, pixel size and matrix size, but a severe cross-talk is an issue needed to be solved.

Through this study, the 3T-APS is adopted in the all approaches and the other pixel architectures are used to verify the simulation methodology.

Table 5. 1. The characteristic of various CMOS pixels

Architectures	Advantages	Disadvantages
3T-APS	Simple and high FF	High noise level
4T-APS	High linear dynamic range	Low Fill Factor (FF)
2.5T-APS	High FF	Severe cross talk
Log-APS	High dynamic range	Non-linear readout

5.4 Perspectives

In the future work, more optical part could be integrated, such as the color filter array (CFA), which can be modeled and added in the simulation, thus, a color output image can be attained. In this thesis work, only photocurrent is set to the simulation parameter, later, more parameters should be considered, such as transistor size (w, l) and process parameter, for improving the simulation efficiency, the multiple dimensional LUT approach which aims at matching and mapping multiple design variables are considered. Based on this simulation methodology, the optimization method of meeting the image quality requirement and pixel size could be another perspective. The optimization could be able to meet the high level specification and requirement.

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Résumé en Français

Chapitre 1:

Ce premier chapitre introduit les concepts élémentaires et présente l'état de l'art des capteurs d'image de l'état solide. Un capteur d'image convertis l'énergie lumineuse, ou l'énergie des photons, dans une autre quantité mesurable: typiquement du courant ou du potentiel électrique. Pour les capteurs de l'état solide, il existe deux grandes classes: les Charge Coupled Devices (CCD, ou dispositif à charge couple) et les CMOS Image Sensors (CIS, pour ceux basé sur technologie CMOS). Grâce aux avances de la technologie CMOS et son faible coût de fabrication, cette dernière classe a gagne en performance ces derniers années et conquérir le marche. La première et la plus simple structure d'un pixel CIS est le pixel passif. Cette structure atteint le plus grand *fill factor* (FF, ou taux de remplissage) et la meilleure efficacité quantique. Cependant elle présente une faible sensibilité et des niveaux élèves de bruit. La structure de pixel actif (APS, Active Pixel Sensor), inventée ultérieurement, adresse le problème de bruit et améliore la performance globale du pixel. L'application de la technique nommée Correlated Double Sampling (CDS, ou double échantillonnage corrélée) supprime le bruit de type fixe. En aval du capteur se trouve un circuit de conversion analogique/numérique (ADC), responsable convertir la mesure de la quantité physique (dans le cas général un potentiel électrique) dans une valeur numérique. Les topologies de ADC les plus courantes (e.g. Slope Flash, SAR et Pipeline) sont introduites et décrites dans ce manuscrit.

La conception des tels systèmes d'acquisition d'image posent un vrai défi au niveau méthodologique du au grand écart entre la modélisation du phénomène physique et celle du système électronique. Par exemple, une camera numérique contient des lentilles, une matrice de pixels, un circuit de traitement, etc, ce qui démontre la nature multi physique de ce type de système. En effet, pour quantifier la performance et ainsi concevoir un capteur d'images CMOS, on doit recourir a des simulations a différents niveaux d'abstraction: au niveau du procède technologique (TCAD, Technology Computer Aided Design), de la performance électrique du pixel (ECAD) ou de l'ensemble du système sur puce. La simulation TCAD est utilisée pour le développement et l'optimisation de la structure des dispositifs semi-conducteurs. Elle emploi des principes élémentaires de la physique et permet une représentation très détaillée et fiable des caractéristiques du composant. Synopsys a annoncée que sont outil TCAD Sentaurus permettra de développer la prochaine génération de capteurs d'image. Néanmoins, la simulation TCAD est principalement utilise pour développer et analyser la structure d'un pixel isole.

Des plateformes EDA, comme Cadence ou Mentor Graphique permettent la simulation au niveau netlist en emploient des modèles SPICE pour les transistors. Cependant, la simulation d'une matrice de pixels de grande taille reste un défi. Dans ces cas, on doit chercher des solutions pour contrecarrer l'explosion du coût de calcul et des besoins en mémoire. Une alternative est d'utiliser un langage de modélisation de plus haut niveau pour remplacer le modèle SPICE du pixel. Néanmoins, il est difficile de l'intégrer dans un environnement de conception classique, et le problème du coût de calcul n'est pas résolu.

Dans l'autre extrême, il est possible d'inclure le comportement du pixel au niveau algorithmique. Cela permet d'analyser la performance de l'ensemble du système. Par contre, cela ne permet pas de prendre en compte l'impact des paramètres physiques, ce qui est un facteur clé dans la conception analogique. Pour trouver un meilleur compromis entre coût de calcul et précision de la simulation, on doit explorer des nouvelles approches pour la simulation au niveau électrique et les intégrer dans un environnement de conception classique. Cette thèse propose une telle approche pour

étudier la performance système en fonction des paramètres de bas niveaux (e.g. dimensions de transistors) et aussi analyser les effets de la variabilité sur la réponse du capteur (e.g. le bruit de type Fixed Pattern Noise).

Chapitre 2:

Conception d'un pixel, composants et paramètres clés

La tension de seuil du transistor MOSFET est la tension entre grille et source au moment où le canal de conduction commence à se former entre drain et source. La valeur de la tension de seuil est sensible aux variations du procède CMOS et peut dégrader la performance du pixel (e.g. en induisant du bruit dans la matrice de pixels). Ce paramètre est pourtant critique quand on s'intéresse a l'étude du pixel soumis à la variation des paramètres.

Défis dans la simulation d'une matrice de pixels

Dans une architecture 3T-APS, il existent trois transistors et une photodiode. Pour une matrice de 256x256 pixels, cela résulte en 196608 transistors et 65536 photodiodes. Pour vérifier la performance de la matrice, un simulateur SPICE doit résoudre 130k équations. Cela peut devenir prohibitif en temps de calcul. Par exemple, une matrice 512x512 a nécessité plusieurs jours dans une machine Intel Xeon 2.4GHz avec 4GB RAM. Cela est du (1) à la complexité du modèle BSIM utilisé pour représenter chaque transistors et (2) à la taille de la matrice, qui détermine directement le temps de calcul.

Solution et méthodologie proposée

Pour surmonter le problème du temps de calcul dans un environnement de simulation classique, nous proposons une méthodologie de simulation rapide intégrée dans la plateforme Cadence. La nouvelle méthodologie est complètement implémentée en langage SKILL, le langage de script spécifique aux outils Cadence. SKILL permet d'éteindre et de customiser l'environnement de simulation de base.

La méthode proposée combine la simulation SPICE avec un algorithme de modélisation de haut niveau. Elle vise particulièrement à résoudre le problème de la simulation de très grandes netlist. Le principe est de effectuer un jeu limité de simulations SPICE en amont et ainsi extraire des informations clés qui sont passées à l'algorithme de modélisation. Cela permet de construire un modèle de haut niveau pour accélérer la simulation système. Il est possible ainsi de réduire drastiquement le temps de calcul tout en gardant une haute précision.

Précision numérique

Quand on néglige les effets de couplage entre les pixels voisins, cela équivaut à considérer les pixels comme étant isolés. Cela simplifie l'analyse, puisque tout pixel partage le même modèle de simulation. Quand on considère ces effets de couplage, la première composante est la capacité parasite de colonne, i.e. celle qui résulte de la connexion de chaque pixel dans une colonne de la matrice. Nous considérons cet effet en ajoutant une capacité équivalente au modèle de simulation.

Au delà de la capacité du nodal de sortie des MOSFETS, la capacitance parasite lié au routage a aussi son effet sur la capacité totale de la colonne. Pour prendre en compte cet effet, nous avons mis en place une structure spécifique où un pixel est place au centre et entourée par 8 ou 24 autres pixels. Cela permet d'extraire la capacitance parasite pour le cas d'une matrice 3x3 et 25x25.

Look Up Table (LUT)

Le grand avantage de l'approche LUT comme méthode de simulation accélérée est de construire une relation directe entre les stimuli d'entrée et le résultat. La table des stimuli est construite en échantillonnant toute la gamme d'intensité lumineuse et, par conséquence, la table de résultats couvre tous les possibles valeurs de tension en sortie. La granularité de l'échantillonnage est déterminée par le niveau de précision souhaitée. En utilisant ces deux tables, la valeur de tension de sortie est obtenue sans faire recours à la simulation. Il suffit de chercher la table d'entrée pour l'intensité lumineuse souhaitée et reporter l'index sur la table de tensions de sortie.

Tension de sortie du pixel et acquisition de l’image

La tension en sortie du pixel est transférée au convertisseur analogique/numérique. La numérisation de l’ensemble de pixels compose l’image. Trois méthodes de génération de l’image sont utilisés afin d’étudier la performance électrique de la matrice en fonction des paramètres de conception. Ces méthodes sont: *relative*, *directe* et *absolute*. La ma méthode directe permet visualiser la tension de sortie du pixel en fonction de la tension d’alimentation et ainsi étudier la gamme dynamique du capteur. La méthode absolue utilise le niveaux de reset du pixel comme référence et reflets la vrai amplitude du signal optique.

Variabilité de la réponse des matrices de pixel d'un capteur d'image CMOS

Dans un capteur d'image CMOS, la tension de seuil des transistors affect directement la plage de tension de sortie des pixels. De plus, l'épaisseur de l'oxide de la grille détermine la capacité de la grille qui est lié au gain. Ces paramètres sont importants pour la conception d'un pixel.

En technologie CMOS, la variabilité affects de manière significative les performances des transistors et par conséquent les performances du capteur d'image à réaliser. Pour étudier les dégradations de performance et identifier les non uniformités de la réponse des pixels (Fixed pattern noise), les simulations Monte Carlo sont utilisés car elles ont la capacité de résoudre des problèmes stochastiques qui prennent en compte un grand nombre de degrés de liberté. Pour de petit circuit, ce type de simulation est suffisante en termes de précision et de temps d'exécution, mais pour un très grand circuit intégré, ce simulation coûterons beaucoup terme de temps et même plusieurs jours dans certain cas.

Pour adapter les simulations Monte Carlo et pour éviter des temps simulations trop longues, une méthode de simulation rapide est ici proposé et étudié. Cette méthode combine une simulation Monte Carlo et un algorithme de haut niveau. La

simulation Monte Carlo reçoit les données originelles qui sont ensuite utilisées par l'algorithme de haut niveau pour prédire le résultat de simulation finale.

Interface graphique de simulation rapide

L'interface graphique de simulation rapide permet de faire interface l'environnement de développement classique et l'algorithme de haut niveau. Il est en charge du transfert bidirectionnel des données numériques entre ces deux parties. Son interface est composée d'un menu, d'option de configuration, de sélection et d'édition. Le développeur de haut niveau peut ainsi charger des images dans le l'environnement de simulation, pour réaliser une simulation au niveau pixel ou au niveau matrice et pour étudier la réponse de la matrice en incluant la variabilité. Dans l'interface, le résultat de simulation est observé visuellement sous la forme d'une image qui est utilisé pour identifier l'impact de l'ajustement des paramètres de bas niveau.

Conclusion

Les très grands circuits présentant une structure en forme de grille régulière comme les capteurs d'image CMOS ou les mémoires montrent les limites des méthodes de simulation actuel. La méthodologie de simulation rapide est étudié comme étant une approche alternative pour accélérer la simulation de très grands circuits permettant de réduire le besoin de recourir à l'utilisation de machine de calcul ultra performante ou de simulateur très rapide. Cela permet de réduire les besoins en termes de ressource système.

La méthodologie de simulation prenant en compte la variabilité est développée avec pour objectif :

1. Aider à comprendre les caractéristiques des capteurs d'images CMOS
2. Pouvoir faire des simulations de grandes matrices en un temps acceptable
3. Aider à l'identifier les effets de la variabilité sur la réponse du capteur

Chapitre 3

- **Réponse nominale d'un 3T-APS**

Trois cas sont considérés pour la simulation du capteur:

1. Le cas d'un pixel sans “cap”, ce qui signifie qu'aucune capacité des pixels voisins n’est considéré.
2. Le cas considérant seulement les capacités des pixels voisins à l'état “OFF”. Elles sont extraites et ajoutées à une capacité équivalente dans la simulation.
3. Le cas où toutes les capacités parasites résultant du layout sous extraites et ajoutées à la simulation.

L'environnement de simulation est paramétré avec le design kit 0,35um CMOS de AMS. Les résultats de simulation montrent qu'il y a une différence de 0,1mV (pour les très grandes matrices) avec ou sans les capacités voisines. Cette différence n'altère pas l'image finale résultant de la structure du pixel sélectionnée. Cependant, une différence de tension est observée quand on considère toutes les capacités parasites. Dans ce cas, une différence est visible sur l'image finale.

- **Réponse d'un 3T-APS incluant la variabilité**

En considérant la variabilité, la réponse de la matrice sous une intensité de lumière uniforme varie d'un pixel à l'autre (dans une zone de 750mV à 820 mV et avec une photo courant de 10pA). La variation de la réponse dans les images de sorties finales (format RAW et absolue) n'est pas visible, mais elle devient évidente quand on applique la méthode relative d'agrandissement dans les données de sortie de la simulation. La réponse uniforme attendue prend alors la forme d'une distribution gaussienne.

- **Performance de la méthode de la simulation rapide**

La méthode de simulation rapide est dédié à l'amélioration des performances de simulation et à maintenir la précision dans un environnement de développement classique. En considérant la méthode de simulation rapide via l'approche LUT (le pire cas), on trouve une erreur de un niveau de gris dans l'image final d'un 3T-APS. Ce qui est équivalent à 0,4% de la plage d'intensité (256 niveaux de gris). Du point de vue de l'image de sortie, cette différence est acceptable.

Le temps d'exécution de la méthode classique est largement amélioré par la méthode de simulation rapide qui montre augmentation réduite du temps d'exécution avec l'augmentation de la taille de la matrice qui est simulée.

Les tests montrent que la méthode de simulation rapide permet d'accélérer 350 fois la simulation d'une matrice de 256x256.

Conclusion

Dans ce chapitre, la méthode de simulation est présenté et validé avec les aspects suivants :

1. Le dépassement de mémoire de la méthode classique est résolu.
2. La capacité de simulation est étendue de 60 fois.
3. Il est prouvé que la méthode de simulation rapide améliore largement l'efficacité de la simulation alors que la précision est maintenue. (e.g. un niveau de gris d'erreur pour une accélération de 350 fois)
4. Cette méthode est particulièrement efficace pour simuler des matrices 3T-APS.

Chapitre 4

Dans ce chapitre, pour valider les capacités et démontrer les performances de la méthodologie de simulation rapide, plusieurs cases étendues sont étudiées avec différentes architectures de pixel et différentes technologies. Les pixels 3T-APS, log-3T-APS, 4T-APS, et l'architecture en pixel partagé 2.5T-APS sont étudiés. La technologie émergente des transistors CNTFET à double grille est utilisée pour construire le model 3T-APS qui est simulé avec la méthodologie de simulation rapide. Pour l’architecture 4T - APS, et comparer avec la méthode classique, la méthodologie de simulation rapide atteint une erreur absolue de 1,1mV (0,2% en erreur relative). Cela prouve que la méthodologie de simulation rapide est fiable pour simuler de l'architecture 4T-APS.

Quand on applique la méthodologie de simulation rapide au capteur d'image log-3T-APS, on trouve également une erreur absolue dans la plage du 1mV.

La fiabilité de la méthodologie de simulation rapide est prouvée pour le log-3T-APS. Le modèle Verilog-A du CNTFET à double grille a été sélectionné pour ce travail de thèse et il est utilisé pour construire la structure du modèle 3T-APS. Toutes les simulations d'erreur sont dans la plage du millivolt et la capacité de la méthode à couvrir différentes technologies est également prouvée.

Dans le chapitre 4, différentes architectures de pixel sont simulées et testées. Après avoir comparer différent résultats de simulation, il peut être conclus que la méthode de simulation rapide via l'approche LUT est stable et accéléré la simulation d'un capteur d'image. Il doit être précisé que cette nouvelle méthodologie peut supporter d'autres architectures de pixel (5T, 7T). Dans ce travail, la lecture du schéma est effectué en mode obturateur déroulant. Le mode obturateur global peut également être supporté mais n'est pas utilisé. Comparé à la méthode classique, le temps d'exécution dans l'approche LUT augmente doucement avec le nombre de pixel

Dans l'approche LUT, et comparé à la méthode classique, l'extensibilité est grandement améliorée les erreurs de dépassement de mémoire sont éliminés. Les résultats de simulation de tous les cas montrent que l'approche LUT est fiable. Elle peut être potentiellement utilisé pour résoudre les problèmes de consommation de mémoire et les délais de traitement nécessaire dans les simulations paramétriques.

Chapitre 5

Dans ce chapitre, les conclusions, les discussions et les perspectives sont présentées. Ce travail de thèse a commencé avec une revue de l'état de l'art des capteurs d'image, avec en particuliers les évolutions technologiques et le développement des architectures de pixels. Pour aider au développement de capteur d'image CMOS, de nombreux outils de CAO ont déjà été développer mais les méthodes de simulations classique font face au défi lié aux circuits ultra large. Le compromis entre les long temps de simulation et leur précision est le problème majeur. Cette thèse est dédiée à l'exploration de nouvelles approches de résolution de ce problème.

Conclusion :

1. Dans cette thèse, une méthode de simulation rapide basée sur les LUT est développé et combiné avec une interface graphique.
2. Les stimuli sont pris en compte dans l'environnement de simulation en lisant une image qui présente une scène virtuelle. La simulation est réalisée au niveau transistor et à un niveau d'abstraction plus élevé.
3. Cette nouvelle approche tire avantage de la grande précision des simulations SPICE et de la vitesse élevée d'un haut niveau de gestion des données.
4. Cette méthode rapide obtient de bons résultats comparés à la méthode classique dans la vérification des performances de sortie d'un capteur au niveau électrique et sa capacité est prouvé pour différentes architectures de pixel et différentes technologies.
5. La taille de la simulation est grandement améliorée jusqu'à des pixels de 15 méga pixels.

Possibilité:

1. Les futurs développements peuvent prendre en compte les paramètres optiques comme les grilles de filtre couleurs qui peuvent être modélisés comme un motif de type Bayer et ajouter à la simulation. Par conséquent, une image de sortie en couleur peut-être obtenue.
2. Ce travail ne considère que la photo courante comme paramètres de simulations. Néanmoins, d'autres paramètres comme les dimensions des transistors (W et L) et les paramètres de process devraient être prisent en compte.
3. Pour continuer à améliorer les performances de simulation, l'approche de LUT multidimensionnel des LUT qui vise à faire correspondre et de cartographier plusieurs variables de conception devrait également être développée.
4. En se basant sur la méthodologie de simulation, la méthode d’optimisation pour améliorer la qualité de l'image et la taille de pixel est une autre possibilité.

Fast Scalable and Variability Aware CMOS Image Sensor Simulation Methodology

Abstract:

The resolution of CMOS image sensor is becoming higher and higher, while for identifying its performance, designers need to do a series of simulations, and this work consumes large CPU time in classical design environment. This thesis titled "Fast Scalable and Variability Aware CMOS Image Sensor Simulation Methodology" is dedicated to explore a new simulation methodology for improving the simulation capability. This simulation methodology is used to study the image sensor performance versus low level design parameter, such as transistor size and process variability. The simulation methodology achieves error less than 0.4% on 3T-APS architecture. The methodology is tested in various pixel architectures, and it is used in simulating image sensor with 15 million pixels, the simulation capability is improved 64 times and time consumption is reduced from days to minutes. The potential application includes simulating array-based circuit, such as memory circuit matrix simulation.

Key words: CMOS Image Sensor, Pixel matrix simulation, Variability, Fast simulation, SKILL, Cadence ADE.

Méthode de simulation rapide de capteur d'image CMOS prenant en compte les paramètres d'extensibilité et de variabilité

Résumé:

L’amélioration de la résolution de ces capteurs implique la nécessité pour les concepteurs de réaliser des séries de simulation de plus en plus longue dans le but de caractériser leurs performances, et ces simulations qui génèrent des résultats difficiles à analyser requièrent de très grandes ressources de calcul ainsi qu’une grande quantité de mémoire. Cette thèse intitulée "Méthode de simulation rapide de capteur d'image CMOS prenant en compte les paramètres d'extensibilité et de variabilité" explore une nouvelle méthodologie de simulation pour améliorer les capacités de traitement actuelles. La méthode qui a été développée est utilisée pour étudier et comparer les performances d’un capteur d’images avec les paramètres de bas niveau de conception de tels circuits ; par exemple la taille des transistors ainsi que la variabilité. La méthodologie obtient l'erreur de sortie moins de 0,4% sur le capteur d’image de style APS-3T. La méthode a été testée avec diverses architectures de pixel, et elle a permis de simuler un capteur d'image de 15 millions de pixels. La vitesse de simulation est améliorée 64 fois, passant de plusieurs jours à plusieurs minutes. La simulation des circuits présentant une structure en matrice comme les mémoires est une autre application potentielle de ce type de méthodologie.

Mots clés: Capteur d’image CMOS, simulation de matrice de pixel, variabilité, Simulation rapide, SKILL, Cadence ADE.