Analysis of an ESD failure mechanism on a SiC MESFET

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Abstract

Efficient energy management become more and more crucial with increasing energy resource scarcity. Power electronic will play a major role in this field and thus require innovations like using wide band gap semiconductor to build power devices. SiC, GaN, diamond based device are currently more or less mature and will sooner or later require investigations on their reliability to allow their wide adoption. In this work we investigate on a SiC-MESFET ElectroStatic-Discharge (ESD) robustness. Surprisingly the ESD robustness is rather low and found to be related to both current non-uniformity and a quite unexpected parasitic NPN bipolar transistor triggering. The outcome of this study allows to propose a simple solution to improve ESD robustness of such devices.

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Introduction

Thanks to major advancements in manufacturing technology, silicon carbide's (SiC) power devices are making their way into large market applications which, in turn, has motivated research into application related performance, robustness and reliability.

Robust design of power systems for such applications requires characterization of the devices under a number of stressful operational conditions. With temperature, ElectroStatique Discharges (ESD) stress is one of the main sources of failure for electronic devices that need to be addressed) [1, 2].

We have characterized and analyzed ESD robustness of a SiC MESFET device that is designed as a driver for Power devices working in harsh environment (temperature>300°C).

1.1. Structure Studied

We studied a lateral SiC MESFET designed to operate as a power-device driver working in harsh environment at high temperature. This MESFET has fast switching capability and low conduction losses.

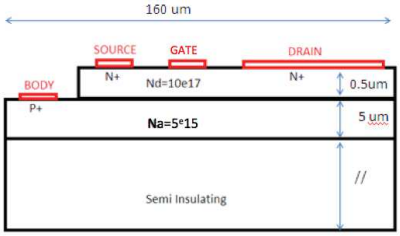

Figure 1: Schematic cross section of the studied SiC MESFET.

It is a normally ON device with conventional drain, source and gate electrodes (Figure 1). A Body electrode has been added [3].

1.2. Results of TLP test

Transmission Line Pulse (TLP) test with 100 ns pulse length was carried out on the device. At 300°K, a positive pulse was applied to the drain while the source is grounded. Gate and Body electrode were kept floating. The pulse amplitude is progressively increased during the test. Hence the drain voltage (Vd) is increased until failure. Both voltage (Vd) and current (Id) are measured during the pulses. Averaged I and V values on the flat part of the pulse are used to extract a quasi-static Id-Vd curve. DC leakage is measured in between each pulse to monitor the device degradation.

During the device test the pulse amplitude was increased by step of 10V. From zero to 300V on the drain the device carries current in its saturated conduction mode. Even if the gate and body electrode have floating potential TCAD simulation shows that their potential is near three volt. Above 300 V a snapback occurs, voltage drops down to 40V and the device carry a large current that is fatal for the device.

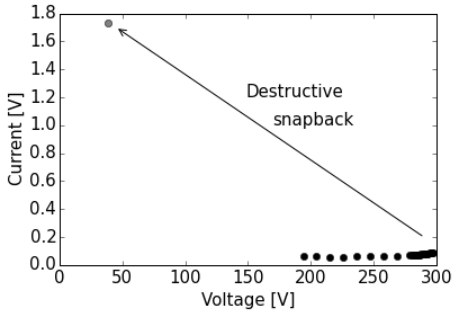

Figure 2: Id-Vd curve; Snapback occurs at a voltage above 300V during TLP Test.

After the device snapback hasoccurred a damaged region is observed at the bottom right corner of device (Circled on Figure 3). The metal of the drain pad is melted at this corner and we also observe a hole in the SiC material.

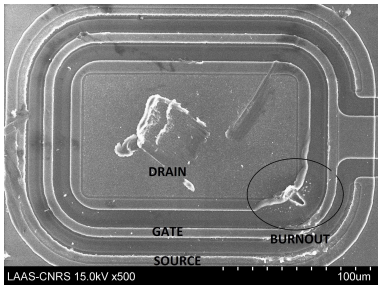

Figure 3: Damage observed at the corner of the SiC MESFET after TLP Stress (SEM photography).

At atmospheric pressure, SiC sublimate at 2700°C (no liquid phase) this might explain the observed hole in the SiC material while no SiC residue are observed.

FIB cross section on the defect location are on going to obtain additional clues on the device failure mechanism. Additional measurement results with gate and body grounded will be presented as well in the final paper.

Finally, given the TLP results, we can evaluate this SIC-MESFET HBM robustness to be lower than 290V. With JEDEC classification, it corresponds to class 1A device, i.e. a very low robustness device requiring very careful handling.

2. Physical understanding

TCAD electrothermal simulation with Sentaurus[6] could allow better understanding of the MESFET device behaviour during TLP and HBM stress [4,5].

The simulations are carried out using a bi-dimensional model of the MESFET calibrated on regular static electrical characteristics at 300K. The TLP pulse is applied on the drain while source is grounded. Gate and body terminal are kept floating by connecting them through a 1MOhm resistance to ground. During the flat portions of the pulses the gate and body terminal voltage are around 3V.

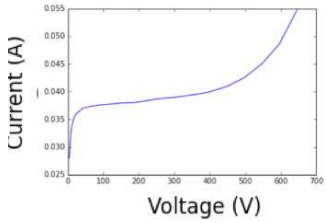

Figure 4: Id-Vd curve, above 600 Volts breakdown voltage observed with the 2D model of the MESFET simulating drain-source TLP Id(Vd) characteristic with floating gate and substrate.

The same current level is found in comparison with experimental TLP test. However, the breakdown voltage is simulated to be above 600V (Figure 4), whereas it is measured lower than 300V in experiments.

A first explanation is that the bi-dimensional simulation of this MESFET does not take into account the corner of the device where the drain junction is cylindrical. A lower breakdown voltage is indeed simulated using a bi-dimensional cylindrical model representing the corners of the device.

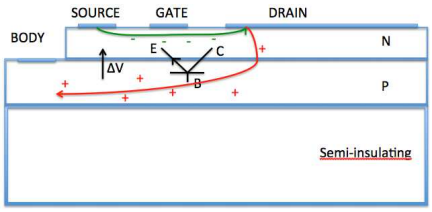

Figure 5: carrier mobility behavior during high voltage in MESFET SiC

Another explanation can be proposed understanding the physical behaviour of the device with the help of the TCAD simulations. Indeed a quite unexpected NPN bipolar transistor appears to triggers on (Figure 5). Between 400V and 500V, electric field is high enough to produce avalanche generation and lead to a hole current flowing in the P body. This current leads to a voltage drop in the body due to its serial resistance. When the avalanche current is high enough, the B-E junction of a parasitic NPN can be forward biased and then NPN is turned ON. The MESFET gets into snapback mode, which leads to a current localization and device deterioration.

Given the detailed new physical understanding, solutions might be proposed to delay the triggering of the parasitic NPN and hence to increase the robustness of the device.

One quite straightforward solution would be to increase the radius of the corners in order to increase the breakdown voltage of the drain at the corner. Indeed, this will proportionally increase the HBM robustness of the device, as it will be demonstrated by simulation in the final paper.

Conclusion

The ESD robustness of the tested MESFET device is quite surprisingly low. This low robustness is related to both current non-uniformity and a quite unexpected parasitic NPN bipolar transistor triggering. The outcome of this study allows proposing a simple solution by properly designing the corner of the device to increase their local breakdown voltage. Reaching class-1B JEDEC-Classification (resistant to 500V) robustness-level seems to be quite achievable. However further investigation would be required to achieve higher ESD robustness specification often required for arch environment.

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