High-temperature characterization of advanced strained nMuGFETs

Rachida Talmat, S. Put, N. Collaert, A. Mercha, C. Claeys, Wei Guo

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R. Talmat[1,2], S. Put[3,4,5], N. Collaert[3], A. Mercha[3], C. Claeys[3,4], W. Guo[1], B. Cretu[1], A.Benfdila[2], J-M. Routoure[1], R. Carin[1] and E. Simoen[3]

[1]GREYC, UMR 6072 CNRS/ENSICAEN/University of Caen, 6 Bd Marechal Juin, Caen, France
[2] GRMNT, Mouloud Mammeri University of Tizi-Ouzou, Algeria
[3]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
[4]E.E. Dept. KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium
[5]SCK·CEN, The Belgian Nuclear Research Center, Boeretang 200, B-2400 Mol, Belgium

1. Abstract

DC measurements at high temperature of n-channel triple-gate transistors with 25 nm fin-width and 65 nm fin-height, high-k dielectric and metal gate for strained and unstrained substrates are investigated. The variations of the main transistor parameters with temperature are analyzed from room temperature up to 200°C.

2. Introduction

One of the assets of Silicon-on-Insulator (SOI) CMOS technologies is their robust high-temperature behaviour which makes them attractive for e.g. automotive applications. This potential has recently also been explored for Multiple-Gate FinFET devices on SOI substrates [1-3]. At the same time, strain engineering is one of the enabling techniques to boost the device performance further along the ITRS roadmap [4,5]. Performance enhancement can be obtained by the use of substrate induced (or biaxial) strained material (sSOI) or the implementation of strained contact etch stop layers (CESL), which leads to uniaxial process induced strain in the channel. This work presents the impact of the temperature on the DC performance from room temperature up to 200°C for standard and strained nFinFETs.

3. Experimental

The n-channel transistors have been fabricated on standard and strained-SOI (sSOI) substrates. Additional splits utilize tensile stress induced by CESL across the gate stack and Selective Epitaxial Growth (SEG) for source and drain regions. The different wafers are indicated by SOI, sSOI, sSOI+tensile CESL, sSOI+SEG+tensile CESL. The gate stack consists of a high-k dielectric (HfSiON) on top of 1 nm interfacial SiO_2, resulting in an equivalent oxide thickness (EOT) of 1.5 nm. The gate metal consists of 10 nm TiN covered by 100 nm polysilicon. Further processing details can be found in [6]. The dimensions of the tested devices were: gate length from L= 40 nm up to 1 µm, fin width W_{fin}= 25 nm and 5 fins in parallel. The results in this work are focused on the transistors with gate length L = 60 nm. The temperature variation of the basic parameters, such as threshold voltage (V_{th}), subthreshold swing (S), mobility (µ) and parasitic series resistance (R_{SD}) are extracted using the Y function method ($Y=I_D/(g_m)^{1/2}$) [7], by comparing devices with different strain under linear operation (V_D = 50 mV).

4. Results and discussion

The reduction of the threshold voltage V_{th} with the temperature increase for the unstrained and strained nFinFETs is shown in Figure 1. The slopes of the characteristics do not differ much for the different types of nFinFETs. The threshold voltage decreases with increasing temperature at a rate of -0.57 mV/°C in the standard nFinFET. Similar values are obtained for strained nFinFET except for sSOI + tCESL (-0.45 mV/°C). The threshold voltage decrease with temperature was relied to Fermi potential reduction with temperature [1-3]. The values of the $\Delta\Phi_F/\Delta T$ are about 1 mV/°C (N_A= 10^{15} cm^{-3}). This disagreement could be explained by using analytical model of the threshold voltage as in [1,2] where the threshold voltage is described as a function of the potential surface and the flatband voltage, the top conduction of the triple-gate FinFET were neglected due to the narrow W_{Fin} under study. This analytical model predicts values in agreement with the experimental results.

Regarding the subthreshold swing, the variation versus temperature can be seen in Figure 2. The obtained values are higher than the ideal one due to charge sharing effect. For temperatures higher than 175°C, one can note a slight increase of the subthreshold swing in strained nFinFETs. This increase could be explained by the gate-to-surface potential coupling and a not ideal exponential dependence of the inversion charge on the surface potential [2].

The drift – diffusion mobility for all studied devices and temperatures investigated were obtained by substracting from the extracted low field mobility (μ_0) the ballistic mobility (μ_{bal}) using the procedure of [8]. The backscattering coefficient r values at 25° and 200°C are shown in Table 1. One can observe that the ballistic transport is more important in strained devices at room temperature. The drift – diffusion mobility variation with temperature is showed in Figure 3. A good correlation with the $T^{-1.5}$ variation law (solid lines in Fig. 3) can be observed. This suggests that for studied devices, the dominating phenomenon is the phonon scattering mechanism. One of the problems related with

the use of narrow nFinFETs is the increase of the parasitic series resistance. The values of R_{SD} at 25°C and the rate $\Delta R_{SD}/\Delta T$ are showed in Table 1. The series resistance is quite similar in SOI and sSOI+ tCESL devices, but we notice a higher variation rate for the latter. Compared with standard devices, the introduction of SEG allows to obtain approximately 70% reduction of R_{SD} for all temperatures investigated.

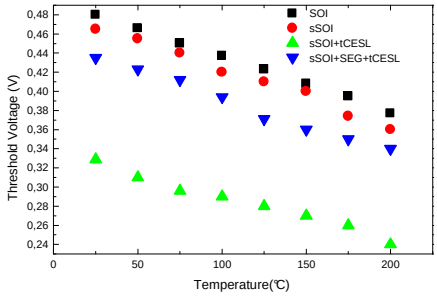

Fig.1: *Extracted threshold voltage (V_{DS}=50mV) as a function of the temperature.*

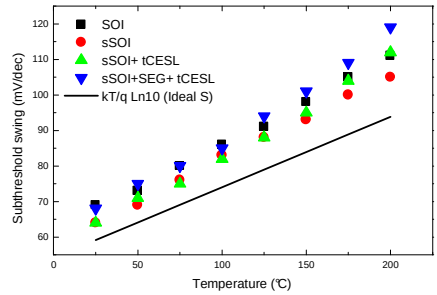

Fig.2: *Extracted subthreshold swing (V_{DS}=50mV) as a function of the temperature.*

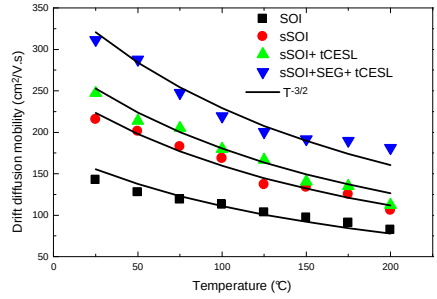

Fig.3: *Drift-diffusion electron mobility (V_{DS}=50mV) as a function of the temperature.*

As the temperature increases, the off-current is increased. The variation of I_{off} is dominated by the degradation in subthreshold swing and by the reduction of the threshold voltage. The values of the estimated energy activation E_a, extracted from the slope of log (I_{off}) versus the temperature and the values of the I_{off} current at room temperature are shown in Table 1. One can notice that the I_{off} current is higher in strained devices.
Finally, in designing digital and analog circuits for high temperature application, it is desirable to bias the circuits at a point where the drain current remains constant as the temperature varies, this point is known as the zero temperature coefficient biasing point; V_{ZTC} are values of V_{GS} at which the reduction of V_{th} is counter balanced by the reduction of the mobility, and as a result, the value of the drain current remains constant as the temperature varies. For gate voltages lower than V_{ZTC}, the decrease of V_{th} is dominant and the drain current increases with temperature while for gate voltages higher than V_{ZTC}, the mobility degradation predominates and the drain current decreases with temperature [9]. The values of V_{ZTC} for studied devices are reported in Table 1. One can note a reduction of the V_{ZTC} between the standard and strained devices.

	SOI	sSOI	sSOI+ tCESL	sSOI+ SEG+ tCESL
$\Delta V_{th}/\Delta T$ (mV/°C)	-0.57	-0.60	-0.45	-0.57
$\Delta S/\Delta T$(mV/ dec/°)	0.24	0.28	0.2→0.28	0.2→0.4
R_{SD} @ 25°C(Ω)	367	256	355	116
$\Delta R_{SD}/\Delta T$ (Ω/°C)	0.64	0.72	1.4	0.31
I_{off} @ 25°C (A)	$1\ 10^{-12}$	$1.8\ 10^{-12}$	$1.4\ 10^{-10}$	$1.1\ 10^{-11}$
E_a (eV)	0.23	0.23	0.17	0.20
V_{ZTC} (V)	0.71	0.58	0.37	0.59
r @25°C	0.94	0.86	0.84	0.80
r @200°C	0.98	0.97	0.97	0.95

Table 1: *Summary of the extracted transistor parameters for the studied devices.*

5. Conclusions

In this paper, the main electrical parameters for strained and unstrained nFinFETs were investigated from 25 up to 200°C. One noticed that the lowest threshold voltage shift is obtained for sSOI+tCESL devices; while the highest mobility is obtained for the sSOI+SEG+CESL. The ZTC voltage was pointed out and the lowest is found in strained nFinFETs. The use of strain techniques prevents the degradation of these parameters at high temperatures; the strain can counteract the high temperatures effect. These devices seem to be less sensitive to the temperature variation than the standard nFinFETs, indicating an additional benefit of strain engineering.

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