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Graphical method for the Phase noise Optimization applied to a 6 -GHz fully integrated NMOS differential LC VCO

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Abstract— This paper describes the design and the optimization in terms of phase noise of a fully integrated NMOS Voltage Controlled Oscillator (VCO) using a 0.25 μm BICMOS SiGe process. A three-dimensional phase noise analysis diagram and a graphical optimization approach is presented to optimize the phase noise of the VCO while satisfying design constraints such as tank amplitude, power dissipation, tuning range and start up conditions. At 2.5 V power supply voltage, the optimized VCO features a simulated phase noise of -118 dBc/Hz at 1 MHz frequency offset from a 6.12 GHz carrier. The VCO is tuned from 6.1 GHz to 7.9 GHz with a tuning voltage varying from 0 to 2.5 V, and a power dissipation of only 7.4 mW.

Keywords: *phase noise, Optimization, graphical method, VCO, NMOS technology.*

I. INTRODUCTION

Voltage controlled oscillators are essential building blocks of modern RF transceivers architectures. The VCO performances in terms of tuning range, power dissipation and phase noise determine most of the basic performances of a complete transceiver.

Due to the evolution of wireless communication systems, the design of integrated oscillators implies many challenges to circuit designers as it involves multiple variables. To overcome these challenges and optimize the phase noise of the oscillator, an accurate graphical optimization method is presented in [1] by Hajimiri & al. The process of this optimization is performed through the minimization of phase noise while satisfying all different design constraints such as startup conditions, tank amplitude and tuning range. Nevertheless, in [1], the bias current of the VCO, which is an important parameter for the phase noise optimization, is chosen arbitrary to the maximum current allowed by the specifications. This choice does not constitute an optimal optimization strategy. Indeed, let us remind that a simplified and widely used phase noise model separates the amplitude

behavior versus the bias current into two operation modes named voltage and current-limited regimes [2]. Thus the phase noise decreases in the first regime until it reaches the stable transition point located between the two regimes. So, the desired bias current point for the optimum phase noise and power consumption performances is located at the intersection of these two regimes.

Due to this considerations, the aim of this work is first, to determine the optimum bias current of the VCO using a three dimensional phase noise representation using a parametric analysis and second, starting from this optimal current, to use the graphical optimization method proposed in [1] and adapted to our 6 GHz NMOS only LC VCO architecture.

This paper is organized as follow. In section II, the cross coupled LC-VCO architecture chosen as application example for the proposed method is described. The graphical optimization method is also presented in detail for the chosen LC VCO architecture. Section III presents the simulation results of the optimized VCO in order to show the accuracy of the presented method. Finally, we give some concluding remarks in section IV.

II. VCO TOPOLOGY AND OPTIMIZATION APPROACH

A. VCO topology

Figure 1 shows the simplified VCO schematic used and based on the well-known cross-coupled NMOS differential topology. The LC tank is made of a symmetric center-tapped inductor and a differentially tuned varactor. The cross connected NMOS differential pair provides the negative resistance to compensate for the tank losses. The tail current source is a simple NMOS current mirror. In these conditions, the width and the length of the NMOS tail transistor must be increased to reduce the flicker noise which lowers significantly the close-in phase noise of the VCO [3]. A tail

capacitor C_T is used to attenuate both the high-frequency noise component of the tail current and the voltage variations on the tail node. This latter effect results in more symmetric waveforms and smaller harmonic distortion in LC-VCO outputs [4], [5].

B. Optimization approach

For this LC VCO architecture, the adopted optimization methodology which is based on the following steps is detailed:

- Specifications definition ;
- VCO model determination ;
- Optimum Bias conditions determination ;
- Phase noise graphical optimization ;
- Phase noise estimation using the optimum parameter found in the previous step.

In the following sub sections, the process of modelization and optimization of the LC-VCO topology is analyzed step by step.

1) VCO model determination

The equivalent circuit model of the oscillator is shown in Figure 2, where the broken line in the middle represents either the common mode or ground.

The frequently appearing parameters in this model are the tank loss g_{tank} , effective negative conductance g_{active} , tank inductance L_{tank} and tank capacitance C_{tank} given by:

$$2g_{\text{tank}} = g_d + g_v + g_L \quad (1)$$

$$2g_{\text{active}} = g_m \quad (2)$$

$$L_{\text{tank}} = 2L \quad (3)$$

$$2C_{\text{tank}} = 4C_{gd} + C_{db} + C_{gs} + C_L + C_V \quad (4)$$

a) Inductor model

As explained in section II-A, the inductor used is a symmetric center-tapped inductor. The global inductance value is about 1.2 nH and the differential quality factor is equal to 19 at 6 GHz. Let us note here that we consider that the inductor has been designed in order to obtain a maximum Q factor at 6 GHz. Using the model in [1], the effective parallel equivalent conductance of the inductor, g_L , is given by:

$$g_L = \frac{1}{R_p} + \frac{R_s}{(\omega L)^2} \quad (5)$$

where R_p and R_s represents the parasitical elements of the inductance.

b) Varactor model

The varactor used is based on NMOS transistors in inversion mode. We modelize the varactor as an ideal capacitance in series with a resistor R_v . The varactor quality factor is equal to 200 at 6 GHz, and the effective parallel equivalent varactor conductance, g_v , is then given by:

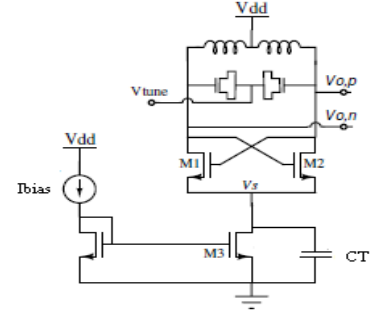


Figure 1. Conventional VCO schematic

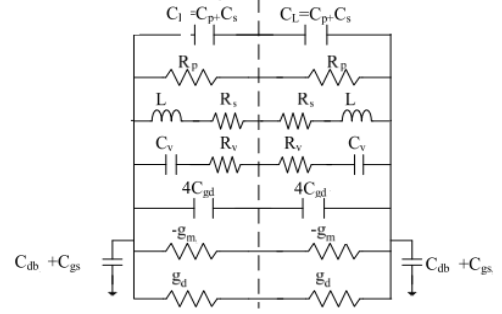


Figure 2. Equivalent oscillator model

$$g_v = \frac{1}{R_v} = \frac{C_v \omega}{Q_v} \quad (6)$$

Where R_v is the MOS varactor parasitic serie resistance and Q_v represent the quality factor of the varactor.

c) Transistor model

The very useful NMOS transistor analytical model described in [6] is used for the graphical optimization and visualization of design constraints.

2) Optimum Bias conditions determination

Let us remind that the aim of this part is to determine the optimum bias current of the VCO for a minimum phase noise. To do so, a program developed in Maple in which we exploit the following expression describing the phase noise model (pn) of the VCO is used [7].

$$Pn(f_{\text{offset}}) = \left[\frac{1}{16\pi^2 f_{\text{offset}}^2} \cdot \frac{L^2 (2\pi f_0)^2}{V_{\text{tank}}^2} \right] [2kT(g_L + g_v + g_d)] \quad (7)$$

Where k is the Boltzmann constant, T is the temperature, V_{tank} is the oscillation amplitude, f_0 is the oscillation frequency, f_{offset} is the offset frequency from the carrier, γ is equal to 5/2 and g_d is the output conductance.

So, for each value of I_{bias} the tank voltage and the phase noise are calculated using equation 8. Figure 3 shows a three-dimensional representation of the LC-VCO phase noise. In this figure, the (x-y) plane describes the bias condition of the VCO and the z-axis corresponds to phase noise prediction. Thus, an initial optimal bias condition for which the phase noise is estimated to be at the minimum is selected. The

coordinate of this minimum for this 6-GHz VCO is given by: $I_{bias}=3.4$ mA and P_n (1 MHz) = -116.71 dBc/Hz.

3) Phase noise graphical optimization

Using the previous model for the chosen LC VCO, the process of optimization consists in the representation of the design constraints in the variable plane; therefore let us, first of all, define the design variables.

a) Design variables

There are many initial design variables associated with the specified VCO: the geometric parameters of the on-chip spiral inductors, the MOS transistors dimensions (W_n and L_n) and the maximum and minimum values of the varactors ($C_{v,max}$ and $C_{v,min}$). The number of these design variables can be reduced as explained in the following: First, the geometric parameters of the inductors are fixed in order to obtain a high inductor quality factor as mentioned previously. Second, the channel length L_n is set to the minimum allowed by the process technology for maximum transition frequency (F_T) and transconductance g_m . Third, the ratio $C_{v,max}/C_{v,min}$ is maximum. Therefore, the varactor introduces only one design variable ($C_{v,max}$).

Finally, we reduce the number to only two design variables, the transistors width W_n and the maximal varactor capacitance $C_{v,max}$ which will be referred to C in the following. Consequently, the design constraints will be represented in the (W_n, C) plane.

a) Design constraints

The main goal of the optimization is to minimize the phase noise of the VCO while satisfying all design constraints such as tank amplitude, startup condition, power dissipation and tuning range.

In these conditions, and in order to ensure a large enough voltage swing, the tank amplitude is required to be larger than $V_{tank,min}$ so that:

$$V_{tank} = \frac{I_{bias}}{g_{tank,max}} \geq V_{tank,min} \quad (8)$$

Where $V_{tank,min}$ is chosen to be equal to 1 V and $g_{tank,max}$ is the maximum tank conductance.

Moreover, the startup condition is fixed by:

$$g_{active} \geq \sigma_{min} g_{tank,max} \quad (9)$$

Where $\sigma_{min} = 3$ is the small-signal loop gain, g_{active} and $g_{tank,max}$ are the active and the tank conductance respectively.

Finally, the oscillation tuning range is limited by two values depending on the center frequency ω_0 , so that:

$$L_{tank} C_{tank,min} \leq \frac{1}{\omega_{max}^2} \quad (10)$$

$$L_{tank} C_{tank,max} \geq \frac{1}{\omega_{min}^2} \quad (11)$$

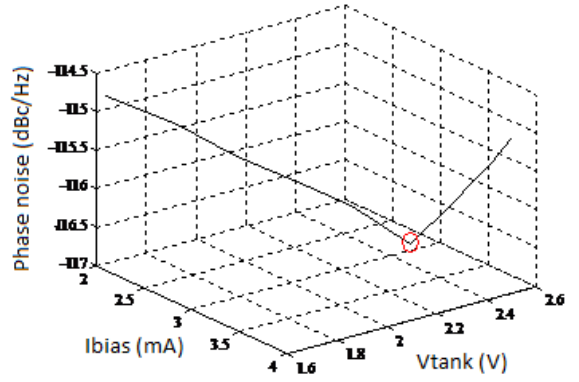


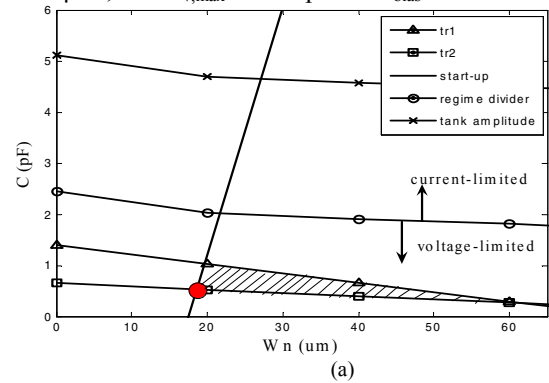
Figure 3. Calculated phase noise versus V_{tank} and I_{bias}

The design constraints given by (8) to (11) are expressed and formulated as functions of W_n and C variables, and a new program was developed in Maple which allows to calculate, for each value of the transistor width, the varactor capacitance C so that the design constraints are fulfilled. The associated curves are shown in figure 4, using the initial I_{bias} condition already determined.

The line representing the limit of the tank amplitude is obtained using (8), the region below this line corresponds to V_{tank} greater than 1 V. The tr_1 and tr_2 lines define the maximum and minimum frequency of the tuning range, and are obtained respectively from (10) and (11). In this case, a tuning range of 25% with a center frequency of 6 GHz is obtained if a design point (a couple C, W_n) lies between the tr_1 line and the tr_2 line. The startup line is obtained from (9). Thus, to ensure proper startup of the VCO, the point must be located on the right-hand side of the startup line for $\sigma_{min} = 3$. Finally the regime divider line presents the limit of the voltage-limited regime and the current-limited regime.

The region with shadow in figure 4(a) satisfies all the design constraints and represents a set of feasible design points. The optimum point is defined by the intersection of the startup line and tr_2 line since this point corresponds to the low parasitic capacitances values. However we can notice that the optimum point is located in the voltage limited regime (below the regime divider). Therefore, the design suffers from waste of power. As a consequence, the bias current must be reduced until the optimum is located on the regime divider line. In this case, figure 4(b) shows the optimum design with $I_{bias} = 2.95$ mA for which no further action is necessary.

Consequently, the obtained optimum point is defined by: $W_n = 18 \mu m$; $C = C_{v,max} = 0.55$ pF and $I_{bias} = 2.95$ mA.



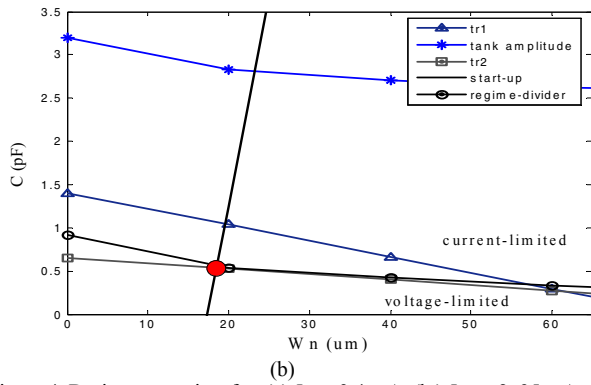


Figure 4. Design constraints for: (a) $I_{bias} = 3.4$ mA; (b) $I_{bias} = 2.95$ mA

III. SIMULATION RESULTS

In this section, simulations using spectre RF Software is performed on the VCO designed using the presented optimization process.

At the beginning, one must verify that the I_{bias} point found through the optimization method is effectively the optimum current for minimum phase noise. To do so, the phase noise at 1 MHz frequency offset versus the bias current is plotted. The curve in figure 5 shows that the phase noise decreases in the first regime and it reaches the stable transition point located between the voltage and current limited regimes. This transition point is defined by a current whose value is located between 2.9 mA and 3.1 mA.

Furthermore, as shown in figure 6, the VCO can be tuned from 6.1 GHz to 7.9 GHz, and shows a phase noise of -118 dBc/Hz at 1 MHz frequency offset from a 6.12 GHz carrier, and a current consumption of 2.95 mA from a 2.5 V power supply.

In order to show the accuracy of the presented graphical optimization method, table I presents a comparison between theoretical (presented method) and simulation (Spectre RF software) results. Let us note that, the phase noise value is calculated using (7) after optimization. As we can see, a good agreement can be found between theoretical and simulated results.

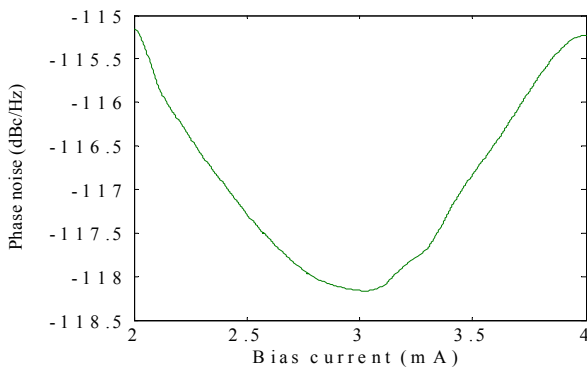


Figure 5. Phase noise versus the bias current.

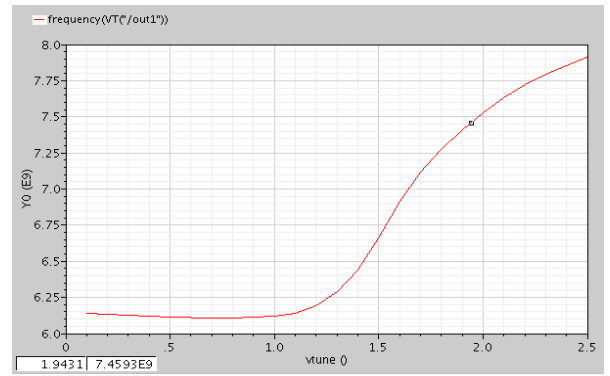


Figure 6. Tuning characteristic of the LC-NMOS VCO

TABLE I: COMPARISON BETWEEN THEORETICAL AND SIMULATION RESULTS

	Graphical Optimization	Spectre RF Software
Frequency (GHz)	6	6.12
Tuning range (%)	25	25.9
Phase noise(dBc/Hz)	-118.44	-118

IV. CONCLUSION

This paper describes a graphical method for the phase noise optimization of LC voltage controlled oscillators. It is based on a three-dimensional phase noise analysis diagram to visualize the different design constraints such as tank amplitude, startup condition and tuning range. It is shown that the design process to minimize phase noise and to obtain optimum bias condition through this illustration and using graphical optimization presents simulated accurate and systematic results. The optimized VCO achieves a phase noise of -118 dBc/Hz at 1 MHz frequency offset for a 6.12 GHz carrier frequency.

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