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Abstract

In this paper, we describe an original method for determining the optimal operating point of the active part (transistor) of an LC oscillator leading to the minimum phase noise for given specifications in terms of power consumption, oscillation frequency and for given devices (i.e., transistor and resonator). The key point of the proposed method is based on the use of a proper *LC* oscillator architecture providing a fixed loaded quality factor for different operating points of the active part within the oscillator. The feedback network of this architecture is made of an *LC* resonator with coupling transformers. In these conditions, we show that it is possible to easily change the operating point of the amplifier, through the determination of the turns ratio of those transformers, and observe its effect on phase noise without modifying the loaded quality factor of the resonator. The optimal operating point for minimum phase noise is then extracted from nonlinear simulations. Once this optimal behaviour of the active part known and by associating the previous *LC* resonator, a design of an *LC* oscillator or VCO with an optimal phase noise becomes possible. The conclusions of the presented simulation results have been widely used to design and implement a fully integrated, *LC* differential VCO on a 0.35 μm BiCMOS SiGe process.

Key words: class-C, cyclostationary noise, *LC* resonator, operating point, power added, oscillators.

1. Introduction

Mobile communication system evolution demands continuous efforts toward the improvement of Radio-Frequency (RF) circuit performances. Concerning the oscillators and voltage-controlled oscillators (VCOs), the phase noise requirements are even more stringent. Indeed, the carrier rejection and the transmission quality of any systems depend on the phase noise of the signals applied to the modulator. Furthermore, from the designer point of view, pressure is growing as design time is getting shorter and shorter. In this context, it seems to be very interesting to know rapidly if the specification required in terms of phase noise and consumption are consistent with the technology provided. Due to these considerations, this paper describes a method for determining the optimal operating point of the active part of an *LC* oscillator leading to the minimum phase noise for given specifications in terms of power consumption, oscillation frequency and for given devices.

Section 2 is a brief review of some of the existing phase noise models giving important key points for phase noise minimization. Section 3 presents the theoretical analysis of the chosen *LC* oscillator topology and concludes with the sequence to be carried out to obtain the oscillation at a frequency f_0 for a given operating point of the amplifier. Section 4 describes the simulations leading to the optimal operating point of a SiGe HBT *LC* oscillator. Finally, section 5 presents the design and implementation of a fully integrated differential VCO optimized in phase noise using the conclusions of the previous section.

2. Brief review of phase noise existing models

The model proposed in [1], known as the Leeson-Cutler phase noise model, predicts a phase noise spectral density in the $\frac{1}{f^2}$ region of the spectrum of

$$S_\Phi(\Delta f) = 10 \cdot \log\left[\frac{2FkT}{P_S}\left(\frac{f_0}{2Q\Delta f}\right)^2\right] \quad (1)$$

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where F is the noise factor, k is the Boltzmann's constant, T is the absolute temperature, P_S is the average power dissipated in the resistive part of the resonator, f_0 is the oscillation frequency, Q is the loaded quality factor of the resonator and Δf is the frequency offset from the carrier.

Although the result of simplifying assumptions, this model offers important key points for reduction of phase noise in the oscillators. Indeed, it can be concluded, from (1), that the loaded quality factor of the resonator needs to be maximized in order to reduce phase noise in the $\frac{1}{f^2}$ region of the spectrum. In the same way, for a given loaded quality factor Q, the phase noise spectral density will be all the more low that the resonator dissipated power P_S will be high. However, the dissipated power in the resonator corresponds to the difference between the output and input powers of the active part under oscillation conditions. This difference represents, in fact, the added power of the oscillator amplifier.

Thus, for a given loaded quality factor, the transistor must be operated under oscillation conditions as close as possible to its maximum added power state [2]. However, equation (1) predicts the phase noise in the $\frac{1}{f^2}$ region mainly due to the tank parallel resistor of the resonator. The Leeson model additionally introduce the factor F as a multiplicative factor, to take into account for the phase noise due to the active part, but without knowing precisely what it depends on and how to reduce it. Unfortunately, the noise generated by the transistor is usually the main phase noise contributor in oscillators and VCOs. Thus, the simplifying assumptions of this model have been revised particularly by Hajimiri and Lee [3, 4], who explicitly showed the time-varying nature of phase noise generation.

The key concept in their linear, time-varying (LTV) phase noise theory is the Impulse Sensitivity Function (ISF), whose calculation leads to a very accurate prediction of phase noise due to stationary and cyclostationary noise sources in the oscillator. Thus, according to the ISF theory, the total single sideband phase noise spectral density in the $\frac{1}{f^2}$ region of the spectrum due to one current noise source on one node of the circuit at an offset frequency $\Delta\omega$ is given by [3]

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{\overline{i_n^2}/\Delta f \cdot \Gamma_{rms}^2}{2 \cdot q_{max}^2 \cdot \Delta\omega^2}\right) \qquad (2)$$

where $\overline{i_n^2}/\Delta f$ is the power spectral density of the current noise source in question, Γ_{rms}^2 is the rms value of the Impulse Sensitivity Function (ISF) associated with the noise source considered previously, and q_{max} is the maximum charge swing across the current noise source.

As mentioned earlier, the transistor mainly contribute to the overall phase noise in an oscillator and the dominant noise sources of the transistor are often cyclostationary. For instance, the collector current shot noise of a bipolar transistor and the channel noise of a MOS device are cyclostationary [5, 6]. Fortunately, the LTV model developed by Hajimiri and Lee is able to accommodate a cyclostationary noise source with ease. Indeed, considering that a white cyclostationary noise current can be written as the product of a white stationary process and a deterministic periodic function $\alpha(x)$, also called the Noise-Modulating Function (NMF) [4, 7, 8], strongly correlated with currents waveforms of the oscillator, the cyclostationary noise can be treated as a stationary noise by introducing the effective ISF given by [3].

$$\Gamma_{eff}(x) = \Gamma(x) \cdot \alpha(x) \qquad (3)$$

Thus, the phase noise due to the cyclostationary current noise source is expressed by (2) replacing Γ_{rms}^2 by $\Gamma_{eff,\,rms}^2$. Consequently, $\Gamma_{eff,\,rms}$ needs to be minimized in order to reduce phase noise significantly. In other words, the transistor would remain off almost all of the time, waking up periodically to deliver an impulse of current at the signal peak of the oscillator, where the ISF ($\Gamma(x)$) has its minimum value, i.e., when the noise to phase noise conversion is at a minimum [5, 9]. Thus, the transistor must be operated in class-C under oscillation conditions in order to reduce significantly the phase noise due to the cyclostationary noise sources.

As a conclusion, the Leeson-Cutler phase noise model states that, the phase noise spectral density will be all the more low that the resonator dissipated power (P_S) will be high and thus that the transistor must be operated under oscillation conditions as close as possible to its maximum added power state [2] for a given loaded quality factor, whereas, according to the phase noise model of Hajimiri and Lee [3], the transistor must be operated in class-C under oscillation conditions in order to reduce significantly the phase noise due to the cyclostationnary noise sources.

Consequently, from the designer point of view, a critical choice, depending partly on the technology used, between those two operating points needs to be done in order to reduce phase noise. Thus, to easily determine this optimal operating point of the active part for given specifications in terms of power consumption, oscillation frequency and for given devices (i.e., transistor and resonator) and loaded quality factor, the right *LC* oscil-

lator topology must be chosen. Indeed, this latter must provide a fixed loaded quality factor for different operating point of the active part within the oscillator. Such a topology is analyzed in detail in the next section.

3. LC oscillator theoretical analysis

A typical oscillator topology essentially consists of a transistor limiting amplifier and a frequency-determining element or feedback network. In our case, the transistor used is a SiGe HBT and the feedback network is made of an *LC* resonator as shown in Fig. 1

Such an oscillator topology can be modeled by a quasi-linear representation in the frequency domain as shown in Fig. 2(b) [2, 10]. Let us note that this linearization implies that the non linear elements are approximated by their equivalent values calculated for the oscillation amplitude at the oscillation frequency f_0 [10, 11].

3.1. Amplifier theoretical analysis

Let us consider the simplified linear representation of the amplifier shown in Fig. 2(a) where G_{in}, C_{in}, G_{out}, C_{out} represent respectively the transistor input and output conductance and capacitance, G_m is the conventional positive large signal transconductance of the transistor and L_{in}, L_{out}, n_{in}, n_{out} are matching elements. Let us now suppose that, for a given bias point, the amplifier is large signal matched to $G_0 = 1/R_0$ ($R_0 = 50\ \Omega$).

Then, the matching elements cited above can be calculated using the following relationships :

$$\begin{cases} L_{in} = \dfrac{1}{B_{in} \cdot \omega_0} \\ n_{in} = \dfrac{1}{\sqrt{R_0 G_{in}}} \end{cases} \qquad \begin{cases} L_{out} = \dfrac{1}{B_{out} \cdot \omega_0} \\ n_{out} = \sqrt{R_0 G_{in}} \end{cases} \tag{4}$$

Where B_{in} and B_{out} are respectively the susceptance of the input and output admittance of the transistor. Once these matching conditions are achieved, the amplifier can be described by the circuit shown in Fig. 2(b) with the following expression for G_{meq} :

$$G_{meq} = G_m \cdot \frac{n_{in}}{n_{out}} \tag{5}$$

This equivalent transconductance G_{meq} can also be expressed in terms of maximum power gain of the amplifier. Indeed, once the 50 Ω matching conditions are achieved, the maximum power gain is given by

$$G_{Pmax} = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{2} \cdot G_0 \cdot V_{out}^2}{\frac{1}{2} \cdot G_0 \cdot V_{in}^2}$$

where

$$V_{out} = -\frac{1}{2 \cdot G_0} \cdot G_{meq} \cdot V_{in}$$

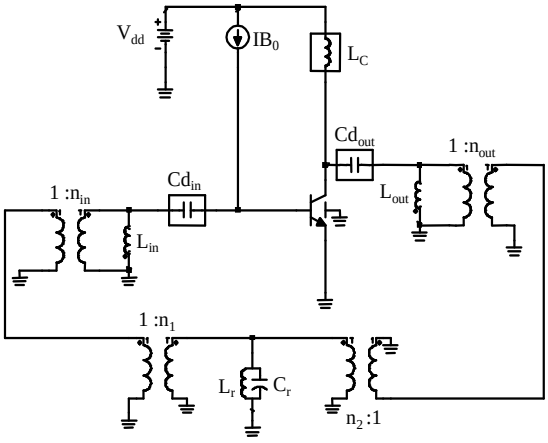

Figure 1: Oscillator schematic

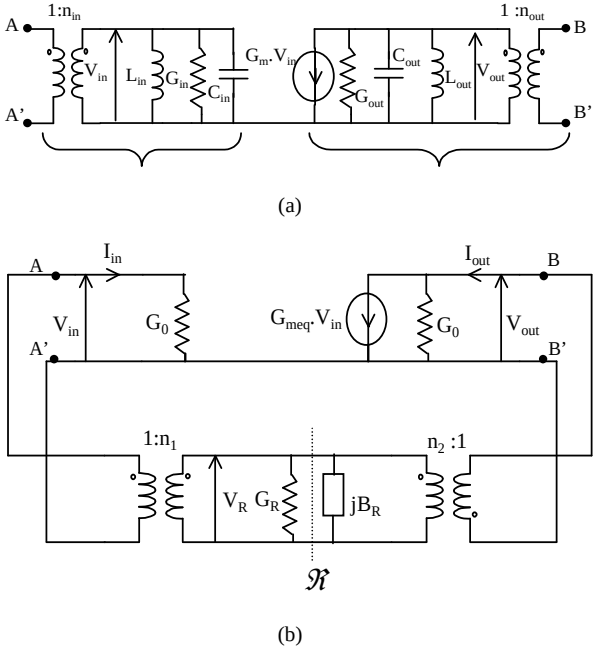

Figure 2: Simplified linear representation of the 50 Ω matched amplifier (a) and the oscillator (b)

so that

$$G_{meq} = 2 \cdot G_0 \cdot \sqrt{\frac{P_{out}}{P_{in}}} \tag{6}$$

As we will see in the next subsection, the determination of G_{meq} will allow us to determine directly the coupling coefficients n_1 and n_2 (Fig. 2(b)).

3.2. Oscillator theoretical analysis

Let us remind that the oscillator topology chosen can be represented by the schematic shown in Fig.2(b) where the resonator is modeled by a G_R conductance and a B_R susceptance with coupling coefficients n_1 and n_2. In these conditions, the equivalent schematic of the oscillator in the resonator plane ($\mathscr{R}$) is given in Fig.3.

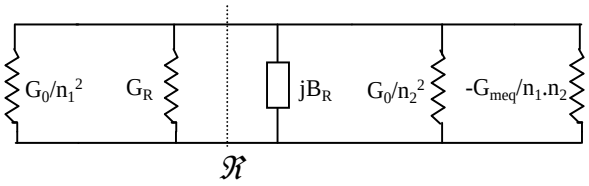

Figure 3: Equivalent schematic of the oscillator in the $\mathscr{R}$-plane

Thus, the oscillation conditions can be written, at the oscillation frequency f_0, as

$$G_R + \frac{G_0}{{n_1}^2} + \frac{G_0}{{n_2}^2} - \frac{G_{meq}}{n_1 \cdot n_2} = 0 \tag{7}$$

Note that we consider here that the oscillation frequency f_0 is the same as the resonant frequency of the *LC* resonator so that $B_R = 0$. Furthermore, for a given operating point of the amplifier and once the 50 Ω matching conditions are achieved, the feedback network must present a 50 Ω load at the amplifier output at the oscillation frequency f_0. This case is illustrated on Fig.4.

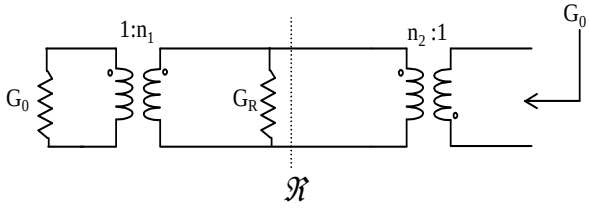

Figure 4: 50 Ω matching condition of the feedback network at f_0

Thus, we have

$$G_0 = \left(\frac{G_0}{{n_1}^2} + G_R \right) \cdot {n_2}^2$$

and then

$$G_R = G_0 \cdot \left(\frac{1}{{n_2}^2} - \frac{1}{{n_1}^2} \right) \tag{8}$$

Combining (7) and (8) now yields

$$n_1 \cdot (2 n_1 G_0 - n_2 G_{meq}) = 0$$

giving only one physical solution for n_1:

$$n_1 = \frac{n_2 G_{meq}}{2 G_0} \tag{9}$$

Now, substituting (9) into (8) gives

$$ {n_2}^2 = \frac{G_0}{G_R} \cdot \left(1 - \frac{4 {G_0}^2}{{G_{meq}}^2} \right) \tag{10}$$

where G_{meq} is calculated, for a given operating point of the amplifier, using (6).

Once these coupling coefficients are calculated, let us determine the loaded quality factor of the resonator. To do this, the conventional rigorous expression of the loaded *Q*-factor calculated at a particular point in the circuit is reminded [10] :

$$Q = \omega_0 \cdot \frac{E_{stored}}{P_{diss}} = \frac{\omega_0}{2G} \cdot \left. \frac{\partial B}{\partial \omega} \right|_{\omega_0} \tag{11}$$

where ω_0 is the resonant pulsation, E_{stored} is the average energy stored in the circuit, P_{diss} is the average dissipated power, G and $\left. \frac{\partial B}{\partial \omega} \right|_{\omega_0}$ are respectively the positive conductance and the susceptance slope at the considered point of the circuit.

In the $\mathscr{R}$-plane, the susceptance slope is perfectly known and is equal to $2C$ in the case of a parallel *RLC* resonator. Thus, the susceptance slope in the $\mathscr{R}$-plane is constant and we call it B so that

$$B = \left. \frac{\partial B_R}{\partial \omega} \right|_{\omega_0} \tag{12}$$

where B_R is the susceptance in the $\mathscr{R}$-plane.

Let us now determine the positive conductance G in the $\mathscr{R}$-plane. According to Fig.4, we have

$$G = G_R + \frac{G_0}{{n_1}^2} + \frac{G_0}{{n_2}^2} \tag{13}$$

Substituting (9) and (10) into (13) yields

$$G = \frac{2 G_R {G_{meq}}^2}{{G_{meq}}^2 - 4 {G_0}^2} \tag{14}$$

Then, from (11), (12) and (14), the loaded *Q*-factor of the *LC* resonator can be written as

$$Q = \frac{\omega_0}{\frac{4G_R {G_{meq}}^2}{{G_{meq}}^2 - 4{G_0}^2}} \cdot B \tag{15}$$

Furthermore, the expression of the unloaded quality factor of the *LC* resonator is the following

$$Q_0 = \frac{\omega_0}{2G_R} \cdot B \tag{16}$$

So that, the loaded *Q*-factor can be expressed in terms of Q_0 as follows

$$Q = \frac{Q_0}{2} \cdot \left(1 - \frac{4{G_0}^2}{{G_{meq}}^2}\right) \tag{17}$$

It can be concluded, from (17), that the loaded *Q*-factor of the resonator is close to $Q_0/2$ for high values of G_{meq} (i.e. for high amplifier power gain). In practice, we will see in the next section that this is always the case when a large voltage swing across the resonator need to be achieved in order to reduce phase noise.

Consequently, according to the theoretical analysis performed here, we can say that the chosen oscillator topology allow to maintain a fixed loaded quality factor especially for a large voltage swing across the resonator. Furthermore, the operating point of the amplifier can be easily controlled under oscillation conditions through the determination of the coupling coefficients n_1 and n_2.

3.3. Successive steps to obtain the oscillation at f_0 for a given operating point of the amplifier

We can now state the sequence to be carried out to obtain the oscillation at a frequency f_0 for a given operating point of the amplifier:

1. Choose a transistor and an *LC* resonator (depending on the technology provided);
2. Get the desired amplifier operating point for a given transistor bias point using a nonlinear simulation;
3. Calculate the 50 Ω matching elements using (4);
4. Calculate the equivalent transconductance G_{meq} using (6);
5. Calculate the coupling coefficients n_1 and n_2 using (9) and (10).

From that point, the phase noise spectrum of the oscillator can be determined, using a nonlinear simulation, for the amplifier operating point chosen. Thus, the next section presents the phase noise simulations of the *LC* oscillator of Fig. 1 for three cases of the active part operating point in order to determine the optimal one.

4. Determination of the optimal operating point of a SiGe HBT *LC* oscillator

4.1. Simulation conditions

As mentionned previously, the oscillator schematic used for the simulations on Agilent's software ADS is shown on Fig. 1. The active part is made of a SiGe HBT with double base contact and an emitter area of 20.32 μm^2 from a 0.35 μm BiCMOS SiGe process. L_c is an ideal *DC* feed, Cd_{in} and Cd_{out} are ideal *DC* blocks, IB_0 is a bias current source which will allow to fix the mean collector current IC_0 of the transistor and L_{in}, L_{out}, n_{in}, n_{out} are the matching elements whose expressions are given in (4).

The feedback network is made of an *LC* resonator with the coupling coefficients n_1 and n_2 calculated using (9) and (10). The value of L_r and C_r are fixed so that the oscillator will oscillate at 1.9 *GHz*. In this case, the inductance value L_r is 1.3 *nH* with an associated *Q* factor of 12 at 1.9 *GHz* and the capacitance value C_r is 5.4 *pF* with an associated *Q* factor of 60 at 1.9 *GHz*. Note that the quality factor of the passive elements constituting the resonator are those provided by the 0.35 μm BiCMOS SiGe technology used. From the above data, the conductance G_R of the resonator can be calculated. Indeed, considering the simplified serial representation of an inductor shown in Fig. 5(a), the quality factor can be expressed as follows

$$Q = \frac{L_s \omega}{r_s} \tag{18}$$

where ω is the working pulsation, L_s the inductance and r_s the serial resistance used to model the inductor losses. Furthermore, let us note that the inductor can also be represented by its equivalent parallel model as shown in Fig. 5(b) where L_p and R_p can be expressed as

$$\left.\begin{array}{r} L_p \simeq L_s \\ \\ R_p \simeq r_s \cdot Q^2 \end{array}\right\} \quad \text{for} \quad Q^2 \gg 1 \tag{19}$$

Thus, for a *Q* factor of 12 at 1.9 *GHz*, we have $R_p = 186.2\ \Omega$ and $L_p = 1.3\ nH$.

In the same way, the capacitor can be represented by its equivalent simplified parallel representation as shown in Fig. 6. The expression of the quality factor is thus the following

$$Q = R_c \cdot C \cdot \omega \tag{20}$$

where ω is the working pulsation, *C* the capacitance and R_c the parallel resistance used to model the capacitor

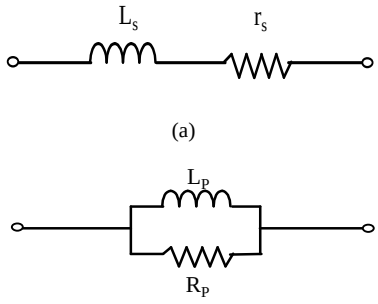

Figure 5: Simplified serial (a) and parallel (b) representation of an inductor

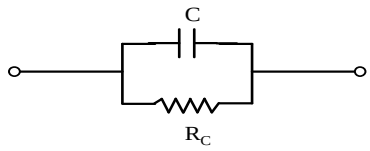

Figure 6: Simplified parallel representation of a capacitor

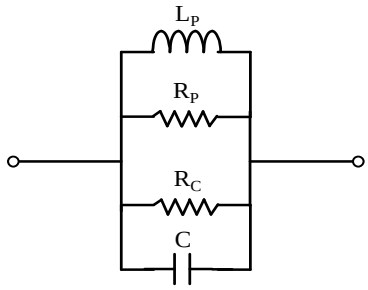

Figure 7: Parallel representation of the *LC* resonator

losses. So, for a capacitor Q factor of 60 at 1.9 GHz, we have $R_c = 930.7\ \Omega$.

Thus, the equivalent parallel representation of the entire resonator is given on Fig. 7 and the conductance G_R of the resonator can be calculated as follows

$$G_R = \frac{R_p + R_c}{R_p R_c} = 6.4\ mS \tag{21}$$

Once the presentation of the oscillator circuit done, let us remind the conditions in which the simulations will be performed. They are summarized in table 1.

4.2. Influence of the amplifier operating point

In this sub-section, three cases of the amplifier operating point will be compared in order to verify their influence on phase noise simulated performances. The first one corresponds to the operating point where the amplifier deliver a low added power. The second one corresponds to a maximum added power operating point and finally, the third one corresponds to a class-*C* operation. Then, the phase noise spectrum of the oscillator will be compared in each case. Let us note that each operating point is obtained using a nonlinear simulation of the amplifier alone with Agilent's software ADS which allows to determine the input (Y_{in}) and output (Y_{out}) admittance of the transistor.

Table 1: Simulation conditions

Transistor	SiGe HBT
L_r	1.3 nH
C_r	5.4 pF
Supply voltage V_{dd}	2.7 V
Current consumption IC_0	3.5 mA
Oscillation frequency	1.9 GHz

For the first case which corresponds to a low power added operating point, we have an input power of 0.0032 mW, an output power of 2.91 mW and thus, an added power of 2.9 mW. In these conditions, the input and output admittance values are

$$Y_{in} = 0.0006307 + j0.0162263\ \Omega^{-1}$$
$$Y_{out} = -0.0058175 + j0.0024814\ \Omega^{-1}$$

Using the above values, the sequence, detailed in subsection 3.3, to obtain the oscillation at 1.9 GHz for a low added power state of the amplifier can be carried out. So, the 50 Ω matching elements calculation using (4) gives $L_{in} = 5.16\ nH$, $L_{out} = 33.7\ nH$, $n_{in} = 5.52$ and $n_{out} = 0.54$. The calculation of the equivalent transconductance G_{meq} using (6) gives 1.19 S and with the value of the conductance G_R given by (21), we obtain, for the coupling coefficients: $n_1 = 52.3$ and $n_2 = 1.76$ using (9) and (10). Let us note that, with those values, the loaded Q-factor of the resonator is $0.998 \times (Q_0/2)$ using (17).

For the second case in which the amplifier is optimized for a maximum added power operation, we have an input power of 0.0093 mW, an output power of 4.58 mW and an added power of 4.57 mW. The input and output admittance values are

$$Y_{in} = 0.0003229 + j0.0115764\ \Omega^{-1}$$
$$Y_{out} = -0.0040698 + j0.0024695\ \Omega^{-1}$$

Thus, $L_{in} = 7.23\ nH$, $L_{out} = 33.9\ nH$, $n_{in} = 7.7$, $n_{out} = 0.45$ and $G_{meq} = 0.869\ S$. This leads to $n_1 = 38.22$ and

$n_2 = 1.76$. Furthermore, with those values, the loaded Q-factor of the resonator is $0.997 \times (Q_0/2)$.

Finally, for the third case in which the amplifier is optimized for a class-C operation, we have an input power of $0.062\ mW$, an output power of $4.25\ mW$ and an added power of $4.18\ mW$ giving :

$$Y_{in} = 0.0000863 + j0.051851\ \Omega^{-1}$$

$$Y_{out} = -0.0037768 + j0.0029948\ \Omega^{-1}$$

Thus, $L_{in} = 16.15\ nH$, $L_{out} = 27.97\ nH$, $n_{in} = 14.99$, $n_{out} = 0.4345$, $G_{meq} = 0.326\ S$, $n_1 = 14.23$ and $n_2 = 1.748$. The loaded Q-factor of the resonator is $0.985 \times (Q_0/2)$ in this case.

It is important to note, at that point, that the maximum loaded Q-factor variation between the first and the third case is only 1.3 %. Thus, as expected from (17), we can say that the chosen oscillator topology allow to maintain a fixed loaded quality factor (close to $Q_0/2$) for the three cases of the amplifier operating point studied.

The phase noise spectrum, for each case of the amplifier operating point, simulated with Agilent's software ADS is then plotted on Fig. 8.

It is clear that the added power is an important parameter for oscillator phase noise reduction since the phase noise of the simulated oscillator at 1 MHz frequency offset is improved by almost 3 dB compared to the low added power case. So, we can conclude that, for a given loaded quality factor, the phase noise spectral density is all the more low that the resonator dissipated power, and thus the added power of the oscillator amplifier, is high.

However, for the LC oscillator simulated here, the crucial parameter is not the added power but the class-C operation of the amplifier as clearly shown in Fig. 8. Indeed, for a class-C operation of the amplifier, the phase noise at 1 MHz frequency offset is improved by 5.5 dB compared to the maximum added power case. As mentioned in section 2, this result can be explained using the linear, time-varying (LTV) phase noise theory of Hajimiri and Lee [3, 4]. Indeed, let us remind that the dominant noise sources of the transistor are often cyclostationary and to reduce significantly phase noise due to the cyclostationary noise sources, the transistor would remain off almost all of the time, waking up periodically to deliver an impulse of current at the minimum of the collector voltage, where the ISF $(\Gamma(x))$ is close to zero. Furthermore, this impulse of current must be as short as possible so that the rms value of the effective ISF is small. This leads to a class-C operation of the active part within the oscillator. To corroborate this, the collector current and collector voltage of the SiGe HBT used are plotted on Fig. 9 for the three different matching conditions. Furthermore, Fig. 10 shows the normalized collector current, the approximated ISF calculated on the collector of the transistor and given by [3]

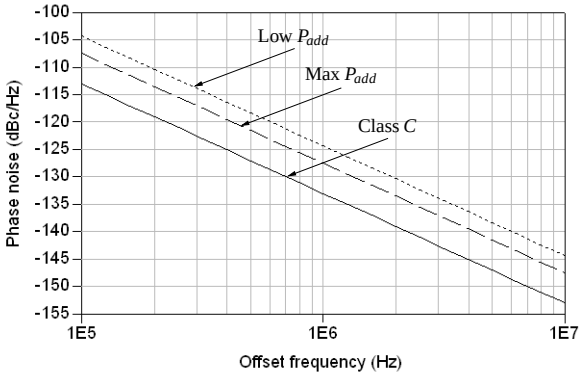

Figure 8: Phase noise spectrum of the oscillator

$$\Gamma_i(x) = \frac{f_i'(x)}{\left(f'_{max}\right)^2} \tag{22}$$

where $\Gamma_i(x)$ is the ISF at node i, $f_i'(x)$ is the derivative of the waveform on node i and $\left(f'_{max}\right)^2$ is the squared maximum value of this derivative function, and the effective ISF which can be approximated by the multiplication of the ISF by the normalized collector current as shown by (3).

Note that, in each case, the surge of collector current and thus, the surge of collector current noise, occurs at the minimum of the collector voltage (Fig. 9), in other words, where the ISF is close to zero (Fig. 10) i.e., when the noise to phase noise conversion is at a minimum [5, 9]. Nevertheless, this impulse of current is clearly shorter in the case (c) than in the cases (a) and (b) which clearly demonstrate that the oscillator operating in class-C presents a smaller value of its effective ISF than that of the oscillator operating in a low or maximum power added state as clearly shown in Fig. 10.

Consequently, we can say that the large improvement in phase noise noted between the case (b) and (c) is mainly due to the class-C operation of the active part, for the reasons mentioned above, all the more that the power added is slightly lower in the case (c) than in the case (b).

Those simulation results clearly show that the optimal operating point, for the given specifications in terms of power consumption, oscillation frequency and for the

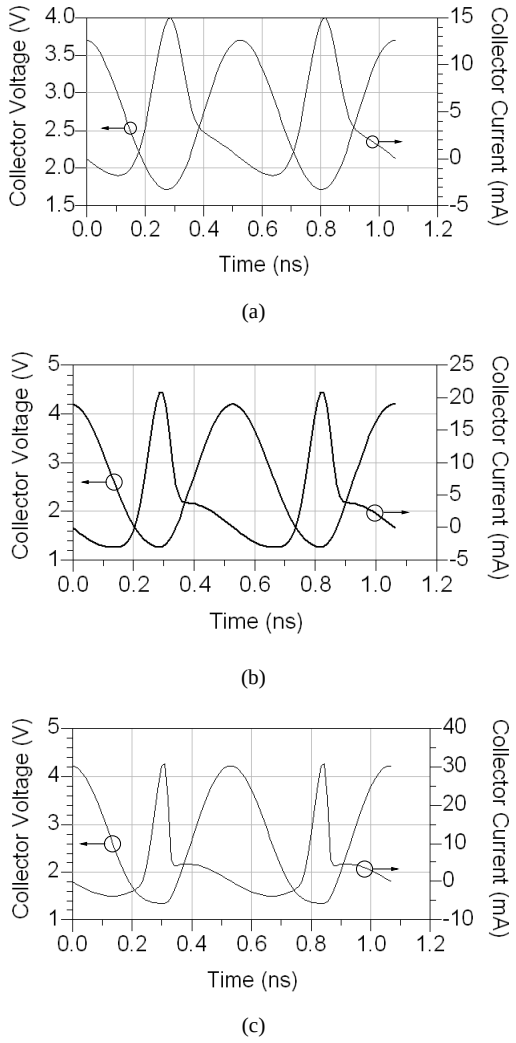

Figure 9: Simulated collector voltage and collector current of the oscillator for (a) a low Padd operating point, (b) a maximum Padd operating point and (c) a class-*C* operation

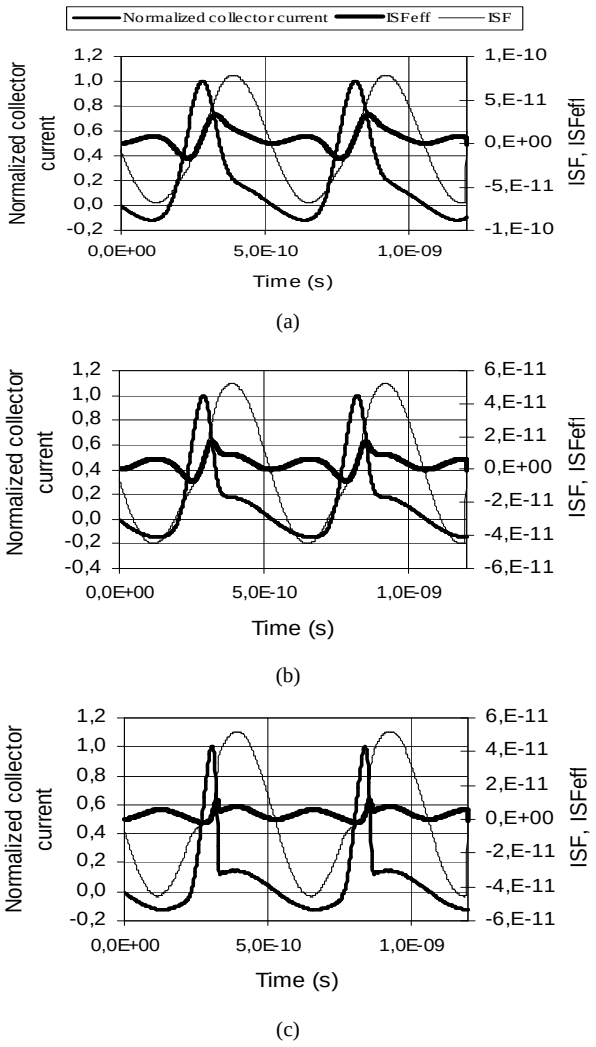

Figure 10: Normalized collector current and approximated ISF and ISF_{eff} for (a) a low Padd operating point, (b) a maximum Padd operating point and (c) a class-*C* operation

BiCMOS SiGe technology chosen, leading to the minimum phase noise is the class-C operation of the active part within the oscillator with a maximum voltage swing across the resonator for a given loaded quality factor. Furthermore, let us note that the presented simulations can easily be reproduced with another technology (i.e., transistors and resonator) and thus, with the architecture presented previously and the technology provided, designers could easily know which operating point of the active part leads to the minimum phase noise.

5. Applications

From the conclusions of the presented simulations, two fully integrated VCOs have been designed and implemented on the same 0.35 μm BiCMOS SiGe process. The first one is a 5 *GHz*, Full PMOS, *LC* differential VCO [12] and the second one, described here, is a dual band, *LC* differential VCO.

The design of this latter will be treated in sub-section 5.1 and sub-section 5.2 presents the measurements results.

5.1. VCO design

Fig. 11 shows the VCO schematic using a cross-coupled differential pair VCO topology. The feedback of the VCO is performed by a capacitive cross-coupling of the collector and base terminals of the differential pair. Note that the transistors are the same as those used for the simulations presented in section 4. The current source Bias1 draws 7 *mA* with a ratio of 14 which reduce significantly the power consumption. The frequency of oscillation is determined by the *LC*-Tank at the collectors. The tuning range depends on the global capacitance C variation and thus on the C_{max}/C_{min} ratio of the varactor diodes and on the AC coupling and nMOS capacitors. For frequency band switching, nMOS transistors operate as variable capacitors. Those transistors are used in inversion-mode (floating Drain-Source and grounded Bulk) because of the wide capacitor variation that can be obtained in this case [13]. The use of a symmetric center-tapped inductor as opposed to two "uncoupled" inductors exploits the benefits of the coupling factor k to increase the inductance value and can lead to a saving in chip area [14]. This inductor was fabricated with the highest metal level, which presents a low resistivity (5.5 $m\Omega/sq.$). Electromagnetic simulations, with Momentum software, result in a global inductance value of 2.6 *nH* (1.3 *nH* on each side) and an associated maximum Q factor of about 12 at 1.9 *GHz*. A tail capacitor C_E is used to attenuate both the high frequency noise components of the tail-current and the voltage variation on the tail node since the tail current source is not without impact on phase noise performances [15]. Thus, the most significant remaining noise source is the upconversion of the flicker noise [16]. Since we use an NMOS tail-current source for better current matching, the width and the length of the NMOS tail transistor must be increased to reduce the flicker noise which lowers significantly the close-in phase noise of the VCO.

To ensure proper startup of the oscillator, the following condition needs to be satisfied [6]:

$$\frac{g_m}{n} \cdot R_p > 1 \tag{23}$$

where g_m is the small signal transconductance of the bipolar transistors, R_p the resistive part of the resonator and n the ratio of collector to base voltage:

$$n = 1 + \frac{C_2}{C_1} \tag{24}$$

According to (23), better startup conditions will be obtained with a low n value and a high g_m of the active device, which requires a sufficient tail current of the differential pair. Fortunately, these two conditions

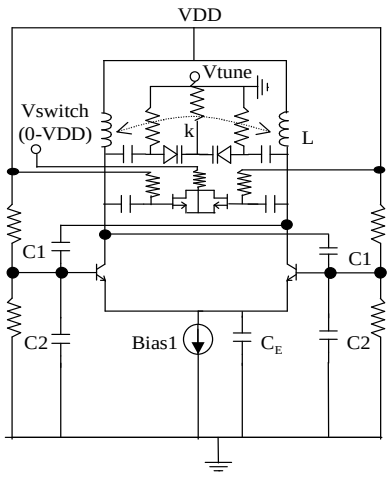

Figure 11: Differential VCO schematic

are consistent with the key point for phase noise minimization, describe in the previous sections. Indeed, a low n value will force the transistor to remain off when the ISF is maximum delivering periodically a peak of current when the ISF is close to zero [3] and increasing the tail current leads to an increase of the voltage swing across the resonator since the VCO is working in the current-limited regime of operation [16].

5.2. Implementation and measurements results

As mentioned previously, a 0.35 μm BiCMOS SiGe process, which provides four metal layers with a 5.3 μm thick top metal, is used to implement the VCO. Fig. 12 shows the microphotograph of the fabricated VCO whose size is 525×860 μm^2. During the layout, we have focus on the symmetry of the balanced circuits.

The tuning characteristic of the VCO is presented in Fig. 13. As expected in simulations, the VCO is tuned from 1.5 to 1.78 *GHz* for the lower band and from 1.64 to 2 *GHz* for the upper band with a tuning voltage varying from 0 to 2.7 V. The error on the prediction of the oscillation frequency is within 3 %.

The phase noise measurements were obtained using Agilent E4407B spectrum analyzer and a battery is used as voltage supply to avoid external parasitic signals. Fig. 14 shows the plot of the phase noise versus offset frequency from a 1.78 *GHz* carrier (Vtune=2.7 V and Vswitch=0 V).

As can be seen on this figure, the VCO features a best case phase noise of -98 dBc/Hz and -104 dBc/Hz at 50 *kHz* and 100 *kHz* frequency offset respectively. The phase noise curve shows -30 $dB/decade$ slope between 10 *kHz* and 20 *kHz* frequency offset and

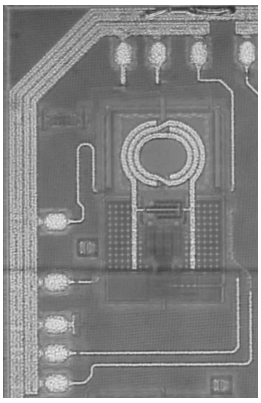

Figure 12: Microphotograph of the fabricated VCO

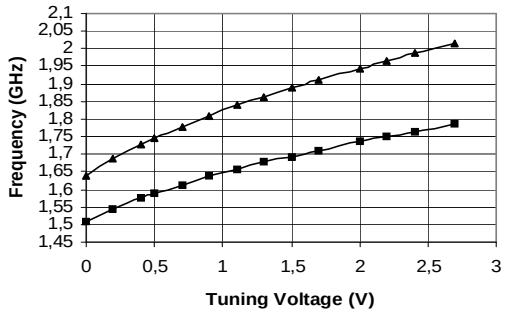

Figure 13: Tuning characteristic of the VCO showing the two frequency bands

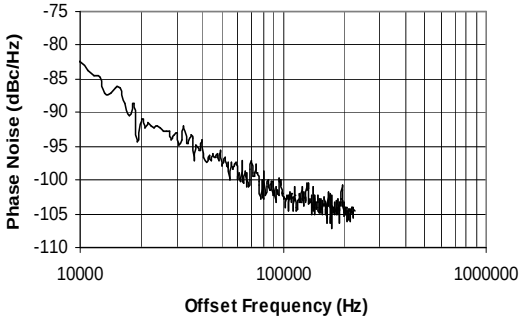

Figure 14: Measured phase noise versus offset frequency at 1.78 *GHz*

-20 $dB/decade$ slope between 20 kHz and 100 kHz frequency offset and reaches the noise floor of the spectrum analyzer beyond. Thus, the phase noise measurements beyond 100 kHz frequency offset is not accurate. However, assuming a -6 $dB/octave$ slope between 100 kHz and 1 MHz frequency offset, one can expect a best case phase noise value of about -124 dBc/Hz at 1 MHz frequency offset.

The figure of merit, that has been introduced to compare the performances of oscillators, is defined as follows:

$$FOM = L(\Delta\omega)\,[dBc/Hz] + 10 \cdot \log(Pdc\,[mW]) - 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) \quad (25)$$

This result in a FOM of -176 dBc/Hz for this design.

The measured performances of this SiGe VCO are summarized in Table 2.

Table 2: Measured VCO performances summary

Supply Voltage	$2.7V$
Power Consumption	$18.9\ mW$
Area	$525 \times 860\ \mu m^2$
Tunning Range (over two frequency bands)	$500\ MHz$
Tuning Voltage	$0 - 2.7\ V$
Center frequency	$1.5 - 2.0\ GHz$
Phase noise @ $50kHz$ **at** $1.78GHz$	$-98\ dBc/Hz$
Phase noise @ $100kHz$ **at** $1.78GHz$	$-104\ dBc/Hz$
FOM	$-176\ dBc/Hz$

6. Conclusion

An original method for determining the optimal operating point of the active part of an *LC* oscillator leading to a minimum phase noise for given specifications in terms of power consumption, oscillation frequency and for given devices (i.e., transistor and resonator) is presented in this paper. To achieve this optimal operating point, a proper *LC* oscillator topology, which provides a fixed loaded quality factor for different operating points of the active part, is studied and simulated. The presented simulation results clearly show that the optimal operating point, for the power consumption, oscillation frequency and the BiCMOS SiGe technology chosen, leading to the minimum phase noise is the class-C operation of the active part within the oscillator with a maximum voltage swing across the resonator for a given loaded quality factor. From this conclusion, a fully integrated, *LC* differential VCO has been designed and implemented on the same 0.35 μm BiCMOS SiGe process. The fabricated VCO is tuned over two frequency bands from 1.5 to 2 GHz with a tuning voltage varying from 0 to 2.7 V. The optimized measured best case phase noise is -98 dBc/Hz and -104 dBc/Hz at 50 kHz and

100 *kHz* frequency offset respectively under 2.7 *V* supply voltage with only 7 *mA* current consumption.

Acknowledgment

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