Design of a low-power 60 GHz transceiver front-end and behavioral modeling and implementation of its key building blocks in 65 nm CMOS

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THÈSE

En vue de l'obtention du

DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE

Délivré par *L'Institut National des Sciences Appliquées de Toulouse*
Discipline ou spécialité : *Micro-Ondes, Electromagnétisme et Optoélectronique*

Présentée et soutenue par *Michael M. Kraemer*
Le *3.12.2010*

Titre : *Design of a low-power 60 GHz transceiver front-end and behavioral modeling and implementation of its key building blocks in 65 nm CMOS*

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Ecole doctorale : *Génie Electrique, Electronique, Télécommunications*
Unité de recherche : *LAAS-CNRS*
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ABSTRACT

Worldwide regulations for short range communication devices allow the unlicensed use of several Gigahertz of bandwidth in the frequency band around 60 GHz. This 60 GHz band is ideally suited for applications like very high data rate, energy-autonomous wireless sensor networks or Gbit/s multimedia links with low power constraints. Not long ago, radio interfaces that operate in the millimeter-wave frequency range could only be realized using expensive compound semiconductor technologies. Today, the latest sub-micron CMOS technologies can be used to design 60 GHz radio frequency integrated circuits (RFICs) at very low cost in mass production.

This thesis is part of an effort to realize a low power System in Package (SiP) including both the radio interface (with baseband and RF circuitry) and an antenna array to directly transmit and receive a 60 GHz signal. The first part of this thesis deals with the design of the low power RF transceiver front-end for the radio interface. The key building blocks of this RF front-end (amplifiers, mixers and a voltage controlled oscillator (VCO)) are designed, realized and measured using the 65 nm CMOS technology of ST Microelectronics. Full custom active and passive devices are developed and characterized for the use within these building blocks.

An important step towards the full integration of the RF transceiver front-end is the assembly of these building blocks to form a basic receiver chip. Circuits with small chip size and low power consumption compared to the state of the art have been accomplished.

The second part of this thesis concerns the development of behavioral models for the designed building blocks. These system level models are necessary to simulate the behavior of the entire SiP, which becomes too complex when using detailed circuit level models.

In particular, a novel technique to model the transient, steady state and phase noise behavior of the VCO in the hardware description language VHDL-AMS is proposed and implemented. The model uses a state space description to describe the dynamic behavior of the VCO. Its nonlinearity is approximated by artificial neural networks. A drastic reduction of simulation time with respect to the circuit level model has been achieved, while at the same time maintaining a very high level of accuracy.

You see, wire telegraph is a kind of a very, very long cat.
You pull his tail in New York and his head is meowing in Los Angeles.
Do you understand this?
And radio operates exactly the same way:
you send signals here, they receive them there.
The only difference is that there is no cat.

— attributed to Albert Einstein

ACKNOWLEDGMENTS

This is the place to express my thanks to many people without whom my doctoral thesis would not have been the same.
First of all I want to express my thanks to Daniela Dragomirescu and Robert Plana for their support and the excellent research environment the MINC group provided.
Next, I want to thank all the examiners for taking their time to read and evaluate my thesis.
I also want to thank Sorin Voinigescu and his Ph.D. students (especially Katya Laskin) for the week I spend at the University of Toronto and the technical discussions we had about mm-wave RFIC design.
Thanks go also to the members of the characterization group, especially Alexandre Rumeau and Laurent Bary, for their help during various measurement campaigns and the sysadmin team (especially Marie-Dominique Cabanne and Frederick Ruault) for their high responsiveness and competent help. A special thank goes to Eric Tournier for his help with the installation and use of the secure network. Thanks also go to Olivier Lliopis for his support during the characterization of the oscillator, and Teddy Borr and Christoph Viallon, all from MOST group, for interesting discussions.
Thank you, Brigitte Ducrocq, for the very efficient help concerning administrative tasks and the organization of conference trips.
My sincere thanks go also to all member of the MINC research group, especially the ones I were in closer contact with, for having made my almost four years at LAAS a pleasant experience. Thanks also for your practical help and the many technical discussions. Namely I want to mention the members of the Wireless Sensor Network team, which I worked with on a daily basis: Aubin Lecointre, Vicent Puyal, Julien Henaut, Thomas Beluch, Mariano Ercoli and Florian Perget.
At the same I am grateful for the time I spent at INSA Toulouse during the monitorat and at the CIES - seminars and the atelier - projet. Thanks to all I got to know there.
Thanks also go to the different external project partners and suppliers I worked with, in particular CEA Leti, CMP, CNFM, Dolphin Integration, IMS Bordeaux, Mühlhaus consulting (support and distribution of Sonnnet Software), NXP Netherlands, STMicroelectronics, and many others. Furthermore, I want to acknowledge the principal sources of financial support of this thesis, namely the research projects RadioSoC, Qstream and Nanocomm.
And as I have surely forgotten someone important: Special thank to those who find themselves not on this list but deserve to be on it.

... and most importantly: Kerstin, thanks for everything !

CONTENTS

ADC	Analog-to-Digital Converter
ADS	Advanced Design System (by Agilent)
ANN	Artificial Neural Network
AMOS	Accumulation-mode MOS
AWGN	Additive White Gaussian Noise
BB	Baseband
BPF	Bandpass Filter
BPSK	Binary Phase Shift Keying
CMOS	Complementary Metal Oxide Semiconductor
CMS	Common Mode Signaling
CPW	Coplanar Waveguide
CS	Common Source
DAMI	Dual Alternate Mark Inversion
DAC	Digital-to-Analog Converter
DC	Direct Current
DK	Design Kit
DSB	Double Sideband
DUT	Device Under Test
EC	European Commission
EIRP	Equivalent Isotropically Radiated Power
EM	Electromagnetic
ENR	Excess Noise Ratio
ESD	Electrostatic Discharge
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FET	Field Effect Transistor
FFT	Finite Fourier Transform
FMCW	Frequency Modulated Continuous Wave
FoM	Figure of Merit
FTR	Frequency Tuning Range
GaAs	Gallium Arsenide
GP	General Purpose
G-S-G	Ground-Signal-Ground
HD	High Definition
HDMI	High-Definition Multimedia Interface
HPBW	Half Power Beam Width
HVT	High Threshold Voltage
IF	Intermediate Frequency
IFE	In-Flight Entertainment
IMOS	Inversion-mode MOS
InP	Indium Phosphide
IP	Intellectual Property
IP_3	Third Order Intermodulation Point
ISI	Inter Symbol Interference
ISS	Impedance Standard Substrate

ITRS	International Technology Roadmap for Semiconductors
LDPC	Low-density Parity-check
LNA	Low Noise Amplifier
LO	Local Oscillator
LOS	Line Of Sight
LP	Low Power
LSB	Lower Sideband
LVT	Low Threshold Voltage
MAC	Medium Access Control
MEMS	Micro Electro Mechanical System
MIM	Metal Insulator Metal
MIMO	Multiple-Input Multiple-Output
MLP	Multilayer Perceptron
MMIC	Monolithic Microwave Integrated Circuit
mm-wave	millimeter-wave
MOM	Metal On Metal
MOS	Metal Oxide Semiconductor
MPG	Monopulse Generator
MSE	Mean Squared Error
NF	Noise Figure
NLOS	Non Line Of Sight
ODE	Ordinary Differential Equation
OFDM	Orthogonal Frequency Division Multiplex
OOK	On-Off-Keying
PA	Power Amplifier
PAL	Protocol Adaptation Layer
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
pHEMT	pseudomorphic High Electron Mobility Transistor
PHY	physical
PLL	Phase Locked Loop
PPM	Pulse Position Modulation
PRF	Pulse Repetition Frequency
PSM	Pulse Shape Modulation
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMS	Root Mean Square
RL	Return Loss
RS	Reed-Solomon
SDR	Software Defined Radio
SiGe	Silicon Germanium
SiP	System in Package
SNR	Signal-to-Noise Ratio
SoC	System on Chip
SOI	Silicon On Isolator
SOLT	Short Open Load Through
SRF	Self Resonant Frequency
SSB	Single Sideband
STI	Shallow Trench Isolation
SVT	Standard Threshold Voltage

TFMS	Thin Film Microstrip
TL	Transmission Line
T/R	Transmit/Receive
US	United States
USB	Upper Sideband
UWB	Ultra Wideband
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VHSIC	Very High Speed Integrated Circuit
VHDL	VHSIC Hardware Description Language
VHDL-AMS	VHSIC Hardware Description Language - Analog and Mixed-Signal
VNA	Vector Network Analyzer
Wi-Fi	Wireless Fidelity
WPAN	Wireless Personal Area Network
WSN	Wireless Sensor Network

GENERAL INTRODUCTION

This thesis is part of a research effort to develop a radio interface for *very high data rate* communication in the unlicensed 60 GHz band. The radio interface is intended to be realized in the form of a System in Package (SiP) exhibiting *very low power consumption* and *very low cost* in order to meet the stringent requirements of applications like Wireless Sensor Networks (WSNs).

The contribution of this thesis to this research effort is twofold:

- On the one hand, the design of the radio front-end and the implementation of its key components in a nanoscale CMOS technology is addressed (cf. part I).
- On the other hand, the behavioral modeling of the front-end's building blocks in the hardware description language VHDL-AMS is discussed and a novel technique to create accurate behavioral models of millimeter-wave oscillators is proposed (cf. part II).

Part one of this thesis treats the different aspects of the design of a high data-rate, low-power, low-cost radio front end for the 60 GHz band. It is divided into six chapters:

Chapter 1 gives an introduction to communication in the unlicensed 60 GHz band. It contains a discussion of the potential applications for wireless high-data rate links. It also illustrates the laws governing systems communicating around 60 GHz: these laws originate from the physical properties of this frequency band, the regional frequency allocations and various communication standards. Finally, an overview of the planned SiP is given to show where the front-end is situated in the system and which blocks it has to interface with.

Chapter 2 presents the state-of-the-art of 60 GHz radio front-ends and discusses transceiver architectures suitable for the intended radio interface. On the basis of this review, a direct conversion architecture is adopted for both the receiver and the transmitter side. This choice impacts the circuit design presented in the subsequent chapters.

Chapter 3 describes the basic principles of mm-wave Radio Frequency Integrated Circuit (RFIC) design using a 65 nm CMOS technology and illustrates the development of full-custom active (varactors) and passive (inductors, transformers) devices.
In this context, improved methodologies are proposed to both accurately simulate the behavior of millimeter-wave (mm-wave) inductors and de-embed measurements of test inductors.
In the remainder of the chapter, important RFIC design and layout techniques, which were commonly employed to build the circuits presented in this thesis, are also illustrated.

Chapter 4 presents design, measurements and a performance evaluation of the four major 60 GHz front-end components realized in the

framework of this thesis. These circuits include a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO) (including output buffers), a down-conversion mixer (including baseband and LO buffers) and a up-conversion mixer (including the baseband buffer). The chapter's conclusion summarizes the features and performance of these components.

Chapter 5 presents the integration of the LNA, VCO and down-conversion mixer to form a 60 GHz direct-conversion receiver front-end, consisting of a single in-phase branch. The measured results are discussed and compared to the state-of-the-art.

Chapter 6 concludes on the transceiver-design part of this thesis and gives an outlook towards future work.

Part two of this thesis discusses the creation of behavioral black-box models that describe the millimeter-wave components presented in part one. It consists of three chapters:

Chapter 7 gives an introduction to behavioral modeling in the context of System on Chip (SoC) and System in Package (SiP) design. It also briefly introduces the hardware description language VHDL-AMS used to implement the presented models.

Chapter 8 proposes a novel technique to create behavioral models of mm-wave oscillators. A theoretical introduction discusses the description of oscillators by nonlinear differential equations, their state space representation and the use of artificial neural networks to approximate arbitrary nonlinear functions. Then, the fundamental structure of the proposed model is introduced and issues arising during parametrization and implementation are discussed. The accuracy of realized modeling examples prove its suitability to model mm-wave CMOS oscillators.

Chapter 9 concludes on oscillator models and shows perspectives towards the modeling of the remaining front-end components and their interaction.

The last part of this thesis is dedicated to a general conclusion, which reviews the presented scientific achievements. It is followed by a list of the associated scientific publications.

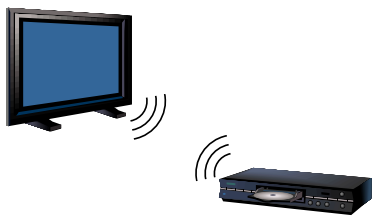
Part I

60 GHZ TRANSCEIVER DESIGN

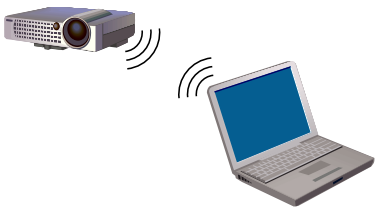
1 INTRODUCTION TO COMMUNICATION IN THE 60 GHZ BAND

1.1 APPLICATIONS FOR LOW-POWER VERY HIGH DATA RATE WIRELESS COMMUNICATIONS

Until recently, communication systems achieving very high data rates (i.e. superior to around 1 Gbit/s) where essentially limited to either wired (electrical and optical) links or commercial wireless point-to-point transmissions [1] (e.g. in telecommunication backhaul networks). However, in the context of high data rate Wireless Personal Area Networks (WPANs), which is the class of networks with a range below 10 m [2], new consumer-oriented applications are emerging.
Two of these applications for very high data rate point-to-point WPANs are illustrated in figure 1.1: Both the connection between a High Definition (HD) television and a HD video source and the wireless link between a personal computer and a video projector demand very high data rates over small distances. Not long ago, only wired connections were feasible for these applications at reasonable cost. Today, the first wireless solutions are available to the end-customer, employing low-cost Complementary Metal Oxide Semiconductor (CMOS) based integrated circuits that exploit different frequency bands[1].
Another potential application where the replacement of multimedia cables by wireless links would be highly beneficial is In-Flight Entertainment (IFE) [4]. This application is still in an early research phase, due to the fact that multiple high data rate point-to-multipoint links are required to equip an entire commercial passenger airliner. The total data rate is thus a multiple of the one needed in the above mentioned point-to-point applications. A further particularity is the propagation channel inside the aircraft cabin.
The common point of the applications discussed above is that they



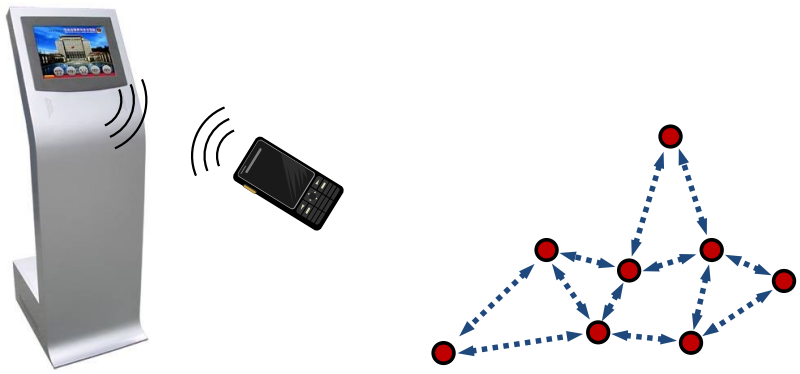
(a) Uncompressed high definition video link



(b) Wireless connection towards a video projector

Figure 1.1: High data rate multimedia in a WPAN context

[1] Three prominent examples of companies that serve the market for these applications are SiBEAM (SiBEAM Inc., www.sibeam.com, providing System in Packages (SiPs) for uncompressed 60 GHz video transmission exploiting the WirelessHD standard) [3], WISAIR (WISAIR Inc., www.wisair.com, realizing uncompressed Ultra Wideband (UWB) data transmission in the band between 3.1 and 10.6 GHz, sold as WirelessUSB) and Intel (Intel Corporation, www.intel.com, implementing a technology called Wireless Display into their next generation of laptop processors that permits a compressed video transmission using the Wireless Fidelity (Wi-Fi) standard at 2.4 GHz)



(a) Wireless download of multimedia contents from kiosk

(b) Multi-hop self-powered WSN

Figure 1.2: High data rate applications with severe power consumption constraints

do not have strong low power constraints. Applications where low power consumption of the circuits is a major issue are illustrated in figure 1.2: the left picture shows a point-to-point connection between a multimedia terminal and a mobile phone. Data rates of several Gbit/s are required to download huge video files rapidly. The low power constraint is introduced by the battery powered mobile phone. Figure 1.2b shows the principal structure of a multi-hop Wireless Sensor Network (WSN) [5]. This kind of WSN is typically used for surveillance, military and monitoring applications. High data rate requirements can have different causes: either, they result from a very short time interval between measurements whose results must be transmitted, or a very high number of communicating nodes, or a high amount of data that has to be transmitted at an event. Due to the fact that the sensors are self-powered (and either use batteries or harvest energy from the environment), their lifetime (and even realizability) strongly depends on the circuit's power consumption, which consequently has to be very low. The commercially available transceivers for very high data rate WPANs do not meet these requirements.
A potential application of WSNs in the aerospace domain is shown in figure 1.3. A large number of sensors is deployed on the wing of a prototype aircraft. They are used during flight tests in the development phase of the aircraft to monitor pressure, temperature and mechanical strain in real time. Today, these sensor networks are wired. In the future, a wireless solution could greatly reduce the cost and setup time of flight tests. The employed wireless sensors need to be energy autonomous during the flight test, leading to the requirement of low power consumption of the employed radio interface [6].
A key challenge when designing a radio interface for the applications illustrated in figures 1.2 and 1.3 is to achieve *both* data rate in excess of 1 Gbit/s *and* limit the circuit's power consumption, which is related to the transmit power. Shannon's channel capacity [7] shows how this can be achieved: The capacity C of a channel of bandwidth B with Additive White Gaussian Noise (AWGN) is given by

$$C = B \log_2 \left(1 + \frac{P_S}{P_N}\right), \tag{1.1}$$

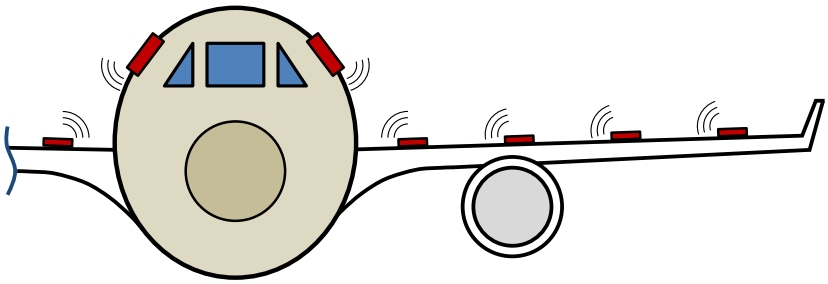


Figure 1.3: WSNs deployed on aircraft wings for real-time in-flight testing

where $\frac{P_S}{P_N}$ is the Signal-to-Noise Ratio (SNR) [7]. As increasing the signal power P_S in order to increase the channel capacity is not an option due to low power constraints, a large bandwidth B is required. Note however, that increasing B is also increasing the noise power P_N, as P_N is proportional to B as well. Nevertheless, there is still a net increase in channel capacity originating from the larger bandwidth, as P_N is part of the binary logarithm.

Two bands with sufficiently large, unlicensed bandwidth are available: The Ultra Wideband (UWB) frequency range from 3.1 GHz to 10.6 GHz [8] and the 60 GHz band (cf. section 1.2.1).
Communication in the UWB frequency range between 3.1 GHz and 10.6 GHz has been subject to extensive research for some time now. An interesting advantage of this band is its suitability for communication by very short impulses, which require large relative bandwidth. These impulse-based UWB modulation schemes allow the implementation of circuits that exhibit very low power consumption. The doctoral thesis of A. Lecointre (2010, [8]) discusses impulse-based UWB communication and describes the development of an impulse-based radio interface for this frequency range. However, there are several obstacles that indicate that a 60 GHz solution might be the better choice: among the most important technical challenges for UWB communication in the frequency band between 3.1 GHz and 10.6 GHz are low permitted transmit power, strong in-band interferers and design of circuits with large relative bandwidth. Furthermore, the commercial exploitation of this band is handicapped by very different regulations between Europe and the United States, as well as standardization issues [9–11].
This thesis is part of a study that evaluates the feasibility of a 60 GHz solution. Thus, it focuses exclusively on this frequency band. The regulations and standards governing communication in the unlicensed 60 GHz band, as well as its specific characteristics, are discussed in section 1.2. A link budget is calculated in section 1.3.

Besides low power and very high data rate, a third requirement for circuits designed for the presented applications is very low fabrication cost [12]. This requirement originates either from the fact that these are consumer applications, or in the case of WSNs that a high number of communicating nodes is needed, whose overall cost must be comparable to a wired solution.
An overview of the planned 60 GHz radio interface for low power applications is given in section 1.4. It is designed in order to accommodate the three major constraints given above. Part I of this thesis deals with

the design of a low power, low cost, ultra wideband CMOS 60 GHz transceiver front-end for this radio interface.

1.2 THE UNLICENSED 60 GHZ FREQUENCY BAND

The circuits presented in this thesis are part of a radio interface that communicates within the 60 GHz band. Thus, this section discusses the regulation and standardization in this band and highlights its important properties. Additional introductory literature is provided by [1, 11–17].

1.2.1 *Regulations of the 60 GHz band*

In January 2001, the Federal Communications Commission (FCC) of the United States (US) realigned the frequencies of the unlicensed 60 GHz band as a consequence of "recent technological advances" in order to "facilitate the commercialization of the millimeter wave spectrum" [18]. An unlicensed use of the band between 57 GHz and 64 GHz is since then possible with an average power density of 9 $\mu W/cm^2$ at 3 m (equals 40 dBm Equivalent Isotropically Radiated Power (EIRP)) and a peak power density of 18 $\mu W/cm^2$ at 3 m (equals 43 dBm EIRP) [15, 19]. The total peak transmitter output power is limited to 500 mW, and is further reduced if the emission bandwidth is less than 100 MHz. As mentioned in [19], the devices must in addition to that regulation comply with the exposure requirements for Radio Frequency (RF) radiations issued by the FCC. Equipment used on aircraft or satellites is not allowed to use the 60 GHz band under the conditions of this unlicensed allocation [19]. In Canada the 60 GHz regulation is harmonized with the one of the US [15].
In the European Union, the European Telecommunications Standards Institute (ETSI) established a basis for future regulations of the 60 GHz band by recommendations published in 2007 [20]. These recommendations are often cited in research papers as a quasi standard [15]. The recommendation states that a change of the present frequency allocation is desirable in order to allow the use of ultra wideband short range devices in the 60 GHz band. In May 2009, the European Commission (EC) amended a prior decision on the harmonization of the radio spectrum for use by short range devices [21] by decision 2009/381/EC [22]. It puts into force the harmonized European standard ETSI EN 302 567 which allocates the 9 GHz frequency band from 57 GHz to 66 GHz for unlicensed use all over the European Union. Within this frequency band, the indoor power density limit is 13 dBm/MHz EIRP with a maximum total power level of 40 dBm EIRP. For outdoor applications, the allowed power is 15 dB less.

Figure 1.4 shows the unlicensed 60 GHz frequency bands in other areas of the world compared to the ones in North America and Europe as outlined in [15]. The unlicensed band common to all of these countries corresponds to the regulation in Australia which reaches from 59.4 GHz to 62.9 GHz.
To sum up, at least 3.5 GHz of unlicensed bandwidth are available in all of the countries listed in figure 1.4. While maximum transmit power levels are mostly restricted to some ten milliwatts, this power can be strongly focused towards one direction by using high gain

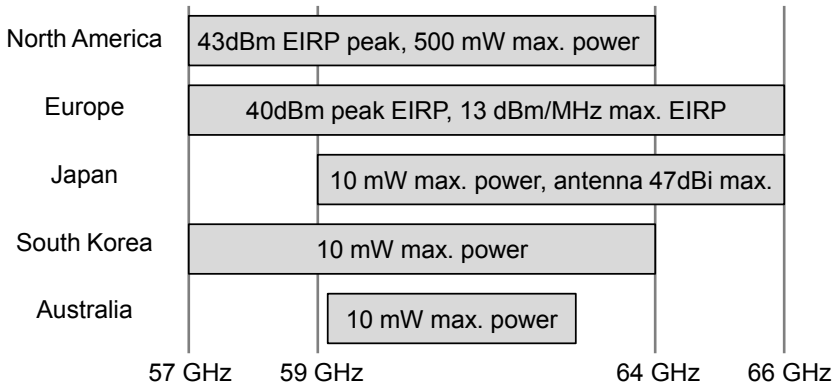


Figure 1.4: Regulation of the 60 GHz band in selected regions

antennas. Compared to the UWB regulation between 3.1 and 10.6 GHz, the allowed EIRP is about a hundred thousand times higher.

1.2.2 *Standardization for the 60 GHz Band*

One advantage of the use of an unlicensed frequency band is that implementations are not bound to a particular standard. This is especially advantageous in the context of WSNs, because it gives more freedom for the implementation of power saving strategies [5]. As all of the nodes usually use radio interfaces developed by the same entity, proprietary communication protocols are sufficient. On the other hand, for commercial applications, industry standards are necessary to permit interoperability between devices of different manufacturers.
This thesis is not based on a particular one of these standards, but rather adopts some of the very general definitions common to all of them (the most important one specifies the communication channels). The reason for this is that the low-power 60 GHz front-end designed as part of this thesis shall be generally applicable. Furthermore, one option for the baseband of the proposed radio front-end is based on impulse modulation [8], for which no 60 GHz standard exists. As impulse-based modulations are particularly well suited for WSNs, the front-end proposed in this thesis needs to be able to up-convert UWB impulses to the 60 GHz band.

In the following, the most important standards for communication in the unlicensed 60 GHz band are briefly introduced to show their similarities and differences. The focus lies on the IEEE 802.15.3c standard, because this is the one which contains most of the definitions that are adopted in this thesis.
The **IEEE 802.15.3c standard** [23] defines an alternative millimeter-wave (mm-wave) Medium Access Control (MAC) and physical (PHY) layer for WPAN applications [2]. The standard's MAC layer includes two different possibilities of beam steering, because phased antenna arrays are necessary at 60 GHz to achieve a high gain in an arbitrary, varying direction (for further details on the MAC layer refer to the standard document [23]).
As spectrum allocation is inconsistent internationally (cf. section 1.2.1), a very important point within the PHY layer description is the definition of communication channels that represent a good compromise

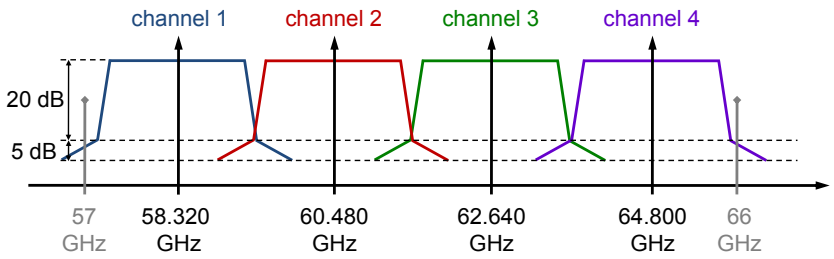


Figure 1.5: The four channels as defined by the IEEE 802.15.3c standard [23]

between the different regional regulations. The solution proposed by the IEEE 802.15.3c standard (and adopted by all other important 60 GHz standards) is given in figure 1.5. The carrier frequencies of neighboring channels are separated by 2.16 GHz. Depending on the regional frequency allocation, only a part of these channels can by used. Figure 1.5 also indicates the spectral masks that have to be respected by compliant devices. The maximum power density stays constant over a bandwidth of 1.880 GHz per channel.
Three fundamental PHY modes are defined within the IEEE 802.15.3c standard:

- A single carrier mode (called *SC PHY*) provides three communication classes that implement single carrier modulation schemes. Either Reed-Solomon (RS) or Low-density Parity-check (LDPC) codes are employed. The first class provides up to 1.5 Gbit/s for low power low cost mobile applications, the second class up to 3 Gbit/s and the third class up to more than 5 Gbit/s for high performance applications. An additional optional class using Dual Alternate Mark Inversion (DAMI) or On-Off-Keying (OOK) modulation is also defined in this mode.

- A high speed interface mode (called *HSI PHY*) provides data rates up to 5.7 Gbit/s using Orthogonal Frequency Division Multiplex (OFDM) modulation. LDPC codes are employed.

- An audio/visual mode (called *A/V PHY*) is implemented. It contains a high-rate PHY with up to 3.8 Gbit/s for uncompressed HD audio/video transmission and a low-rate omnidirectional PHY mode with up to 10 Mbit/s for coordination purposes. Both modes employ OFDM with convolutional inner code and RS outer code.

In addition, to promote coexistence and interoperability, a Common Mode Signaling (CMS) scheme is defined based on a low data rate single carrier mode. This multitude of modes make the IEEE 802.15.3c a very general standard that is well suited to address most of the applications given in section 1.1.

The other standards presented in the following are either inspired by IEEE 802.15.3c, or exhibit similar properties due to the specificities of the 60 GHz band. In particular, the channel frequencies (cf. figure 1.5) are the same for all published specifications, and all MAC layers implement beam steering.
The **WirelessHD** standard [24] is focused on the delivery of high quality, uncompressed audio/video content with up to 1080 pixel resolution, 24

bit color and 60 Hz refresh rates for version 1.0a. A range of at least 10 m is achieved by employing highly directive smart antenna technology and exploiting Non Line Of Sight (NLOS) communication [24]. Version 1.0a of the standard supports data rates up to 3 Gbit/s, while newer generations define higher resolutions and data rates up to 28 Gbit/s.
The **ECMA-387 standard** [25] defines a 60 GHz PHY and MAC layer as well as a High-Definition Multimedia Interface (HDMI) Protocol Adaptation Layer (PAL). The standard addresses both data transfer applications and uncompressed audio/video streaming and is thus, like the IEEE 802.15.3c standard, suitable for most of the applications introduced in section 1.1. Single channel data rates up to 6.35 Gbit/s are supported. As special feature, channel bonding permits the usage of multiple channels in parallel, providing a theoretical maximum data rate of 25 Gbit/s.
The **Wireless Gigabit Alliance's WiGig 1.0** specification, which is only available for adopters of the standard, is more oriented towards data transmission in the context of Wi-Fi networks. It supplements the IEEE 802.11 MAC layer and is backward compatible to the IEEE 802.11 standard. Distances in excess of 10 m are expected due to the use of highly directive antennas and beam forming. The PHY layer is supporting both low power and high performance devices, while data transmission modes with rates up to 7 Gbit/s are defined.
A standardization effort similar to WiGig is carried out by the **IEEE 802.11ad task group**[26], which evolved from the IEEE 802.11VHT study group. Their objective is to define standardized modifications to both the 802.11 PHY layer and the 802.11 MAC layer to enable operation in the 60 GHz frequency band capable of very high throughput. Up to now, no finalized proposal is available.

1.2.3 *Characteristics of the 60 GHz band*

This section presents the physical conditions of communication in the unlicensed 60 GHz band. Some of the very basic properties of this band originate from the fact that the free space wavelength at 60 GHz of $\lambda_{60\,\mathrm{GHz},0} = 5\,\mathrm{mm}$ is much smaller than at frequencies previously used for short range communication.

ANTENNAS The short wavelength has a strong influence on the behavior of the antennas used in the 60 GHz band. As the capability of an antenna to obtain power from an electromagnetic field depends more directly on the effective area A_e than on directivity or gain, the following considerations start with this antenna parameter. It is defined by

$$A_e = \frac{\lambda_0^2}{4\pi} G \tag{1.2}$$

for a lossless isotropic radiator (with gain G = 1, that is 0 dBi) [27]. A_e decreases quadratically with decreasing wavelengths. This reflects the observation that the size of a simple antenna (like a dipole or a patch antenna), which is related to its effective area, decreases with increasing frequency.
The smaller antenna size, in turn, impacts the capability of the antenna to extract power from an incoming electromagnetic wave of power

spectral density S: the power obtained by the receiving antenna is directly proportional to its effective area [27], as can be seen from

$$P_{r,max} = SA_{e,r}, \tag{1.3}$$

where $P_{r,max}$ is the maximum power that can be extracted from the incident wave by a lossless receiving antenna in case of power match. The consequence is that a receiving antenna with a given gain $G_{r,1}$ at 60 GHz obtains less power from a field of electromagnetic power density S than an antenna with the same gain $G_{r,1}$ at lower frequencies. This can be seen if putting (1.2) and (1.3) together according to

$$P_{r,max} = S\frac{\lambda_0^2}{4\pi}G_{r,1}. \tag{1.4}$$

Because of the quadratic term λ_0^2, the received power decreases with frequency even if the same gain is available.
The electromagnetic power density $S(r)$ in free space, which was created by the transmit antenna, obeys to a different law: it decays equally fast at all frequencies as a function of distance r. Namely,

$$S(r) = P_t\frac{G_{t,1}}{4\pi r^2}, \tag{1.5}$$

where $G_{t,1}$ is the gain of the transmitting antenna and P_t the transmit power [27].
Thus, according to equation (1.3), the antennas need to have *the same effective area* at 60 GHz as at lower frequencies (and not the same gain) to receive the same power. The use of an antenna with smaller effective area (often considered an asset of the 60 GHz band) is, despite the possibility that it might have a higher gain, accompanied by a higher path loss. The Friis transmission formula [28], which results when putting together (1.2), (1.3) and (1.5), illustrates this:

$$\frac{P_r}{P_t} = G_tG_t\left(\frac{\lambda_0}{4\pi r}\right)^2. \tag{1.6}$$

As this equation is often used in a context where the antennas are characterized by their gain, the increased loss at 60 GHz is implicitly assigned to the channel and not to the antenna. However, as illustrated by (1.2), the part of the transmission formula including λ_0 is introduced by the antenna, whose effective area is wavelength-dependent according to (1.2). As the gain of an antenna of the same effective area is higher at higher frequencies, in the 60 GHz band a much higher antenna directivity is required to obtain the same path loss as at lower frequencies (refer also to the link budget calculation in section 1.3). In practice, this often results in the use of aperture antennas, parabolas or antenna arrays.

The higher directivity of 60 GHz links demands a continuous effort to align the antenna beams if one of the communicating nodes is mobile. While in the case of the kiosk application this alignment of antenna beams is done by the user, in more advanced applications electronic beam forming or beam switching has to be employed. The standards for communication in the 60 GHz band (cf. section 1.2.2) consequently provide beam steering technology in the different communication layers.

Another approach to increase the total antenna area can be the use of Multiple-Input Multiple-Output (MIMO) systems [29], where each antenna is associated with a separate transceiver circuit. While complexity increases drastically in this case, especially if a high number of antennas is employed, a high level of integration can make these kind of solution feasible (e.g. antennas together with RF front-end and baseband-circuitry, including MIMO processing, in one SiP).

CHANNEL In addition to the path loss originating from the spreading of the transmitted power by the antenna, there are other sources of loss to consider. An attenuation phenomenon that is particularly pronounced in the 60 GHz band is oxygen absorption [30]. In the spectrum of absorption due to atmospheric gases, plotted in figure 1.6, a peak around 60 GHz is clearly observable. However, while the absorption in this frequency band is quite high relative to other frequencies (consider the logarithmic ordinate), it remains below 0.2 dB at 10 m and is thus negligible with respect to free space loss in a WPAN context. The same is true for attenuation due to rain, which is on the same order of magnitude as oxygen attenuation [1, 16, 31]. Besides, this second mechanism applies only to outdoor environments.
A more immediate effect on WPANs is caused by the high attenuation of materials like concrete, stone or wood [12, 16, 31]. Penetration loss can be as high as 35 dB if the 60 GHz wave is passing through a simple composite wall [32]. Thus, wave propagation through walls is hardly possible in the 60 GHz band and indoor WPANs are usually limited to one room at this frequency if one single transceiver is employed [33, 34].
Inside a room, the blocking of the Line Of Sight (LOS) path by obstacles (e.g. furniture) drastically increases the attenuation. Besides the higher penetration loss, this comes from the fact that at 60 GHz neither diffraction nor diffuse reflection (scattering) contribute significantly to the received power [33], because most obstacles are large compared to the wavelength at 60 GHz [16]. Non Line Of Sight (NLOS) paths that avoid the obstacle should be exploited to maintain communication in

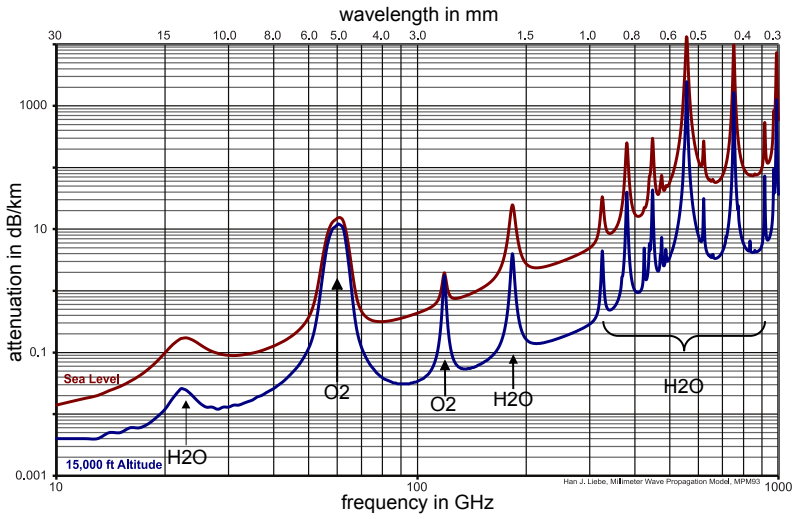


Figure 1.6: Absorption of mm-waves due to atmospheric gases at sea level and 15.000 feet altitude (courtesy of OML Inc., www.omlinc.com)

these cases [1].
A particularly severe case is the blocking of the LOS path by a person: on the one hand, additional attenuation ranging from 18 dB to 36 dB due to the high water content of the human body have to be expected [15]. On the other hand, the person must be considered a moving obstacle. Thus, if beam steering is employed to find the NLOS path of lowest attenuation, a very frequent update of the optimum path has to be provided.
In the WPAN context, the high attenuation and directivity of the 60 GHz channel nevertheless provides some advantages: A high density of communication cells that re-use the same frequency, especially in indoor environments, is possible (i.e. possible frequency re-use in adjacent apartments/offices), and the interference level is quite low (also because the 60 GHz band is barely exploited today). Another consequence is a less harsh multipath environment compared to lower frequencies. The remainder of this section discusses this aspect.
In a 60 GHz indoor channel, multiple NLOS propagation paths can be observed, especially if highly reflective walls are present. As mm-waves are sufficiently short, each path can be considered as a discrete ray, resolvable from the impulse response if the measurement resolution is fine enough [31]. This is in contrast to lower frequencies, where diffraction and scattering significantly contribute to the spreading of the signal [16, 33].
To quantify the temporal spreading effect on the signal due to multipath propagation, the Root Mean Square (RMS) delay spread τ_{RMS} is usually employed [16]. If τ_{RMS} becomes comparable or superior to the interval between the transmitted symbols (which is inversely proportional to the data rate), Inter Symbol Interference (ISI) occurs. As a consequence, techniques to remove ISI (e.g. equalization, OFDM) become necessary at the receiver side [16, 33, 35]. This is usually not desired for transceivers serving low cost low power applications, hence the interest in a small RMS delay spread.
Measurements of the channel impulse response in 60 GHz indoor environments yield typical RMS delay spreads ranging from 15 to 40 ns for small rooms and from 40 to 70 ns for larger office buildings, if omnidirectional antennas are employed [31, 33]. These values still introduce significant ISI at Gbit/s rates. However, the use of directional antennas can decrease τ_{RMS} considerably, since they limit the angle of arrival of the signal. Signals coming from the direction the antenna beam is pointed to are amplified, while signals coming from other directions are attenuated. Antennas with Half Power Beam Widths (HPBWs) of 30°achieve typical values of $\tau_{RMS} < 10$ ns, while values as small as $\tau_{RMS} = 1$ ns are obtained using antennas with very focused beams (HPBW around 5 °) [14, 16]. As very directive antennas are needed to achieve a sufficient effective area, such low τ_{RMS} values are not unrealistic in 60 GHz communication systems.
Especially in smallband channels multipath propagation also leads to signal fading. However, as channels have a typical bandwidth of around 2 GHz in the ultra wide 60 GHz band (cf. to section 1.2.2), fading is expected to be less of an issue [31]. A maximum signal attenuation due to fading of only 3 dB is considered to be realistic [29].

1.3 a link budget for the 60 ghz band

In order to illustrate which distances can be expected for Gbit/s links at 60 GHz in a WPAN context, this section provides a simple link budget for LOS and NLOS environments. It assumes a low cost CMOS transceiver front-end and phased antenna arrays that can be integrated within a System on Chip. The intention is to give an overview of the key issues, without focusing on a specific environment or implementation. More specific link budgets can be found for example in [15] or [29].
The link budget in logarithmic form (dB, dBm) is given by [15, 29]

$$\mathrm{SNR} = P_t + G_t - \mathrm{PL}(d) + G_r - P_N - \mathrm{IL} - \mathrm{FM}, \tag{1.7}$$

where P_t is the transmit power, G_t and G_r are the antenna gains, $\mathrm{PL}(d)$ is the path loss at a distance d, P_N the noise power, IL the implementation loss and FM the fading margin. These values are given in table 1.1 for two 60 GHz examples and are discussed in the following.
The SNR is calculated by subtracting received power from received noise. An SNR between 10 dB and 15 dB is considered to be sufficient in order to achieve data rates in excess of 1 Gbit/s over a 1.88 GHz bandwidth, when simple single carrier or impulse modulations are employed [8, 14, 31].
The transmit power P_t is assumed to be 8 dBm. This represents a value a low-power output amplifier realized in sub-micron CMOS technology can provide without entering compression.
As discussed in section 1.2.3, at 60 GHz even an antenna having a small effective area A_e is very directive. If omnidirectional antennas are used, the achievable link distance is prohibitively small. Thus, the gain of transmit and receive antenna, G_t and G_r, are set to 15 dBi for the following calculations. This is a value that can be achieved by an antenna array of reasonable size, integrable in package. The corresponding effective area is $A_e = 62.91\,\mathrm{mm}^2$.
The noise term P_N in equation (1.7) is given by

$$P_N = 10\log_{10}(kBT) + \mathrm{NF}. \tag{1.8}$$

The first part corresponds to the thermal noise power over the channel bandwidth $B = 1.880$ GHz. Due to this ultra wide bandwidth, a quite

Parameter	Value	
Bandwidth B	1.880 GHz	
Transmit power P_t	8 dBm	
Receive antenna gain G_t	15 dBi	
Transmit antenna gain G_r	15 dBi	
Noise power P_N	−74 dBm	
SNR	10 dB	
Implementation IL	6 dB	
Fading FM	3 dB	
Path Loss at 1 m $\mathrm{PL}(d_0)$	68 dB	
Resulting path loss $\mathrm{PL}(d_{max})$	88 dB	
	LOS	NLOS
Pathloss exponent n	2	4
Maximum achievable distance d_{max}	10 m	3.16 m

Table 1.1: Parameters for link budget analysis and obtained maximum distance

large value of -81.09 dBm at room temperature $T = 300\,K$ is obtained. This is one of the reasons due to which the distance of UWB communications stays low, provided that the total signal power is not increased proportional to bandwidth. The second part of (1.8) is the receiver noise figure NF, which is added to the thermal noise level due to noise added by the receiver front-end. The CMOS receiver front-end designed as part of this thesis is expected to achieve a noise figure of around 7 dB (cf. sections 4.2 and 5.2).
Due to the reasons given in section 1.2.3, which include strong attenuation and very directive antennas, the interference level which is usually added to thermal noise in link budget calculations is expected to be very low in the 60 GHz band. Thus, interference is neglected here.
The term IL in (1.7) accounts for implementation loss. It originates from non-idealities of the transceiver that degrade the signal, like nonlinearity in the front-end and phase noise of the local oscillator. An implementation loss of IL = 6dB is assumed [15].
The factor FM represents the fading margin. As fading decreases with channel bandwidth, the FM remains as low as 3 dB for a channel bandwidth of 1.880 GHz [29].
The path loss PL as a function of distance d is given by the pathloss exponent model [34] according to

$$PL(d) = PL(d_0) + 10\,n \log_{10}\left(\frac{d}{d_0}\right) + X_\sigma, \tag{1.9}$$

where n is the path loss exponent and X_σ is the shadowing parameter. The reference path loss at a close reference distance d_0 corresponds to the free space path loss [27] given by

$$PL(d_0) = 20 \log_{10}\left(\frac{\lambda}{4\pi d_0}\right). \tag{1.10}$$

The path loss exponent n, which equals 2 in the case of ideal free space propagation, depends on the environment due to constructive and destructive multipaths and additional attenuation . The final report of the sub-committee responsible for channel modeling for the IEEE 802.15.3c standard gives a good summary of 60 GHz indoor channel properties [36]. It shows that for LOS indoor channels, the path loss component n varies from 1.2 to 2.0 [36]. For NLOS environments, n lies between 1.97 and 10. An exhaustive list of the different cases can be found in [37], summarizing published measurements and models that were considered by the sub-committee.
For outdoor environments with distances not exceeding several hundred meters, Smulders et al. [31] show that the LOS value for n lies somewhere between 2 and 2.5, thus ideal free space propagation gives a good approximation.
For the following considerations, one LOS indoor/outdoor channel with $n = 2$ and one indoor NLOS channel with $n = 4$ are taken as example. Similar values for n are likely to appear in typical 60 GHz environments.
Due to the variation in the surrounding environments, the received power will be different from the mean value by the shadowing parameter X_σ [36]. In the following, X_σ will be neglected and only the mean value is taken into account. However, depending on the environment, several dB of shadowing margin could become necessary for a more pessimistic estimation.

Table 1.1 summarizes the parameters introduced above. Two maximum distances d_{max} are obtained by evaluating (1.7) for the LOS and NLOS path loss exponent. The LOS transmission allows a distance of 10 m, while in the NLOS case only 3.16 m are achieved in the given configuration.
However, the situation is different if blockage is present, which was not yet included in (1.7): if the LOS path is blocked, e.g. by a human being that can introduce loss as high as 36 dB [15], the maximum LOS distance drops well below 1 m. Thus, reflections need to be exploited. If this is done by pointing directive receive and transmit antennas to the spot where the strongest reflection occurs, the NLOS path loss exponent n can be considerably decreased (down to around $n=2$ in highly reflecting environnements). Thus, an increase of NLOS distance beyond the calculated value is possible.
The considerations of this section show that even for short UWB links in the 60 GHz band, considerable technological effort is necessary. Highly directive antennas with adaptable beam direction are necessary if transmit power shall remain low. A low power RF front end has to be optimized with respect to receiver noise figure and oscillator phase noise to maximize the attainable distance.

1.4 THE RADIO INTERFACE

The previous sections introduced the properties of the ultra wide, unlicensed 60 GHz band. This band is ideally suited for the applications proposed in section 1.1, provided a low power, low cost radio interface that allows UWB communication can be developed. Until recently, this was not the case: the most integrated solutions to convert a signal from and to the 60 GHz band were based on costly and power consuming compound semiconductor Monolithic Microwave Integrated Circuits (MMICs). An on-chip integration together with digital and mixed-signal baseband circuitry was not feasible, which further increased cost and complexity of a potential 60 GHz radio interface.
Today, the situation is different: starting from the 130 nm node, CMOS technology exhibits unity gain frequencies sufficiently high for the

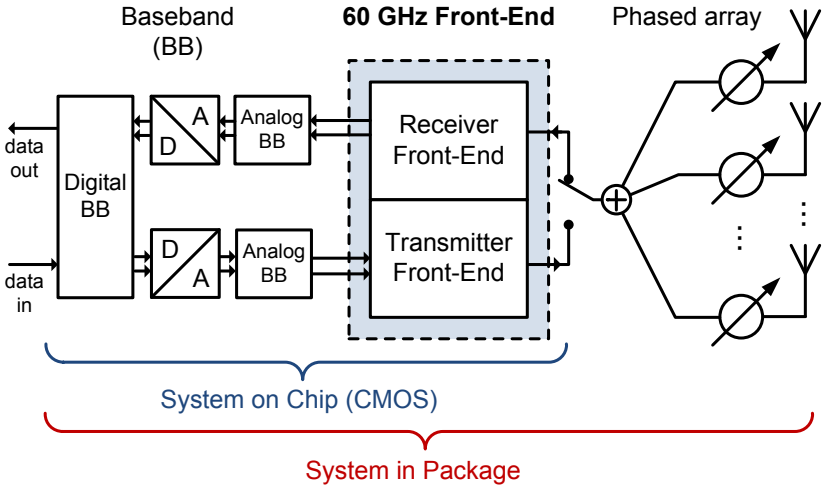


Figure 1.7: The proposed 60 GHz radio interface, whose 60 GHz transceiver front-end (highlighted in grey) is the subject of this thesis

realization of mm-wave Radio Frequency Integrated Circuits (RFICs) [12],[17]. The 65 nm CMOS node turns out to be perfectly suited for low-power circuits operating in the 60 GHz band (cf. chapter 3). As this technology also allows the implementation of the low power, high speed baseband circuitry, a completely integrated System on Chip (SoC) solution becomes feasible. This is essential to avoid interconnect issues and to further minimize mass production cost. Figure 1.7 shows the block diagram of an integrated low power radio interface. The Baseband (BB) and mm-wave circuitry together form a SoC that will be realized in 65 nm CMOS technology.
The principal functions of the digital baseband are modulation and demodulation, equalization, channel estimation, error correction and synchronization. (More specifically, the reconfigurable impulse UWB baseband presented in [8] is one option. Alternatively, digital BBs that use single or multi carrier modulation schemes can be used). The digital baseband is connected to Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) that provide the transition to the analog domain. Two channels are necessary if quadrature modulation is employed as indicated in figure 1.7.
The analog baseband, which is connected to the converters, provides variable gain amplification to raise the received signal level to the converter's full scale, and low-pass filtering to reduce the noise bandwidth. Additional analog blocks can implement parts of the synchronization and equalization functionality [14, 35], if this is not done in the digital BB. The bandwidth required for the BB circuitry corresponds to the channel bandwidth of 1.88 GHz (cf. section 1.5) divided by two, because an upper and lower sideband is created around the carrier frequency.
The block diagram of the 60 GHz front-end is discussed in detail in chapter 2, since it is realized in the framework of this thesis. It implements the up-conversion from BB to one of the channels in the 60 GHz band.
A phased array, including low loss phase shifters for beam steering and an array of planar antennas, is integrated into one single package together the CMOS circuit in order to achieve a compact, low cost SiP. A SoC integration of the phased array is not desirable: the high substrate loss in bulk CMOS technology decreases antenna efficiency, and the large size compared to the transceiver circuit increases cost considerably. If electronic beam steering is not necessary due to manual alignment of antennas, the phase shifters are obsolete. However, a single antenna is not sufficient to achieve the effective area needed to address the targeted applications (cf. previous sections).
The development of the radio interface shown in figure 1.7 is the essential part of a research effort whose goal is to show the suitability of the 60 GHz band for the applications of section 1.1. The key issues are low power consumption, very high data rate, and low cost integration. They provide the guidelines for the optimization of individual circuit blocks, which always have to be seen in a system context. At longer term, WSNs containing multiple nodes which use the proposed radio interface are targeted.

Part one of this thesis describes the contribution to the design of the 60 GHz front-end that is highlighted in figure 1.7. The choice of the front-end's architecture, based on a thorough literature review ad a discussion of the suitable possibilities, is presented in chapter 2. Chapter 3

describes the conditions of 60 GHz circuit design in 65 nm CMOS technology. Available and full-custom devices are also introduced. Chapter 4 presents the details of the front-end's key building blocks. They are developed in the framework of this thesis. Their performance is evaluated and compared to the state of the art. Chapter 5 presents the first steps towards an integration of the complete 60 GHz RF front-end.
The second part of this thesis describes research work concerning behavioral modeling of the 60 GHz front-end. System level models are necessary to represent the behavior of the transceiver circuits in simulations of the entire radio interface.

2 60 GHZ TRANSCEIVER FRONT-ENDS: STATE OF THE ART AND ARCHITECTURE CONSIDERATIONS

This chapter serves two purposes: On the one hand, it reviews the state-of-the-art of integrated 60 GHz front-ends implemented in silicon-based technologies. Since the circuits developed as part of this thesis are based on a 65 nm CMOS technology, the focus lies on CMOS realizations. Nevertheless, some important work in Silicon Germanium (SiGe) / BiCMOS technology is also mentioned. While section 2.1 provides a brief historical literature review, the later sections include references to published work that implements a certain front-end architecture.
On the other hand, a front-end architecture suitable for the low-power, high data-rate applications discussed in chapter 1 shall be chosen. To this end, section 2.2 establishes the requirements the front-end has to meet. Then, possible topologies for 60 GHz receivers and transmitters are reviewed in sections 2.3 and 2.4. On this basis, a suitable architecture is chosen. The adopted solution is discussed in detail in section 2.5.

2.1 HISTORICAL INTRODUCTION

Transceiver circuits operating in the 60 GHz band have been existing for several decades now. As early as 1975, Y.-W. Chang *et al.* published a solid state mm-wave transmitter module that is able to transmit at 4 Gbit/s providing 500 mW of output power at 60 GHz [38]. While their circuit uses silicon-based active devices (an IMPATT oscillator, a two stage p-i-n diode quadriphase modulator and a three stage IMPATT amplifier), the components are not integrated on a common substrate, but individually assembled and connected by waveguides.
A monolithically integrated Gallium Arsenide (GaAs) 60 GHz transceiver was published in 1989 by A. Colquhoun *et al.* [39]. The used active devices are Schottky diodes and MESFET transistors. Passive elements like branchline couplers, transmission lines and spiral inductors are used for power division and matching. Compound semiconductor based MMICs were since then used for 60 GHz transceiver circuits [40]. As recently as 2004/2005, Zirath *et al.* and Gunnarsson *et al.* (both from Chalmers University, Göteborg, Sweden) reported highly integrated 60 GHz transceiver circuits based on GaAs pseudomorphic High Electron Mobility Transistors (pHEMTs).
Since the early first decade of the 21st century, silicon based 60 GHz RFICs are used to built 60 GHz transceiver front-ends [41]. The main advantage is low cost in mass production, low power consumption compared to compound semiconductors, and the possibility of an integration together with digital baseband circuitry [17].
The earliest silicon-based 60 GHz front-end RFICs are implemented in SiGe technology: in 2004, S. Reynolds and his colleagues from the IBM research center in Yorktown Heights, US, published their first SiGe bipolar transceiver circuits working in the 60 GHz band [42–44]. IBM continued its research efforts, yielding an advanced next generation transceiver [45], and finally phased array SiGe receivers in 2010 [46, 47]. Later, they also implement a 60 GHz CMOS front-end [48].

Also in 2004, researchers of S. Voinigescu's group at the University of Toronto, Canada, published their first 60 GHz SiGe transmitter/receiver circuits [49, 50]. They make heavy use of spiral inductors and transformers [51]. This approach indicates the change from the thitherto very common MMIC paradigm to RFIC design techniques even at mm-wave frequencies. The research of this group on SiGe circuits continued towards higher mm-wave frequencies [52].
Other important contributions to the research on 60 GHz circuit design, this time in SiGe:C BiCMOS technology, originate from IHP GmbH, Frankfurt (Oder), Germany. Starting also in 2004 with circuits supporting simple modulation schemes [53–55], their subsequent publications show SiGe:C based front-ends for an OFDM communication system [56–58].
In this context of mm-wave SiGe front-ends, the work of A. Hajimiri's group at California Institute of Technology in Pasadena, US, on a 77 GHz phased array transceiver is worth mentioning: in 2006, and until today, this circuit shows the by far highest degree of integration in SiGe BiCMOS technology at mm-waves [59, 60].

The development of 60 GHz transceivers in CMOS technology gained momentum with the publication of "Millimeter-Wave CMOS Design" by C.H. Doan, S. Emami *et al.* in early 2005 [61]. It shows the feasibility of 60 GHz RFICs using the 130 nm CMOS node. In 2007, a 60 GHz CMOS front-end receiver was published by the same authors [62]. This work was accomplished at Berkley Wireless Research Center (BWRC), US, under the direction of A. M. Niknejad and R. W. Brodersen and resulted in the foundation of SiBEAM[1]. The continued research on 60 GHz CMOS circuits at BWRC yielded a low-power receiver in 2008 [63] and a highly integrated transceiver including baseband circuitry in 2009 [64, 65].
The first 60 GHz receiver in CMOS, however, was already published in early 2005 by B. Razavi from University of California, LA, US [66–68]. While this circuit uses a direct conversion architecture (cf. section 2.4.4) and is implemented in 130 nm CMOS, subsequent research by Razavi and his students investigates other topologies and use lower-scale CMOS technologies.
Another early 60 GHz receiver was published in 2006 by D. Alldred *et al.* of S. Voinigescu's research group at the University of Toronto, Canada [69]. Like the 60 GHz SiGe circuits of this research group, their 60 GHz CMOS radio makes heavy use of small spiral inductors and transformers for matching [69]. After they clearly showed the advantage of designing mm-wave RFICs using lumped elements [51], this technique was widely adopted by other designers and is also used in this thesis (cf. section 3.4 for a detailed discussion of this topic). Subsequent research within Voinigescu's group lead to the publication of a more complete 60 GHz transceiver in 65 nm CMOS by A. Tomkins *et al.* [70, 71], though recent research on CMOS circuit design in Voinigescu's group mainly concerns frequencies well above 60 GHz [72].
The National Taiwan University in Taipei, Taiwan, also participated from the beginning in the research efforts concerning 60 GHz CMOS transceivers [41]. As early as 2007, C.H. Wang *et al.* published a 60 GHz six-port transceiver in 130 nm CMOS technology (cf. to section 2.4.7 for more details on this architecture). Subsequently, National Taiwan

[1] SiBEAM Inc., www.sibeam.com

University's researchers published various receiver and transceiver circuits, implementing quite inventive topologies [73–76]. In addition to these circuits at 60 GHz, in 2010, Y.-A. Li *et al.* showed the feasibility of a 77 GHz Radar system in 65 nm achieving a detectable range of 106 m [77].
In 2007, Mitomo *et al.* of the Toshiba Research and Development Center, Japan, published the first 60 GHz CMOS receiver with integrated frequency synthesizer. The same research group achieved a 77 GHz Frequency Modulated Continuous Wave (FMCW) [78] radar transceiver in 2009 [79].
A 60 GHz radio published in 2008 by S. Pinel, S. Sarkar *et al.* shows the integration of a complete transceiver front-end together with baseband, digital signal processor, DACs and ADCs [80, 81]. It was developed by the research group of J. Laskar at Georgia Electronic Design Center (GEDC), Georgiatech, US. GEDC's researchers also published 60 GHz radio front-ends in SiGe and CMOS technology using non-coherent detection [82, 83]. The paper of D. Dawn *et al.* from GEDC presents considerations on integrated 60 GHz transmitter design [84].
Apart from these early contributions of some of the key institutions that do research on silicon-based 60 GHz circuits, a multitude of other 60 GHz transmitters and receivers have been published. They employ CMOS technologies down to the 45 nm node (e.g. J. Borremans *et al.* from IMEC, Belgium) and use techniques as exotic as an injection locked 60 GHz pulse transmission (e.g. implemented in 65 nm CMOS Silicon On Isolator (SOI) technology by N. Deparis of IEMN in Lille, France). A substantial part of the published work on these circuits is referenced in sections 2.3 and 2.4, where architectures suitable for 60 GHz CMOS front-ends are reviewed.

As illustrated in chapter 1, integrated phased array antennas are necessary for most 60 GHz applications in order to achieve a sufficient range. Some work on SiGe-based phased array transceiver front-ends at 60 GHz and 77 GHz is cited in the part on SiGe circuits above. But also in CMOS technology the on-chip integration of transceivers together with active phase shifters (and sometimes even on-chip antennas) becomes an important research topic. Related work was published for example by K. Scheir *et al.* from IMEC, Belgium [85, 86], Y. Yu *et al.* from University of Eindhoven and NXP Semiconductors, Netherlands [87], S. Kishimoto *et al.* and M. Tanomura *et al.* from NEC, Japan [88, 89], E. Cohen *et al.* from Technion, Israel [90–92] or W.L. Chan *et al.* from Delft University, Netherlands [93].
However, as this thesis is only concerned with the CMOS transceiver front-end (phase shifters and antennas are planned to be outside the CMOS chip, see section 1.4), a further discussion of these phased array transceivers is not included here.

2.2 FRONT-END REQUIREMENTS

As indicated in section 1.4, high data-rate capabilities, low cost (and hence small circuit size), very low power consumption and complete integrability are the key requirements for the 60 GHz transceiver front-end. Furthermore, the chosen transmitter has to be able to provide an output signal that respects the IEEE 802.15.3c channel limits. The consequences on the front-end's architecture are manifold:

- low complexity is required to decrease the device count and thus power consumption and circuit size
- all circuit blocks need to be realizable in CMOS, forbidding components that require low tolerance or a high quality factor (the only exception is a reference resonator that is necessary in any case to create the clock frequency for the digital circuit part)
- to achieve very high data-rates, the spectrum needs to be used efficiently even though ultra-wide bandwidth is available in the 60 GHz band
- the implementation of certain architectures (for example Software Defined Radio (SDR) with analog-to-digital conversion in the RF band) require technologies with cutoff frequencies several times higher than the carrier frequency, rendering their use for 60 GHz radios impossible

In addition to these general requirements, certain limitations are imposed on the choice of the modulation schemes: while there is not one modulation explicitly specified, the impulse-based BB circuit developed for the radio interface (cf. doctoral thesis of A. Lecointre [8]) must be supported by the front-end. Furthermore, also modulations based on continuous carriers should be feasible, because they are better suited to support data rates of multiple Gbit/s within the channels introduced in section 1.2.2. Thus, the chosen front-end architecture needs to be very versatile and able to support various modulation schemes.

2.3 Transmitter Architectures

In the following, various architectures suitable for 60 GHz transmitter front-ends are reviewed, and work that is employing the respective front-end at 60 GHz is cited. Refer to [78, 94, 95] for further details on these architectures.

2.3.1 *Impulse Radio Transmitter*

Rather then changing the properties of one or several continuous wave carriers, impulse radio transmitters transmit transient impulses of finite duration [96, 97]. The information is contained either in position (in the case of Pulse Position Modulation (PPM)), polarity (for Binary Phase Shift Keying (BPSK)), shape (for Pulse Shape Modulation (PSM)), amplitude (for Pulse Amplitude Modulation (PAM)) or, in the special case of On-Off-Keying (OOK), in the simple fact that an impulse is transmitted.
In order to achieve very short pulses, ultra wide bandwidth is required. Thus, the unlicensed frequency band between 3.1 and 10.6 GHz is the most prominent example for the use of this modulation scheme, because the very high relative bandwidth of this band allows the use of very short monocycle impulse forms [8, 97, 98].
While their absolute bandwidths are about equivalent, the 60 GHz band exhibits a considerably lower relative bandwidth than the band between 3.1 and 10.6 GHz. This implies that monocyle impulses are not a viable option at 60 GHz: only an impulse shape containing an

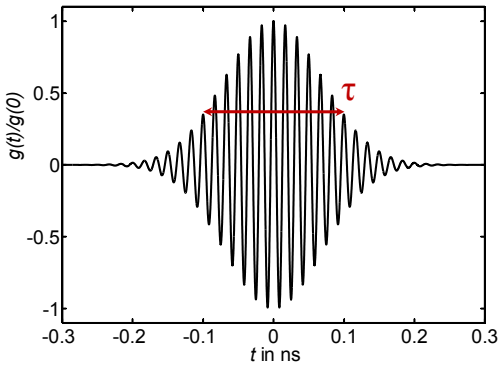


Figure 2.1: Gaussian Impulse for the 60 GHz band

oscillation of multiple cycles meets the spectrum requirements [95]. A typical impulse of this kind is the Gaussian impulse described by

$$g(t) = e^{-\left(\frac{t}{\tau}\right)^2} \cos(2\pi f t), \tag{2.1}$$

where τ determines the impulse's width and f the frequency of the oscillation. Figure 2.1 gives the normalized impulse described by (2.1), parametrized to occupy around 7 GHz of the unlicensed 60 GHZ band. To obtain an impulse that fits one of the IEEE 802.15.3c 60 GHz channels, the impulse width τ has to be increased accordingly.
As discussed by the author of this thesis in [95], this kind of impulse at 60 GHz can be generated in two fundamentally different ways that yield impulses with a fundamental, inherent difference:

1. When using a conversion approach, the envelope waveform (in the case of (2.1) described by $e^{-(t/\tau)^2}$) is generated in the baseband. There, it is used to create a modulated pulse train. Subsequently, this pulse train is up-converted to the 60 GHz band. (A slightly modified form of this transmitter principle uses rectangular control impulses in baseband, that are used to control a mm-wave switch at the output of a 60 GHz oscillator. The rectangular pulses created that way are shaped by a pulse shaping filter at 60 GHz). Because modulation takes place in baseband, a time shift t_0 used to change the impulse position only influences the envelope, while the carrier phase is continuous. The shifted impulse at 60 GHz is thus described by

   $$g_{\text{converted}}(t - \mathbf{t_0}) = e^{-\left(\frac{t-\mathbf{t_0}}{\tau}\right)^2} \cos(2\pi f t), \tag{2.2}$$

   showing that the exact 60 GHz impulse shape depends on the time shift.
   This kind of impulse transmitter front-end is just an application of the direct conversion approach to an impulse-modulated baseband signal. It is thus discussed in section 2.3.2.1 as a special case of the direct conversion transmitter.

2. The other possibility is to generate the pulse waveform shown in figure 2.1 directly at 60 GHz. A multiplication with a carrier signal is thus not necessary. Consequently, a time shift by t_0 delays the whole impulse, including the cosine part. The resulting waveform is

   $$g_{\text{created}}(t - \mathbf{t_0}) = e^{-\left(\frac{t-\mathbf{t_0}}{\tau}\right)^2} \cos(2\pi f (t - \mathbf{t_0})), \tag{2.3}$$

where the impulse shape stays exactly the same regardless the time shift. Architectures that allow the generation of this kind of impulses directly at 60 GHz are discussed in subsection 2.3.1.1.

The difference between the phase of the cosine function in (2.2) and (2.3) has consequences on the coherent demodulation of these kind of signals. While for the conversion approach, the coherent demodulation corresponds to the one in case of a continuous carrier, for the second case a coherent impulse receiver is necessary. This kind of receiver is introduced in section 2.4.3. The non-coherent receiver discussed in section 2.4.1 is suitable for both kind of transmitted impulses, but exhibits inferior performance [95].

2.3.1.1 *Direct Impulse Generation at 60 GHz*

Two possibilities exist to directly generate UWB impulses at 60 GHz. The first one was proposed in 2007 by B.B.M. Wasanthamala Badalawa *et al.* from the University of Japan [99]. Its is based on Monopulse Generators (MPGs) that exploit the propagation delay of CMOS inverter cells to generate ultra-short monocycles [100]. Several of these monopulses need to be delayed, added and low-pass filtered in order to generate a waveform similar to the one shown in figure 2.1.
The topology of this kind of pulse transmitter is given in figure 2.2. Each MPG generates a short monopulse, whose amplitude and length is chosen when dimensioning the MPG. At the output of the MPGs, the delayed monopulses are summed up to form the 60 GHz impulse, whose form is optimized by the subsequent LC filter. The Power Amplifier (PA) increases the output power level.
As the digital input initiates the generation of an impulse, but cannot modify its shape or amplitude, the basic version of this transmitter as depicted in figure 2.2 is limited to modulations like PPM and OOK. Another disadvantage is that the impulse bandwidth and center frequency are prone to process tolerances (there is no high-precision oscillator that serves as reference). Furthermore, spectral efficiency is low. The first reason thereof is inherent to impulse transmission, and consists in the fact that the spectrum of the impulse usually does not allow a constant, high power density over the entire communication channel. The second reason is that two orthogonal impulses are not feasible, because the phase of the oscillation contained in the impulse depends on its shape and position. This latter mechanism divides the spectral efficiency by two.
Advantages of circuits using this architecture are their small size, their low average power consumption (due to the absence of a continuous carrier) and their low complexity.

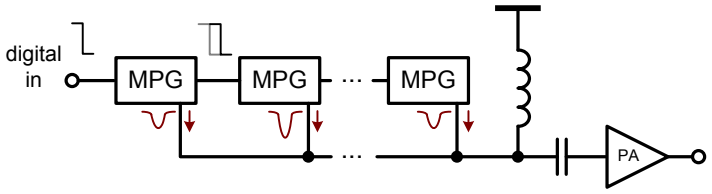


Figure 2.2: 60 GHz pulse transmitter based on Monopulse Generators (MPGs)

The second possibility to directly generate 60 GHz impulses uses a mm-wave oscillator whose startup is initiated by a baseband impulse with short transient time. It was proposed by N. Deparis *et al.* from IEMN, Lille, France in 2007 [101]. First implemented in a pHEMT GaAs technology [101–103] using a 30 GHz oscillator and a frequency doubler, the topology was later on also realized in 65 nm CMOS SOI technology using a 60 GHz oscillator [104].
As indicated in figure 2.3, rather than starting arbitrarily from noise, the oscillator's start-up is initiated by the rising edge of an impulse with fast transition time. This controlled start-up is possible as the frequency spectrum of the impulse contains, due to its steep slope, an energy density well above the noise level at the resonance frequency f_0 of the oscillator. As the oscillation condition is only ensured during the duration of this baseband impulse, its width determines the width of the 60 GHz impulse. If a Voltage Controlled Oscillator (VCO) is used, f_0 can be adjusted by a control voltage.
Due to the fact that the oscillation is initiated abruptly by the baseband impulse's rising edge, its phase is well-defined and the 60 GHz impulse's shape is always the same. Its carrier shifts with the envelope as illustrated in equation (2.3).
One disadvantage of this kind of transmitter is the quite limited number of possible modulations, all of which exhibit low spectral efficiency. Furthermore, process tolerances limit its benefits: firstly, the impulse shape varies due to variation of the transistor's properties. Secondly, the VCO's center frequency differs between different chips for the same control voltage. The synchronization to a very stable reference oscillator is handicapped by the fact that a carrier with continuous phase is not available.
The use of the sub-harmonic injection locking technique, as proposed in [101–104], is no remedy: the reason for this is that the harmonic frequencies on which the oscillator locks are created by the Pulse Repetition Frequency (PRF) of the baseband impulses. Hence, not only the carrier phase is locked to a precise reference, but also the position in time of the impulses that carry the information. In the frequency domain, rather then obtaining one single, very pure spectral line (which is desired in classical transmitters as carrier), the continuous spectrum of a single 60 GHz pulse serves as envelope of a discrete line spectrum that is obtained at the transmitter output. This line spectrum results from the periodicity of the 60 GHz pulse train. The frequency spacing between two lines is the PRF.
Thus, despite the locking technique proposed by Deparis *et al.*, the 60 GHz pulse train is still centered around the frequency f_0 of the unlocked VCO, and the low phase noise of each of the spectral lines does not increase the quality of the transmitted signal.

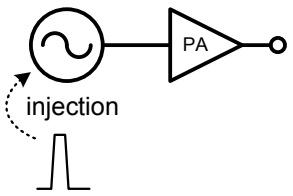


Figure 2.3: 60 GHz impulse transmitter based on a mm-wave oscillator with fast, impulse-triggered start-up

If the above mentioned limitations can be tolerated (which are by the way also present in the impulse transmitter described in the previous section), the implementation of this transmitter architecture exhibits nevertheless several advantages: they include its very low power consumption due to the absence of a continuous carrier, a high peak output power (which can render the use of a power amplifier obsolete), small circuit size and low complexity.

2.3.2 *Direct Conversion Transmitter*

Figure 2.4 illustrates the principle of a direct up-conversion architecture [78, 94]: the in-phase (I) and quadrature (Q) components of the baseband signal are multiplied by two Local Oscillator (LO) signals that are 90° out of phase. Thus, the I and Q signals are quadrature-modulated on the carrier and up-converted to the communication frequency band simultaneously. The frequency of the LO signal is equivalent to the center frequency at the receiver output. The band-pass filter deletes mixer spurs and out-of band components of the RF signal. This functionality can also be realized by the frequency-selective nature of the PA. The PA amplifies the RF signal to obtain the desired output level.
The use of this quadrature architecture permits to obtain different signals in the Lower Sideband (LSB) and Upper Sideband (USB), thus doubling the spectral efficiency of the output signal. If a low complexity transmitter is desired, the implementation of one single branch of the architecture depicted in figure 2.4 is possible. However, this is at the expense of spectral efficiency. Sub-section 2.3.2.1 discusses this kind of transmitter for direct impulse up-conversion.
In a fully integrated transmitter, the LO signal is generated by an on-chip VCO, which has to be synchronized to a very accurate reference signal by a feedback loop, i.e. employing a Phase Locked Loop (PLL)-based synthesizer circuit. Otherwise, sufficient stability cannot be ensured due to frequency drift with time and temperature.
The direct up-conversion architecture suffers from an important drawback: as the spectrum at the output of the PA is centered around the frequency of the VCO, injection pulling (also called injection locking, cf. to [105] for details) occurs [78, 94]. The impact of this phenomenon depends on the amount of parasitic coupling from the PA output to the VCO: if strong interfering signals around the oscillation frequency are present in the VCO circuit, they perturb its output spectrum and lead to frequency drift. To avoid this problem, other architectures with LO frequencies outside the RF frequency band can be employed (cf. section

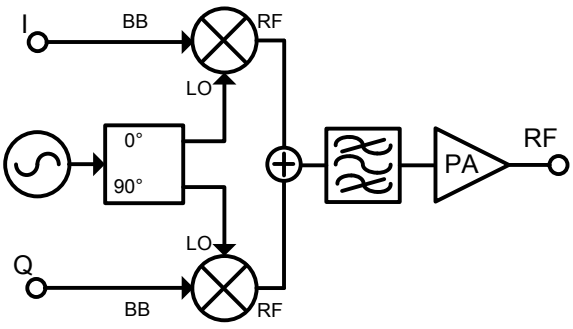


Figure 2.4: Simplyfied architecture of a direct conversion transmitter

2.3.3). Alternatively, the LO signal can be generated by a VCO at a fraction of the LO frequency, followed by a frequency multiplier. If the direct conversion architecture of figure 2.4 is used, circuit techniques to achieve high isolation between PA and VCO can alleviate the problem.
The advantages of a direct conversion transmitter front-end are its versatility, allowing the use of a variety of different modulations (including the efficient up-conversion of baseband impulses), its spectral efficiency and its rather low complexity compared to two-step up-converters, permitting low chip size and low power consumption.
Especially due to its low complexity, requiring only very few basic mm-wave building blocks, this architecture is implemented in many early 60 GHz transmitters: at the University of Toronto, Canada, the first SiGe transmitter by C. Lee *et al.* employ direct BPSK modulation [49]. The direct conversion approach is also used for the 60 GHz CMOS transceiver of A. Tomkins *et al.* [70, 71].
At UCLA, US, B. Razavi uses this architecture for an early 60 GHz transmitter [68]. At the University of Melbourne, Australia, a quite complete direct conversion transceiver was implemented [106–108]. The highest degree of integration of a transceiver using the direct conversion architecture is demonstrated by researchers of the University of California, Berkeley, in the papers of C. Marcu *et al.* [64, 65].
The simplicity of this architecture is also the reason of its use in phased array transmitters: Researchers at NEC, Japan, first presented a single direct conversion transmitter [89], and later on an antenna array using this kind of architecture [88]. At Delft University, Netherlands, H.-Y. Chan *et al.* use the direct conversion approach with phase-shifted LO for a beam-forming front-end [93].
Researchers of the National Taiwan University, Taipei, make use of a less straightforward version of the direct conversion transmitter: in their 2007 paper, Wang *et al.* show a 60 GHz CMOS transmitter that uses a reflection-type I/Q modulator as up-converter [109]. The reflection-type I/Q modulator is composed of two reflection type BPSK transmitters using LO inputs that are 90° out of phase. Details on this modulator can be found in [110].

2.3.2.1 *Direct Conversion Architecture for Impulse Transmission*

Due to its ability to convert an arbitrary waveform to a desired frequency band, the direct conversion architecture is also suitable for 60 GHz impulse transmitters. The fundamental difference between this conversion approach and a direct impulse generation is discussed in section 2.3.1 and in [95].
Figure 2.5 shows a frequently employed architecture for impulse conversion transmitters. It corresponds to one branch of the quadrature

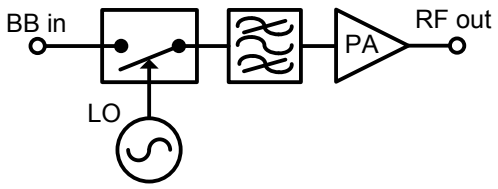


Figure 2.5: Simple direct-conversion impulse transmitter using a mm-wave switch

direct conversion transmitter, where the mixer is replaced by a simple mm-wave switch. Rather than performing an amplitude modulation, the carrier is either passed through or not. Modulation schemes are thus limited to OOK and PPM. After the switch, a bandpass filter is required to shape the impulse.
The most important advantage of this architecture is its simplicity: lower power consumption and lower circuit size with respect to a quadrature direct conversion transmitter can be achieved. The continuously enabled VCO allows a synchronization to a reference oscillator, which is not possible for direct 60 GHz impulse transmitters (cf. section 2.3.1.1). These advantages are accompanied by disadvantages like poor spectral efficiency due to the single-phase carrier and the simple modulation schemes employed. Furthermore, the direct impulse transmitters presented in section 2.3.1 can achieve even lower power consumption, due to the fact that they completely switch off the oscillator during the pause between impulses.
Several 60 GHz transmitters using this architecture are found in literature, especially for the implementation of OOK modulation: W. Winkler *et al.* from IHP, Germany, present switch, PA and VCO constituting this transmitter in SiGe:C technology [53, 54]. Research activities by N. Deparis, M. Devulder *et al.* at IEMN, Lille, France investigated impulse-based communication in the 60 GHz band. The resulting transmitters were first realized in GaAs pHEMT [111] and later in SiGe technology [112].
E. Juntunen et al. from Georgiatech, US [83] and J. Lee *et al.* from University of Taiwan, [75] also published direct conversion impulse transmitters.

2.3.3 *Two-step Transmitter*

Figure 2.6 shows the block diagram of a two-step transmitter [94]. The first stage resembles a direct conversion transmitter, but converts to a lower Intermediate Frequency (IF) f_1 rather than directly to the output frequency. In addition to the first conversion, this part provides quadrature modulation. The second mixer up-converts the signal to the output frequency $f_1 + f_2$. During this conversion step an unwanted image sideband at $|f_2 - f_1|$ is created, which has to be removed by a very selective bandpass filter.
This architecture provides several advantages over the direct conversion receiver (while maintaining its features by supporting a large number of modulation schemes, including impulse up-conversion): most im-

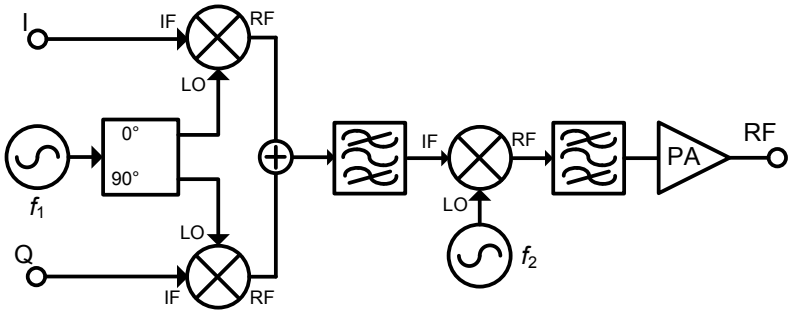


Figure 2.6: Two-step transmitter front-end using two different LO frequencies

portantly, as both f_1 and f_2 are far from the frequency range of the PA, injection locking is not a major issue. Also, since both LOs work at lower frequencies compared to a direct conversion transmitter, I and Q matching is superior and a higher spectral purity of the carrier can be achieved.
However, there are two major drawbacks that come along with these advantages: Firstly, the image rejection necessitates a high quality bandpass filter, which passes only the wanted sideband around 60 GHz. The on-chip integration of this filter is a considerable challenge, especially if the intermediate frequency f_1 is close to the output frequency. The second drawback is the high complexity of a two-step transmitter, causing high cost (due to increased chip size and a more elaborate design) and high power consumption.
Historically, two-step transmitters (and, more importantly, heterodyne receivers, as discussed in section 2.4.5) use a fixed IF in order to allow the use of an IF bandpass filter with narrow passband and steep slopes at a constant center frequency. Thus, f_1 is fixed while f_2 is variable to allow channel selection. This kind of fixed-IF two-step transmitter front-end is implemented in the transceivers of Georgiatech, US, [80, 81, 84] and the transmitter front-end of M. Kärkkäinen *et al.* from Helsinki University of Technology, Finland.

2.3.3.1 *The sliding IF architecture*

In the case of an integrated implementation of a two-step transmitter (and also receiver) at 60 GHz, a fixed IF provides fewer advantages. A often used alternative, which creates the two LO frequencies f_1 and f_2 from a single oscillator at f_0, is illustrated in figure 2.7. The higher LO frequency is $f_2 = Nf_0$, while the IF frequency is $f_1 = f_0/M$. Two-step transmitters (receivers) using this kind of frequency generation are often called "sliding IF" transmitters (receivers).
They provide several advantages: As the LO signal for all mixers can be derived from the same oscillator, only one synthesizer is necessary. The output of this synthesizer does not need to provide quadrature phases, as the first conversion step can obtain them as by-product of the frequency division (the first conversion realizes the I/Q modulation and uses a LO frequency lower than the one provided by the synthesizer), and the second conversion step does not require them. An additional advantage is that the oscillator's frequency f_0 can be quite low, facilitating the VCO design and improving its phase noise characteristics.
Drawbacks are that, due to the fact that the IF is changing, the quadrature mixers need to exhibit a very broadband behavior. In addition,

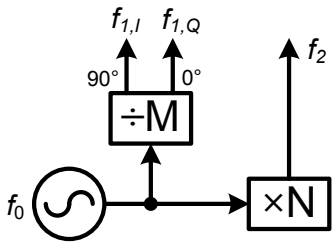


Figure 2.7: Frequency generation from a single synthesizer using dividers and multipliers

the LO distribution, division and multiplication constitute some design challenges.
The most prominent example of a sliding IF transmitter is given by IBM. Their SiGe transceiver, published by S. Reynolds *et al.*, uses a PLL working around 17 GHz and derives the required LO frequencies from its output frequency, by both a multiplication by $N = 3$ and a division by $M = 2$. Their CMOS transceiver, published by Valdes-Garcia *et al.*, uses the same architecture [48].
A. Parsa and B. Razavi propose a new architecture for the 60 GHz band, also with varying IF. However, they avoid multipliers and dividers by using an LO of $f_1 = f_2 = f0 = 30$ GHz. To realize quadrature modulation, a poly-phase filter dephases the RF signal path. Further details concerning this architecture can be found in [113].
60 GHz heterodyne receivers that use a sliding IF are discussed in section 2.4.5.

2.4 Receiver Architectures

This section details various receiver front-end architectures suitable for integrated 60 GHz CMOS receivers. The explications are accompanied by references towards sucessful implementations of these architectures in 60 GHz receivers and transceivers. Subsection 2.4.8 discusses subharmonic mixing, which can be employed in different receiver and transmitter architectures.

2.4.1 *Non-Coherent Receiver*

The simplest form of receiver is a non-coherent detector, which does not multiply the received signal by the carrier, but determines the envelope that modulates the 60 GHz carrier.
The principal architecture of this kind of non-coherent receiver is given in figure 2.8. In a highly integrated solution, the input filtering can be carried out by the antenna and the Low Noise Amplifier (LNA) due to their frequency-selective nature. The low noise amplification is necessary to achieve sufficient sensitivity. The low-pass filter removes the remainders of the RF signal.

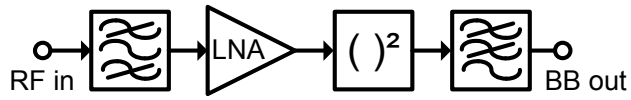


Figure 2.8: Block diagram of a non-coherent receiver front-end

Different implementations of the power detector in CMOS and SiGe technology at 60 GHz are found in literature: S. Sarkar *et al.* from Georgiatech, US, use a diode as square law detector in SiGe [82], while E. Juntunen *et al.* of the same institute [83] use a transistor-based self-mixer in CMOS. M. Devulder, N. Deparis *et al.* from IEMN, Lille, France, also employ diodes in their impulse detectors [101, 112]. The non-coherent impulse receivers presented by A. Oncü from the University of Tokyo exploits the nonlinearity of amplifiers to rectify the RF signal [114–116]. K. Kang *et al.* from the National University of Singapore propose a differential detector based on MOS transistors [117].
Non-coherent detection allows very low-power, low-cost and low-complexity implementations without the need of a reference oscillator

of appropriate phase. On the other hand, severe drawbacks exist: first, the SNR that can be achieved at the baseband is lower than in coherent receivers due to the lack of a low-noise signal template that is used for down-conversion or detection. Secondly, no information about the carrier phase is available, forbidding demodulation of phase or frequency-modulated carriers. This leads to a limited spectral efficiency, also because quadrature de-modulation is not possible.
The above limitations restrict the use of non-coherent detectors mainly to low-complexity transceivers that demodulate impulse-modulated signals.

2.4.2 *Super-regenerative Receiver*

The super-regenerative receiver was introduced in 1922 by E.H. Armstrong as a cheap means to improve the selectivity and sensibility of non-coherent envelope detectors [118]. The principle is illustrated in figure 2.9: the received signal is coupled to a parallel resonator, whose center frequency is tuned by a variable capacitance. The resonator's loss is represented by R_1. An active device is added to the circuit in such a way that it adds a negative resistance of absolute value $|R_2| < |R_1|$. This causes the circuit to become temporarily unstable. The RF signal is amplified considerably, facilitating the subsequent envelope detection. A quench signal is used to regularly remove the negative resistance from the circuit, thus avoiding saturated oscillation. The mean value of the tank resistance has to stay slightly positive in order to permit the circuit to act like a high gain amplifier rather then an oscillator.

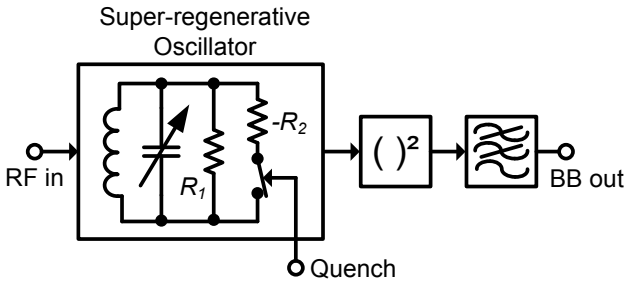


Figure 2.9: Principle of the super-regenerative receiver

The super-regenerative principle is introduced here because it was proposed by K.-H. Lian *et al.* from the University of California, Santa Barbara, US, for the use in a 60 GHz CMOS receiver [119]. It exhibits high sensitivity and low power consumption, and has the potential of low cost integration.
However, its real advantage dates back to a time where the device count needed to be minimized, and thus a high gain had to be achieved employing one single device. Today, integrated high-gain amplifiers can be realized at very low power consumption. They exhibit unconditional stability and much lower signal distortion. The fact that they use a larger number of transistors is less of an issue for integrated solutions.

2.4.3 *Coherent Impulse Radio Receiver*

The previous sub-sections present receivers for non-coherent detection, which are also applicable for the reception of impulse-modulated sig-

nals. However, for optimal detection, a coherent receiver using either a correlation-type demodulator or a matched-filter demodulator needs to be employed [98, 120].

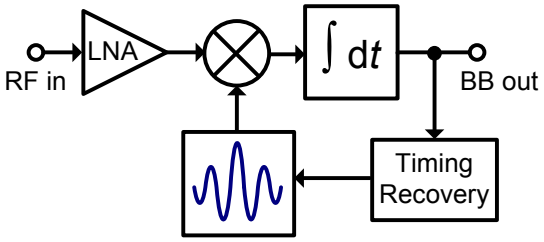


Figure 2.10: Principle of the impulse correlation receiver

Figure 2.10 shows the principle of an impulse correlation receiver: after amplification of the input waveform, the RF signal is directly correlated with a noise-free template waveform that corresponds to the transmitted 60 GHz impulse. The baseband output shows a maximum if an impulse is present at the RF input at the instance of launching the reference impulse [78, 97, 98].
This receiver architecture allows optimal detection of an impulse-modulated signal in an AWGN channel. However, its implementation directly at 60 GHz presents a major challenge due to the fact that the 60 GHz template waveform needs to be launched with very high timing accuracy [95]: if its timing is not synchronized with the incoming pulse train (and this synchronization thus not maintained with very high precision), the detection fails. Note that inaccuracies as small as 4.17 ps, which corresponds to 1/4 of the carrier interval at 60 GHz, result in orthogonality between the received impulse and the template. In this case, the signal is not visible to the baseband circuit. Due to these difficulties, at present no 60 GHz impulse correlation receiver exists in literature.
Nevertheless, the coherent impulse radio receiver can be used in a (either digital or analog) baseband circuit to detect down-converted impulse envelopes, because synchronization timing is less critical here [8].

2.4.4 *Direct Conversion Receiver*

A direct conversion receiver down-converts the RF signals that are situated in the Lower Sideband (LSB) and Upper Sideband (USB) around a carrier frequency f_{LO} in a single step to baseband [78, 94]. As the Intermediate Frequency (IF) is zero in this case, it is also called zero-IF receiver.

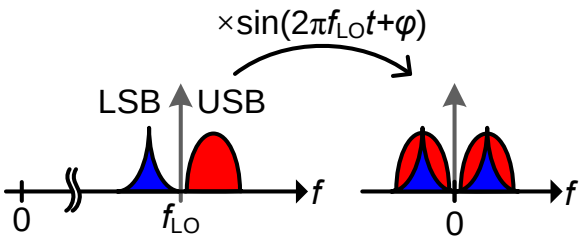


Figure 2.11: Principle of direct down-conversion using a single LO of phase φ and frequency f_{LO}

Figure 2.11 illustrates a direct down-conversion by multiplication of the RF signal with a single carrier of phase φ. In baseband, the signals originating from both sidebands overlap: thus, if LSB and USB spectra do not originate from the same BB signal, they yield an incomprehensible mix of the two sidebands at the receiver output. Furthermore, the carrier phase cannot be reconstructed from these overlapping signals [94]. Hence, the multiplication by a single carrier permits only to down-convert amplitude-modulated signals that are composed of two identical sidebands.
(A down-conversion of 60 GHz impulses that have been up-converted by the impulse-converters described in section 2.3.2.1 is thus feasible, but requires a carrier phase synchronization of the LO. The analog implementation of this kind of synchronization is in general more complex as the quadrature direct-down conversion receiver discussed in the following.)
To avoid the issue illustrated in figure 2.11, a direct conversion receiver usually employs the architecture shown in figure 2.12. It performs down-conversion and I/Q demodulation simultaneously. Each of the two branches down-converts one of the two orthogonal signals that are present around the carrier and that contain each the same information in the upper and lower sideband. Because the two LO signals of the mixers are 90° out of phase, the two baseband signals I and Q are independent, and can be considered as real and imaginary part of a complex signal. Hence, a multitude of amplitude and/or phase modulations as well as the down-conversion of two orthogonal pulses trains are supported.

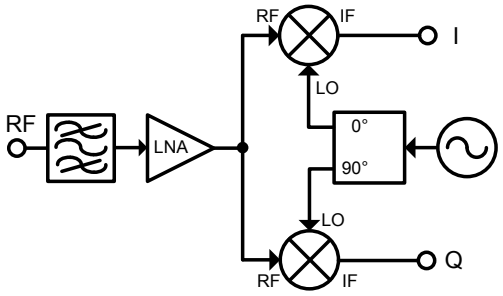


Figure 2.12: Principle of a direct conversion receiver creating the quadrature phases at the mixer's LO input by a 90° phase shifter

The bandpass filter shown in figure 2.12 removes out-of-band interferers and noise. It can also be implemented by the bandpass characteristic of antenna and LNA. Other than that, only low-pass filters are needed in the baseband circuit to perform channel filtering. The absence of high-Q filters is one major advantage of the direct conversion receiver with respect to the heterodyne approach (cf. section 2.4.5), thus permitting a completely integrated CMOS implementation of the front-end without impairment of the signal quality.
The direct conversion architecture is appealing for integrated RF front-ends that need to provide high data rate capabilities at low power consumption and cost. Furthermore, it is not limited to a specific modulation scheme. Nevertheless, its design provides some specific challenges that are discussed in articles of A.A. Abidi [121] and B. Razavi [122]. In the following, the major issues are highlighted and

their importance for an integrated UWB 60 GHz transceiver front-end is analyzed. These issues are:

- **DC offsets:** As illustrated in figure 2.11, the down-converted band extends to zero frequency. Thus, a parasitic DC offset is amplified in baseband together with the received, down-converted signal. If the offset is considerably higher in amplitude than the wanted signal (which still can be as low as some 100 µV after low noise amplification), it dominates and saturates the following amplifier stages.
  The principal source of a parasitic DC offset is self-mixing between a strong signal at one port of the down-mixer and coupling of the same signal to the other mixer port. The resulting baseband signal is of zero frequency. The strong signal can originate either from an interferer or the LO signal, or both.
  While for receivers of narrow-band signals the DC removal is quite challenging due to reasons given in [122], in the case of UWB 60 GHz communication, AC coupling can be employed: The high-pass filter that removes the DC offset before baseband amplification can have a cut-off frequency as high as 1 MHz, because this value is small with respect to the signal's bandwidth. Furthermore, the transmit signal can be designed taking into account this impairment of the receiver. Nevertheless, the effects that create the DC offset issue should be minimized by a strategy targeting to decouple the individual circuit blocks, filtering of strong in-band interferers and high LNA gain.

- **Flicker noise**: Since the flicker noise density is inverse proportional to frequency, it exceeds thermal noise at low frequencies. However, as the flicker noise corner frequencies of typical Metal Oxide Semiconductor (MOS) Field Effect Transistors (FETs) stay below 1 MHz [78], and AC coupling should be employed to remove the DC offset as mentioned before, in 60 GHz UWB receivers thermal noise is the by far dominating mechanism. Furthermore, the 60 GHz LNA screens the subsequent stages, thus flicker noise is not an issue in this kind of implementation.

- **Even order distortion**: In addition to odd-order intermodulation, which creates spurious signals in the RF band, even order distortion becomes an issue in Zero-IF receivers, because the spurious signals are created at low frequencies. Thus, due to RF to IF leakage in the down-mixer, products of even-order distortion in LNA and mixer can corrupt the baseband signal. To alleviate the problem, differential circuits can be employed for LNA and mixer, and their design should be optimized for linearity. Besides, due to the characteristics of the 60 GHz band (cf. 1.2.3), a quite low input power level is expected.

- **LO leakage**: The leakage of the LO signal, passing from the VCO via the mixer and the LNA to the antenna, creates in-band interference for other receivers. This kind of interference is less of an issue if using a heterodyne architecture, as the LO frequency lies outside the RF band. The use of balanced mixers and LNAs with high reverse isolation (e.g. using cascode stages) eases this issue.

- **I/Q mismatch**: The explanations of the direct conversion principal assumed perfect orthogonality between the I and Q signal. In reality, the LO outputs are not exactly 90° out of phase, and other non-idealities introduce further phase shift. If the quadrature demodulation is not done directly from 60 GHz, but at a lower intermediate frequency (cf. section 2.4.5), this phase error is smaller. A completely digital demodulation practically eliminates this error. However, both of these alternatives considerably increase transceiver complexity. A possible remedy, maintaining the direct conversion principle, is provided by the use of signal processing techniques, which are in any case necessary to do carrier phase synchronization.

The discussion above shows that the direct conversion architecture is particularly well suited for integrated UWB 60 GHz transceivers. The phenomena that disadvantage this architecture for narrow-band receivers are less severe in integrated 60 GHz RFICs. This, together with the fact that only few fundamental building blocks are required, makes it the most popular choice in 60 GHz receiver front-ends published so far.
The first SiGe receiver by S. Reynolds, B. Floyd *et al.* from IBM uses a direct conversion architecture with frequency tripler for the LO generation. The quadrature generation is accomplished by a branchline coupler [42, 43]. The very first 60 GHz CMOS receiver front-end, presented by B. Razavi, UCLA, US, also uses this topology [66–68].
The group of S. Voinigescu at University of Toronto employs direct conversion for both SiGe receivers (M.Q. Gordon et al. [50]) and CMOS receiver and transceiver front-ends (D. Alldred et al. in 2006 [69] and A. Tomkins et al. in 2008 [70, 71]) .
Many others also use the direct conversion architecture for their front ends: T. Mitomo *et al.* from Toshiba, Japan, [123, 124] include a 60 GHz PLL in their front end, B. Wicks *et al.* from University of Melbourne, present a complete receiver with PLL [108], while the same group presents earlier circuits in [106]; M. Tanomura *et al.* from NEC, Japan, [89], J. Lee *et al.* from National Taiwan University [75] and C.-C. Chen *et al.* from National Chi Nan University, Taiwan, [125] all base their 60 GHz CMOS front-ends on direct conversion.
Researchers from IMEC, Belgium, presented both a direct down-conversion phased array receiver front-end (K. Scheir *et al.* [85, 86]) and the first 60 GHz direct down-converter in 45 nm CMOS (J. Borremans *et al.* [126]).
The highest degree of integration so far reported for a direct conversion 60 GHz CMOS transceiver stems from the University of California, Berkeley (Marcu et al, 2009 [64, 65]). B. Afshar *et al.* from the same university implemented a much simpler low-power 60 GHz direct down-conversion receiver front-end [63].

2.4.5 *Heterodyne Receiver*

Figure 2.13 shows the principal architecture of a heterodyne receiver. Its RF part includes a Bandpass Filter (BPF) for image rejection and a LNA to raise the signal level and screen the noise of the subsequent stages. The mixing stage converts both the wanted signal and the unwanted signal remaining at the image frequency towards the IF, using a LO of frequency $f_1 = f_{RF} - f_{IF}$. At IF, a second filter selects the channel

and removes the unwanted mixing-product around $2f_{RF} - f_{IF}$. A subsequent high-gain amplifier, usually with variable gain, amplifies the IF signal to facilitate further treatment.
The I/Q demodulator added at the output of the heterodyne receiver front-end in figure 2.13 is one possible option to obtain the demodulated complex baseband signal. While its topology resembles a direct conversion receiver (cf. section 2.4.4), it does not exhibit its disadvantages because of the much stronger input signal due to the IF amplifier and the lower input frequency.

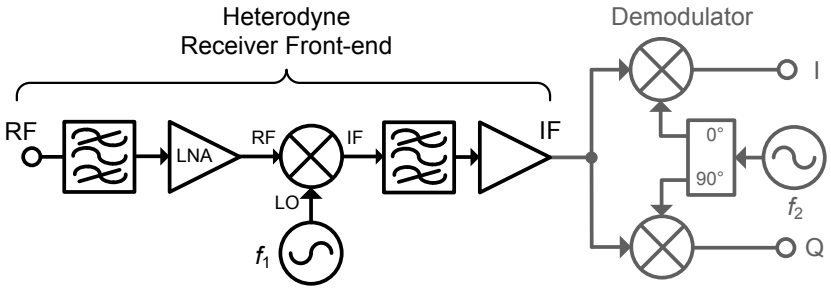


Figure 2.13: Block diagram of heterodyne receiver front-end with subsequent I/Q demodulator

The principal issue of the heterodyne receiver front-end, especially in integrated circuits where high quality filters are not available, is image and adjacent channel rejection [94]. Figure 2.14 illustrates the process of converting the RF signal to the IF: on the left, an exemplary signal at the receiver input is given. It contains the wanted signal (red, at $f_{LO} + f_{IF}$), an second signal close to the image frequency (blue, $f_{LO} - f_{IF}$), and an interferer present in an adjacent channel (green). The image signal has to be removed by an image reject Bandpass Filter (BPF) before conversion. Any remaining signal at the image frequency falls into the same band as the wanted signal when down-converted to IF. This is illustrated on the right side in figure 2.14, which shows the result of the down conversion by multiplication with a carrier at f_{LO}. The image signal, while strongly attenuated by the image reject filter, is still present in the signal band at IF.

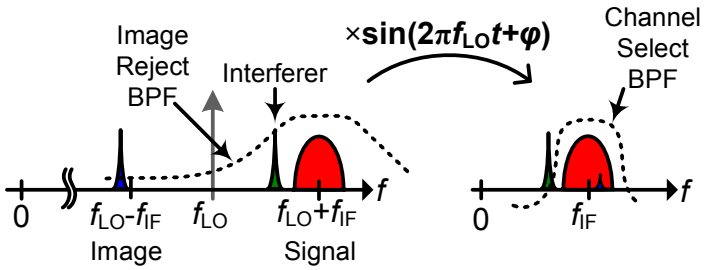


Figure 2.14: Illustrated spectrum in heterodyne down-conversion

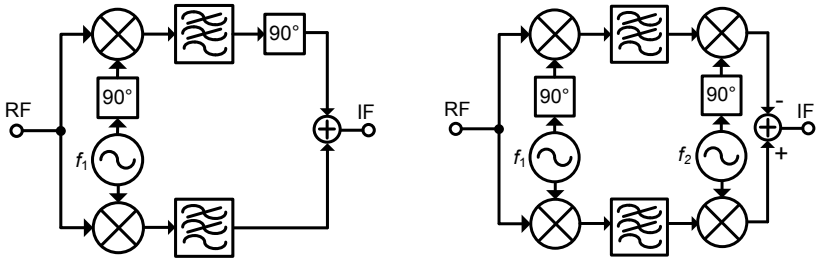
The higher the IF is chosen, the better the image can be rejected by a given filter, because the separation of wanted signal and image is greater. In 60 GHz transceivers, IFs frequencies from several GHz up to several ten GHz are usually employed, avoiding the use of off-chip image-reject filters.
However, a considerable drawback of using a high IF (in addition to the fact that IF circuits at higher frequencies are harder to design and

exhibit lower performance) is also illustrated in figure 2.14: as signals present in adjacent channels are not sufficiently attenuated by the image reject filter, a subsequent IF filter becomes necessary. The lower the IF, the steeper is the *absolute* slope of this filter (for a given quality factor). The optimum IF for channel filtering is thus zero, as in the case of the direct conversion receiver. A compromise can be the use of two different IF frequencies, leading to a dual-IF topology [94].
In addition to the image issue, which demands high quality filters and a wise choice of the IF frequency, a further drawback of the heterodyne receiver is its quite high complexity, leading to increased chip size and power consumption with respect to the direct conversion receiver. However, this disadvantage is not that severe because most of the complexity is not added at 60 GHz, but at the IF, where the additional circuitry consumes less power and is easier to implement. Especially the part requiring quadrature phases is not situated in the mm-wave front-end, but at lower frequencies.
The main advantages of the heterodyne receiver originate from the fact that signal processing can be done at the frequency best suited for a particular task (i.e. either at RF, IF or in baseband). Frequency planning is thus an essential aspect in heterodyne receiver design [94]. A well designed 60 GHz heterodyne front-end yields high sensitivity and selectivity, excellent I/Q balance (especially if demodulation is done in the digital domain) and good interference rejection, even if strong interferers are present.
A large number of 60 GHz receiver front-ends employ this well-established architecture. As in the case of two-step transmitters, both fixed-IF and sliding IF architectures (cf. section 2.3.3.1) are employed at 60 GHz. In SiGe technology, a 60 GHz heterodyne receiver front-end with sliding IF is proposed by S. Reynolds *et al.* of IBM, US, using a single LO around 17 GHz [44, 45]. A phased array receiver based on these circuits is published in [46]. Researchers from IHP, Germany, use a fixed IF of 5 GHz for their 60 GHz receiver front-end in SiGe:C BiCMOS technology [55, 56, 58].
The first heterodyne receiver front-ends in CMOS were presented in 2007. S. Emami, C.H. Doan *et al.* from the University of California, Berkeley, use a fixed IF of 1 GHz, while the LO is created by doubling the frequency of a 29 GHz signal [62]. B. Razavi from University of California, Los Angeles, implemented a 60 GHz receiver front-end with sliding IF around 20 GHz, derived from a 40 GHz LO [127, 128]. Later on, A. Parsa and B. Razavi proposed a new, heterodyne-based architecture that employs a single 30 GHz LO that is used for both conversion steps [113]. Complex signal processing permits the use of only one differential VCO without quadrature phases.
A highly integrated 60 GHz transceiver from Georgiatech, US, uses a heterodyne receiver with fixed IF that permits an UWB IF signal from 7 to 13 GHz [80, 81, 84]. Researchers from National Taiwan University propose different heterodyne receiver front-ends: K.-H. Chen *et al.* present a dual band receiver with integrated PLL and two different IFs [73]. C.-S. Wang *et al.* use a sliding IF around 20 GHz [74]. Their receiver employs sub-harmonic mixing, whose use in 60 GHz receiver front-ends is discussed in section 2.4.8. The same receiver is employed in their phased array receiver front-end [76].
Other implementations originate from Helsinki University of Technology, Finland, where M. Varonen, M. Kärkkäinen *et al.* employ an IF of

1.5 GHz [129], and integrate their receiver front-end together with an on-chip ADC [130]. F. Vecchi, S. Bozzola *et al.* from University of Pavia and ST Microelectronics, Italy, realized a front-end with a sliding IF around 20 GHz. Coupled resonators in their LNA's matching networks realize a steep-slope image rejection filter [131, 132].

2.4.6 *Image Rejection Receivers*

Section 2.4.5 illustrates the issue of image rejection in heterodyne receivers. It shows that the use of an image rejection filter requires a tradeoff between good image rejection and the use of a low IF frequency, which facilitates channel filtering and IF processing in general. The concept used in image rejection receivers provides an alternative solution to the image problem [78, 94, 133]. It uses two receiver arms for down-conversion that are combined at the IF. The signal's phase in either of the two arms is shifted in such a way as to delete the image signal at the IF output by adding it out of phase. The desired signal is doubled by adding it in phase.



(a) Hartley - topology [134] (b) Weaver - topology [135]

Figure 2.15: Image rejection receiver principles

Figure 2.15 shows the two principal topologies of image rejection receivers, proposed by R. Hartley in 1928 [134] and D.K. Weaver in 1953 [135]. While Hartley uses a single conversion step and an additional 90° phase shift in the signal path, Weaver introduces the total phase shift by two conversion steps in one of the branches, and subtracts the signal of both branches.
A 60 GHz image rejection receiver front-end is proposed by J. Kim *et al.* from Seoul National University, South Korea, in a pHEMT technology [136]. It is based on the Hartley architecture and uses varactor tuning to adjust the introduced phase shift and thus improve image rejection performance.
The same principles can be employed to implement a Single Sideband (SSB) transmitter, where rather than rejecting the received image, one of the sidebands that appear at the output of a direct or two-step conversion transmitter is eliminated. Thus, only one sideband is transmitted.
The main advantage of an image rejection receiver front-end is that it provides an elegant solution to the image issue. However, its performance comes at the expense of RF circuit complexity (and thus cost and power consumption) and depends on the tolerance that can be achieved for the 90° phase shift. Even though quadrature phases are necessary for the LO, a quadrature de-modulation is not obtained at the IF output. Thus, like in the case of a classical heterodyne-receiver,

either a quadrature demodulator or any other kind of demodulation at the IF needs to be added, further increasing circuit complexity. The direct conversion receiver (introduced in section 2.4.4), on the other hand, already provides quadrature demodulation while exhibiting a complexity below the one of the Hartley architecture (cf. section 2.4.4).

2.4.7 *Six-Port Receiver*

The six-port receiver is based on a technology that was developed in the 1970s to perform network analysis [137, 138]. In that context, a six-port circuit (comprising two inputs and four outputs as described below) is employed to obtain the complex reflection coefficient of a Device Under Test (DUT). It compares the wave reflected at one port of the DUT, which is fed to one of the six-port's inputs, to the wave incident on the same or another port of the DUT, which is applied to the other input of the six-port.
The same technique proves useful to demodulate a quadrature modulated signal [139], if the two inputs of the six-port are connected to the received signal and a reference signal at the carrier frequency, respectively. The six-port circuit provides four outputs, whose signal amplitudes allow to obtain the phase and amplitude difference between the two inputs to compare. Hence, it is well suited for both phase and amplitude modulations.
Figure 2.16 shows the principal architecture of a receiver employing a six port circuit [109]. The first input is provided by a local reference oscillator. The second input is the received, amplified signal. As both signals are compared, it is sufficient if the LO power is of the same order of magnitude as the RF power. The diode symbols indicate power detectors that are connected at the four outputs of the six port circuit: they are used to determine the amplitude of the signals at these outputs. Their actual implementation corresponds to one non-coherent receiver, as detailed in section 2.4.1, per port. Note that despite the fact that no coherent detection is necessary at these four output ports, the phase of the receiver signal can be determined from the detected amplitudes [138].
Figure 2.17 shows a typical implementation of a six-port circuit using three quadrature hybrids and a power divider [109, 139, 140]. Assuming the complex harmonic phasors a_{LO} and a_{RF} of frequency f_0 at the inputs, the resulting phasors at the output are indicated for the ideal case of 90°phase shift of the hybrids and negligible parasitic coupling. The amplitudes of the output signals, annotated in figure 2.17, vary both with phase and amplitude difference of the input signals.

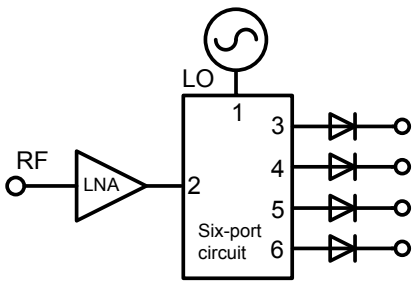


Figure 2.16: Block diagram of six-port receiver front-end

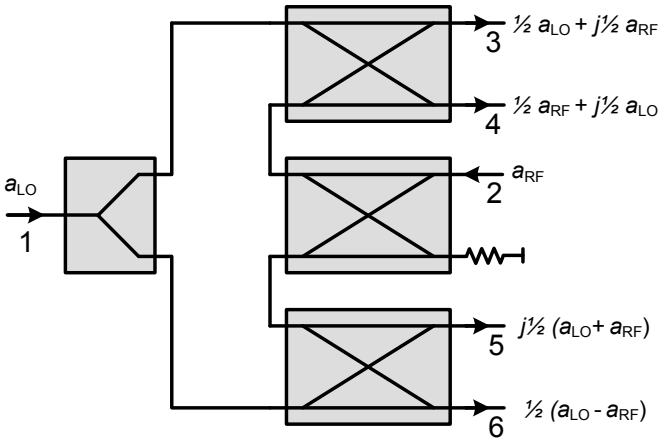
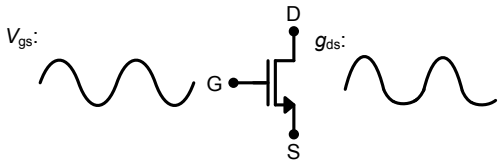


Figure 2.17: Typical implementation of a six-port demodulator

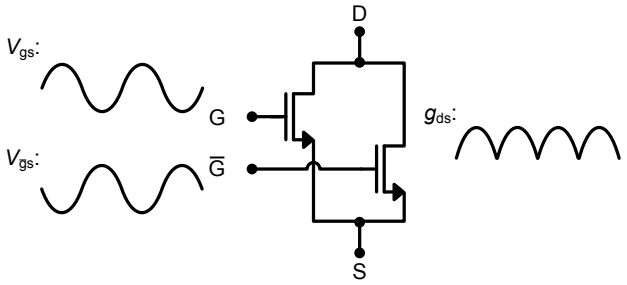
A simple example for the signal at port 3 illustrates how the phase difference between the two input ports influences the output amplitude: in the case of $|a_{RF}| = |a_{LO}|$ at the inputs, the amplitude at port 3 equals $|a_{RF}|$, if the phase of the RF signal is shifted by -90° with respect to the LO signal. If the phase shift is +90°, the output amplitude at port 3 is 0. In the general case where amplitude and phase of an RF input signal are unknown, both can be reconstructed by the baseband circuit of the receiver (if taking into account all four output amplitudes, and applying appropriate calibration). Further details on the required baseband processing are given in [139].
The six-port receiver has several advantages with respect to conversion architectures. It provides coherent detection of a quadrature modulated signal without the use of mixers. This also implies that the necessary LO power can be as low as that of the received RF signal. The front-end's power consumption can thus be very low. As interpretation of the received signal is usually done by the digital baseband, a high degree of reconfigurability can be achieved. Furthermore, as the used components can all be very broadband, the receiver can cover a vast frequency range. Another advantage is the high spectral efficiency that the detectable modulation schemes can provide.
A drawback of this architecture consists in the high device count for the baseband circuit at its outputs: Four accurate power detectors and thus four times the subsequent baseband circuitry (including ADCs) are necessary. Another disadvantage is that this principle is designed for continuous carrier modulations, because it calculates phase and amplitude of a received signal, rather then down-converting an arbitrary waveform. It is thus not appropriate for impulse modulation.
The six-port receiver architecture is used in a 60 GHz CMOS transceiver presented as early as 2007 by C.-H. Wang *et al.* of National Taiwan University, Taiwan [109]. S.O. Tatu, E. Maoldovan *et al.* from INRS-EMT, Montreal, Canada also do research on V-band receivers based on six-port circuits [140, 141]. They also propose the use of this architecture together with Butler matrices to constitute a integrated phased array front-end [142] (a Butler matrix [143] can be constructed using the same basic building blocks as the six-port circuit in figure 2.17).

2.4.8 *Sub-harmonic Mixing in 60 GHz Transceivers*

In the presentation of receiver and transmitter architectures given so far, fundamental frequency mixing was implicitly assumed. Figure 2.18a illustrates the simple switching principle that is employed in basically all kinds of FET based mixers to implement this kind of mixing. If employing fundamental mixing, a conversion from f_1 to f_2 requires a local oscillator of frequency $f_1 \pm f_2$. Especially in 60 GHz direct conversion transceivers, this implies a quite high LO frequency, resulting in decreased phase noise performance and challenging frequency synthesizer design. Furthermore, direct conversion architectures using fundamental frequency mixing suffer from LO self mixing (cf. section 2.4.4).



(a) Principle of harmonic mixing



(b) Principle of sub-harmonic mixing

Figure 2.18: Harmonic versus sub-harmonic mixing principle

To avoid the afore-mentioned issues, sub-harmonic mixing can be employed. The principle is illustrated in figure 2.18b: the switching transistor in a harmonic mixer is replaced by two transistors in parallel. They are driven by two LO signals that are 180° out of phase. Due to the fact that the driving signal is not perfectly rectangular, the transistor's large signal output conductance g_{ds} varies with twice the LO frequency (and not with the LO frequency as in the harmonic case). A conversion from f_1 to f_2 thus requires an LO frequency of only $(f_1 \pm f_2)/2$. For unbalanced switching, an LO signal with 0° and 180° is needed. A balanced mixer requires four LO phases of 0°, 90°, 180°and 270°. This requirement is one drawback of sub-harmonic architectures, another one being the decreased conversion efficiency with respect to front-ends using fundamental frequency mixing.
Sub-harmonic mixing is successfully employed in the 60 GHz CMOS heterodyne receiver front-end presented by C.-S. Wang *et al.* from National Taiwan University [74]. This front-end is also part of the phased array receiver front-end they published in 2009 [76].
M.A.T. Sanduleanu and J.R. Long from Philips Research and Delft University of Technology, Netherlands, also use the sub-harmonic mixing approach in their 60 GHz CMOS direct conversion receiver [144]. They employ a 30 GHz four-phase VCO to allow balanced operation.

2.5 The adopted transceiver architecture

The preceding sections discussed in detail the different architectures viable for integrated 60 GHz transceiver front-ends. They provide the necessary background to select the type of front-end to use in the low-power, low-cost radio interface introduced in chapter 1. From the presented options, direct conversion is chosen both for the transmitter and the receiver front-end. Sections 2.5.1 and 2.5.2 briefly justify this choice for each side, and discuss details on the targeted implementation.

2.5.1 *Adopted Direct Conversion Transmitter Front-end*

The main reason for the adoption of the direct conversion architecture at the transmitter side (cf. section 2.3.2) is its low complexity while providing at the same time high versatility. This allows the use of various modulation schemes (among them up-conversion of baseband impulses). A specific impulse radio transmitter (as described in section 2.3.1) is not chosen due to the fact that it does not permit continuous carrier modulation. A two-step transmitter (cf. section 2.3.3), though permitting the same modulations as the adopted direct conversion type is not utilized here due to its higher complexity.

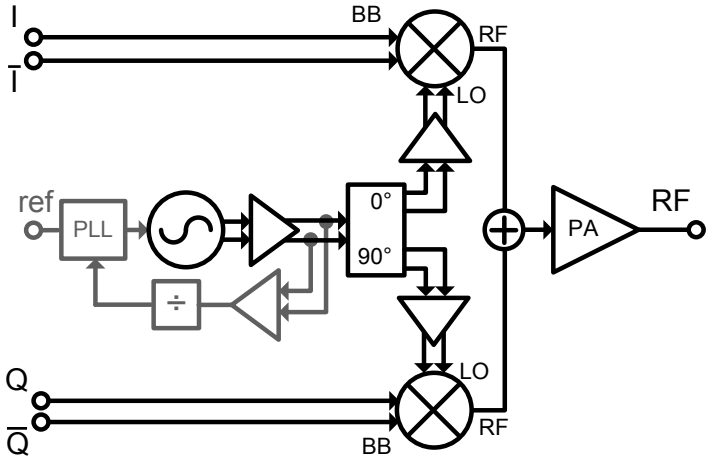


Figure 2.19: Block diagram of adopted direct conversion transmitter

Figure 2.19 gives the block diagram of the proposed transmitter front-end. At the left, the quadrature inputs, $I/\overline{I}$ for the in-phase component and $Q/\overline{Q}$ for the quadrature component, are shown. These signals are differential, in order to provide an interface to the baseband circuit that does not suffer from common mode interference or noise. They are up-converted by a balanced mixer, which allows a high LO-to-RF isolation. This isolation is important, because the LO signal falls into the transmitted RF band in direct conversion transmitters, and thus cannot be filtered after the mixer. The use of such a balanced mixer requires a differential LO signal.
The mixer output provides a single-ended signal to allow the use of a single ended PA [145] and antenna. The PA raises the signal level to about 10 mW, while its matching networks provide filtering of the transmit signal.
The frequency synthesizer employs a differential, fundamental frequency VCO that oscillates in the 60 GHz band. Neither frequency

doubling nor sub-harmonic mixing (cf. section 2.4.8), which would allow lower VCO frequencies, are employed: despite the advantages of these solutions, they decrease the power efficiency of the front-end and thus increase power consumption. This cannot be tolerated for the present applications. The PLL and frequency divider, which synchronize the VCO to a very stable external reference signal of fixed frequency, are not detailed here as they are not subject of this thesis.
At the output of the VCO, a phase shifting network is required to generate orthogonal LO signals: the VCO provides a differential signal, which has to be passed to the two mixers 90° out of phase, while maintaining the same amplitude. If this phase shift is not exactly 90°, the I and Q components lose orthogonality.
The VCO output signal has to be distributed to both mixers and the frequency divider. Because these frequency conversion blocks require high signal amplitudes, buffer amplifiers are inevitable and thus added to the transmitter front-end. In order to decrease their power consumption, which is proportional to their linearity, mixers and dividers have to be optimized for low LO power consumption. Note that other, smaller buffer amplifiers might also be necessary at the BB input and RF output of the mixers.
The design of the transmitter front-end components is governed by the linearity requirement: as can be seen from the link budget in section 1.3, the transmitter output power, which is related to its linearity, directly influences the realizable link distance.
The 1 dB compression point P_{1dB} is well suited to quantify linearity [78, 94, 133]. It represents the power value (either input-referred as IP_{1dB} or output-referred as OP_{1dB}) for which a component's large signal gain for a harmonic signal of given frequency lies 1 dB below the linear gain.
The compression point of the transmitter depends on the linearity of its building blocks: if the gain G_i and the 1 dB compression point $P_{1dB,i}$ of each individual stage are known, the cascade of n stages from input 1 to output n has an approximated[1] 1 dB compression point given by

$$\frac{1}{P_{1dB,tot}} \approx \frac{1}{P_{1dB,1} G_2 \cdot \ldots \cdot G_n} + \frac{1}{P_{1dB,2} G_3 \cdot \ldots \cdot G_n} + \ldots \\ \ldots + \frac{1}{P_{1dB,n-1} G_n} + \frac{1}{P_{1dB,n}}. \tag{2.4}$$

This equation shows that the linearity of the last stage (i.e. the PA), given by $P_{1dB,n}$, is decisive for the linearity of the transceiver, if this stage adds sufficient gain G_n. However, (2.4) also shows that if the compression point of the next to last stage (i.e. the mixer in figure 2.19), given by $P_{1dB,n-1}$, is lower than $P_{1dB,n}$ by the gain G_n of the last stage, both stages contribute equally to the overall linearity. This shows the importance of taking into account (2.4) during the design of *all* transmitter building blocks: a power amplifier with high output power cannot exploit its potential if the mixer limits the RF output power.

[1] Note that all values are linear, i.e. not in dB(m). Equation (2.4) is a worst-case estimate [94], derived making use of the theoretical relationship between P_{1dB} and the Third Order Intermodulation Point (IP_3)

2.5.2 *Adopted Direct Conversion Receiver Front-end*

Like at the transmitter side, a direct conversion architecture is also employed by the receiver. It is considered more adequate than other topologies due to several reasons: First, the receiver should be able to demodulate *all* the signal forms which the transmitter can generate. This eliminates the use of non-coherent receivers (cf. section 2.4.1) , super-regenerative receivers (cf. section 2.4.2) or coherent impulse radio receivers (cf. section 2.4.3). While these kind of architectures have low power capabilities, they only permit the reception of low complexity modulations with poor spectral efficiency. The six-port receiver (cf. section 2.4.7) cannot be adopted, because it is not well suited for the down-conversion of 60 GHz impulses. However, this also is a major requirement stipulated in section 2.2.
From the remaining receiver architectures (i.e. heterodyne receivers, cf. section 2.4.5, image rejection receivers, cf. section 2.4.6, and direct conversion receivers, cf. section 2.4.4), the latter one promises lowest complexity and lends itself to a fully integrated solution. It is thus adopted for the receiver side in the configuration shown in figure 2.20. The drawbacks of this architecture are expected to be tolerable for UWB communication in the 60 GHz band, if the receiver is designed in awareness of the potential issues.

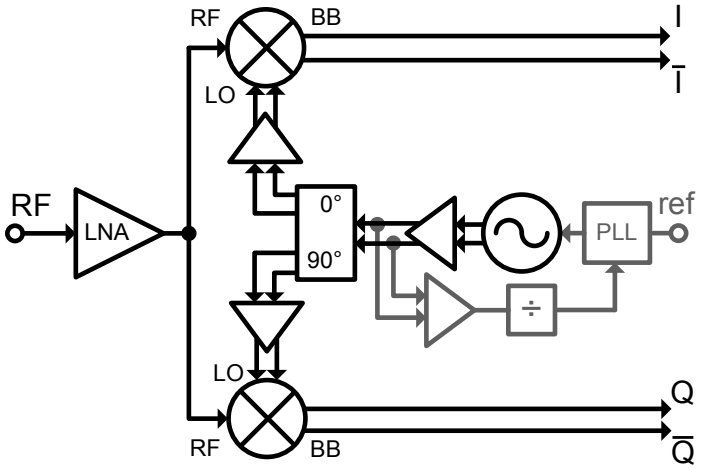


Figure 2.20: Block diagram of adopted direct conversion receiver

As illustrated in figure 2.20, the RF input of the receiver is single-ended to allow the use of a single-ended antenna and reduce LNA complexity. The LNA exhibits a band-pass characteristic, thus acting also as input filter.
The down-conversion mixers are of single-balanced type: this allows a good RF-to-BB isolation (isolation is, however, less critical for 60 GHz direct conversion receivers, because the LO and RF are far from the BB and can thus be filtered easily). Furthermore, the use of a differential LO enables the mixer to easily generate differential baseband outputs from a single-ended RF input. Thus, this interface to the baseband, presented by $I/\overline{I}$ for the in-phase component and $Q/\overline{Q}$ for the quadrature part, is much less susceptible to common mode interference.
The synthesizer and LO distribution network is identical to the one of the transmitter front-end (cf. section 2.5.1 for details on this circuit part). Thus, if receiver and transmitter front-end are integrated on the same

chip, the synthesizer needs to be implemented only once, provided that additional buffers are added.
The most important parameter of the receiver front-end is its Noise Figure (NF). It directly influences the link distance as can be seen from the calculations in section 1.3. To understand how the individual circuit blocks contribute to the receiver's NF, the NF of a system of cascaded stages with gain G_i and noise figure NF_i is considered. It is given by the Friis equation [146]

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdot \ldots \cdot + \frac{NF_n - 1}{G_1 G_2 \ldots G_{n-1}}, \quad (2.5)$$

where the indices reach from 1 to denote the input stage to n to denote the output stage. Equation (2.5) shows that the NF of stage one (i.e. the LNA) is directly added to the receiver NF, while its gain G_1 is screening the noise of all subsequent stages. A well designed LNA, providing low NF and high gain, is thus essential for the performance of the receiver front-end.
As in the case of the transmitter, linearity also has to be considered during receiver design. As illustrated by the relationship given in (2.4), high linearity in the LNA is not sufficient to achieve a good receiver linearity. The subsequent stages (especially the mixer) need to be of corresponding linearity, thus being more likely the blocks limiting performance in this regard. Note, however, that linearity requirements are less an issue in the 60 GHz band compared to lower frequencies: while out-of band interferers need to be removed by filtering, the remaining in-band interferers are expected to be of low power due to the properties of the 60 GHz channel discussed in section 1.2.3.

2.6 CONCLUSION

This chapter provided a thorough discussion of suitable architectures for high data-rate transceiver front-ends. It was accompanied by a review of the state of the art of 60 GHz RFIC implementations of this kind of architectures. Based on these considerations, the direct conversion approach was chosen both for the transmitter and receiver front-end. It presents the most appropriate architecture[1] in the context of the low-cost, low-power, high data rate radio interface presented in chapter 1.
The remainder of part I of this thesis is concerned with the implementation of the essential parts of the transceiver front-end presented in section 2.5. As the performance of the front-end heavily depends on the mutual adjustment of its building blocks, their interaction has to be kept in mind during their design.
The following chapters are organized according to the transceiver's circuit hierarchy: chapter 3 introduces the employed 65 nm CMOS technology and presents the employed active and passive devices. It also discusses design techniques common to all building blocks. Chapter 4 illustrates the design and implementation of the transceiver's key building blocks realized in the framework of this thesis. Chapter 5 illustrates the progress towards the on-chip assembly of these building blocks by presenting the implementation of one branch of the receiver front-end.

[1] The suitability of this choice is confirmed in particular by the recently published 60 GHz transceiver from University of Berkeley [64, 65].

3 MILLIMETER-WAVE CIRCUIT DESIGN IN 65 NM CMOS

3.1 INTRODUCTION

As detailed in section 1.4, the mm-wave front-end, whose architecture was chosen in chapter 2, shall be integrated together with digital circuitry on the same chip to minimize size and reduce packaging effort and cost. This mandates the use of a CMOS-based technology, which is the only means of efficiently implementing very complex digital circuits. Thus, either CMOS or BiCMOS are potential technologies for the realization of the 60 GHz radio interface. Other reasons to favor (Bi)CMOS over competitors like the compound semiconductor technologies GaAs or Indium Phosphide (InP) include the potential for low power consumption, small circuit size, low cost in mass production and the performance that can be achieved with recent (Bi)CMOS technologies.

When it comes to the choice between CMOS and BiCMOS technology, it has to be noted that both recent CMOS and SiGe BiCMOS technologies exhibit the necessary performance for RFIC design at 60 GHz [42, 61]. In the latter case this becomes possible due to the use of powerful bipolar transistors that exhibit much higher unity gain frequencies as the field-effect transistors of the CMOS technology they are implemented in.

However, there are different arguments that support the use of standard CMOS instead of BiCMOS technology. First of all, nanoscale CMOS RFICs usually dissipate less power with respect to RFICs of same performance employing bipolar transistors. Secondly, the performance of the CMOS transistors in a BiCMOS process is clearly inferior to the performance of the available bipolar transistors. Thus, while for example a 130 nm SiGe BiCMOS process exhibits mm-wave performance comparable to a 65 nm CMOS technology, the digital circuitry on the same chip, which is in any of these two cases a synthesized CMOS circuit, will suffer from lower performance, higher power consumption and larger circuit size. These reasons, and a potential cost advantage if the number of fabricated circuits is very large as in the case of consumer applications, makes CMOS technology the first choice for the 60 GHz radio interface.

To allow the design of high performance, low power circuits at 60 GHz, a gate length below 130 nm is desirable. The adopted choice, not only for the front-end circuits designed in this thesis, but also for the other components of the radio interface [8], is the 65 nm CMOS technology of STMicroelectronics[1]. As its transistor's cutoff frequencies are roughly three times above the desired operating frequency (see section 3.2.2), comfortable RFIC design becomes possible. Technologies featuring even smaller gate lengths, which became available only recently, are not necessary. They would even add further design challenges due to a scaled metal back-end and more severe metal density rules.

[1] http://www.st.com

This chapter first discusses the chosen 65 nm technology of STMicroelectronics in section 3.2. The metal back-end, as well as Design Kit (DK) devices that are used for circuit design in this thesis are briefly introduced. Next, full custom devices created to supplement the resources of the DK are discussed in detail (varactors in section 3.3, Transmission Lines (TLs), spiral inductors and transformers in section 3.4). The accurate measurement of these full-custom devices is studied in section 3.5. Finally, some design (section 3.6) and layout (section 3.7) techniques that are common to all components and essential to the successful creation of mm-wave CMOS circuits are outlined.

3.2 TECHNOLOGY DESCRIPTION

To respect the confidentiality imposed by the non-disclosure agreement with STMicroelectronics, the following informations remain quite general. More detailed informations as well as the 65 nm DK can be obtained via CMP[1] or directly from STMicroelectronics.
The name of the basic digital 65 nm CMOS platform [147] does not exactly correspond to the physical gatelength, but is rather chosen due to historical reasons. While the minimum drawn gatelenth in this technology is 60 nm, the actual phyisical gate lengths are even smaller and depend on the transistor type. Two principal MOS transistors are provided as both n-channel and p-channel type:

- a General Purpose (GP) transistor for 1.0 V $\pm$ 10% applications with thin gate oxide
- a Low Power (LP) transistor for 1.2 V $\pm$ 10% applications with thicker gate oxide

In addition to that, 1.8 V and 2.5 V transistors are provided for the digital output cells. They exhibit correspondingly thicker gate oxides. The process uses Shallow Trench Isolation (STI) [148] to allow a higher density of integration and in based on a p-type low resistivity substrate to prevent latch-up of the parasitic substrate transistors. Further front-end features include deep n-wells and dual or triple threshold voltage (V_{th}) transistors.
A SOI version of the 65 nm CMOS process has become available recently, allowing high resistivity substrates and superior RF performance. However, this process flavor was not finalized when beginning the designs for this thesis, mandating a design in bulk CMOS technology.
The metal back-end can provide up to ten metal layers for interconnect, using dual-damascene copper for all but the last layer. The standard process used during this thesis, named 7M-4X-0Y-2Z, contains seven copper layers plus one aluminum pad layer as illustrated in section 3.2.1. A low k inter-metal dielectric ($\epsilon_r = 2.9$) is employed.
Optional analog/RF capabilities do exist that provide additional components and somewhat relaxed inductor design rules. However, of these additional RF components, the circuits presented in this thesis only use the Metal On Metal (MOM) capacitors (cf. section 3.2.3).

[1] http://cmp.imag.fr

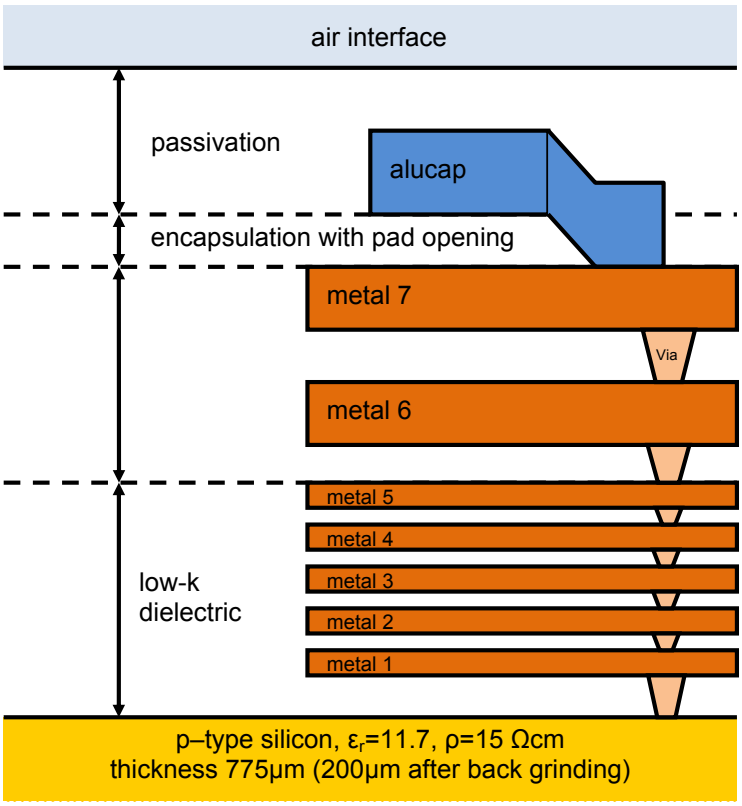


Figure 3.1: Simplified metal-backend of the 65 nm CMOS technology

3.2.1 *Metal Back-End*

A simplified illustration of the processes' metal back-end is given in figure 3.1. As mentioned before, the topmost layer (alucap, AP) consists of aluminum while metal 1 to metal 7 layers and the vias consist of dual damascene copper. To get a rough idea of the very small vertical dimensions encountered, note that the figure is approximately to scale, the metal layers AP, M6 and M7 are about 1 µm thick, and the whole back-end does not even attain 10 µm thickness. Its dimensions make it challenging to design high quality full-custom passive devices (cf. section 3.4). The silicon substrate has a resistivity of $\rho = 15\Omega$cm, is 775 µm thick and may be back-grinded to 200 µm.

3.2.2 *MOS Transistors*

As mentioned above, all transistors are available both in a n and p channel version: figure 3.2 gives the symbol and voltage and current definitions used withing this thesis when describing these MOSFETs. The terminals S, D, G and B designate source, drain and gate and bulk respectively. As the high-frequency performance (apart from flicker noise) is considerably lower for p-channel MOSFETs, they are not considered in the following and are not used in the 60 GHz designs presented in this thesis.
For both the LP and GP transistors, which are introduced above, three versions exist: A SVT type with standard threshold voltage, a LVT type with low threshold voltage, and a HVT type with high threshold voltage. The different threshold voltages V_{th} are achieved by adjusting

(a) Symbol of the n-channel MOSFET (b) Symbol of the p-channel MOSFET

Figure 3.2: Definition of the symbols used for n and p channel MOSFETs. A missing bulk contact when using these symbols in a circuit indicates a shorting of this contact to the ground.

channel doping. The LVT type transistor exhibits highest switching speed, but the leakage current in off-state ($V_{GS} = 0\,V$) is also quite high. The inverse is true for the HVT transistor, where both speed and off-state leakage are lower.
This reasoning works well to choose one of these transistors for (usually digital) switching applications, where leakage increases the static power consumption, and the transistors gate voltages switch from $0\,V$ to the supply voltage V_{DD}.
However, in RFICs the transistors are usually biased at a constant drain current density (cf. section 3.6.1), which, together with the drain-source voltage V_{DS}, determines the transistor's power consumption. Which V_{GS} has to be applied to achieve the desired bias current density has no influence on the dissipated DC power. Furthermore, high switching speed is not equivalent to good mm-wave behavior. Thus, figures of merit that characterize the transistor's RF behavior are required.

3.2.2.1 *MOSFET high frequency performance*

To characterize a transistor's RF performance at a given bias point, one of the following two small-signal figures of merit are usually employed [148]:

- The **cutoff-frequency** (also known as *transient frequency* or *unity-current-gain frequency*) is denoted by f_T. It is defined as the frequency at which the common source small signal current gain for a short-circuited load drops to unity.
- The **maximum oscillation frequency** is denoted by f_{max}. It is the frequency for which the transistor's power gain becomes unity. In contrast to f_T it also takes into account the effect of the gate resistance (cf. section 3.2.2.4).

The computation of these two frequencies based on the MOSFET's equivalent circuit, which illustrates the influence of the device's parasitic elements, is given in section 3.2.2.4. In the remainder of the present sub-section, measured f_T and f_{max} values are used as qualitative indicators [148] to decide which bias point and transistor type is the best choice to achieve optimum mm-wave performance.
An evaluation of f_T and f_{max} performance of different types of 65 nm transistors are found for instance in [149–151]. Figure 3.3, adopted from [150], shows the measured f_T for both LP and GP transistors with stan-

dard and high threshold voltage. (The f_T curves for the LVT transistor, which are not given here, lie even slightly above the SVT types [151]). At the left, f_T is plotted versus gate-source voltage. At the right, the same curves are aligned according to the associated drain current densities. This shows that the maxima of f_T are achieved for an identical, characteristic current density for all types of transistors. This fact is exploited for constant current biasing [152] as detailed in section 3.6.1, and also implies that the different maximum f_T values are achieved by transistors consuming the same DC power. This proves that the LVT GP NMOS transistor is the one that yields best performance with respect to both high frequency gain and low power consumption. It is thus preferably used in this thesis.
Figure 3.4, which is also adopted from [150], plots f_T and f_{max} over the drain-source voltage for the current density that yields maximum f_T. It shows that the unity gain frequencies increase monotonically with V_{DS}. For a supply voltage of 1 V, which is the one specified for the LVT GP NMOS transistor, this device is expected to yield an f_T of

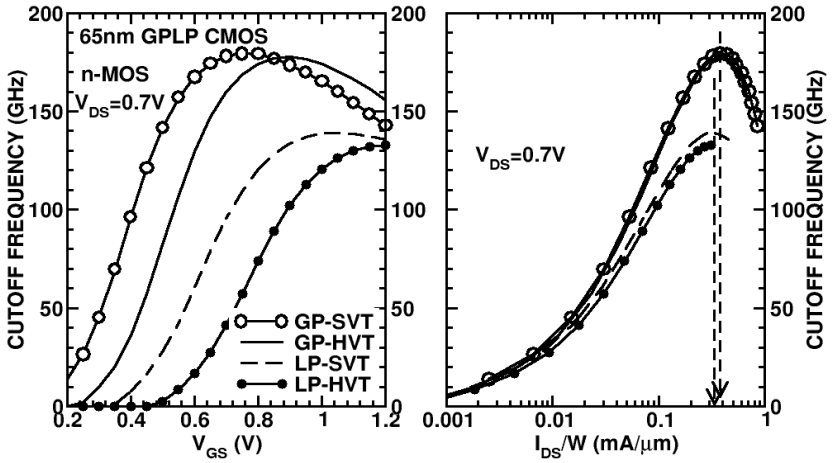


Figure 3.3: f_T of 65 nm NMOS transistors with 80 fingers of 1 µm width versus gate-source voltage and drain current density, adopted from [150] with permission, Copyright IEEE 2007.

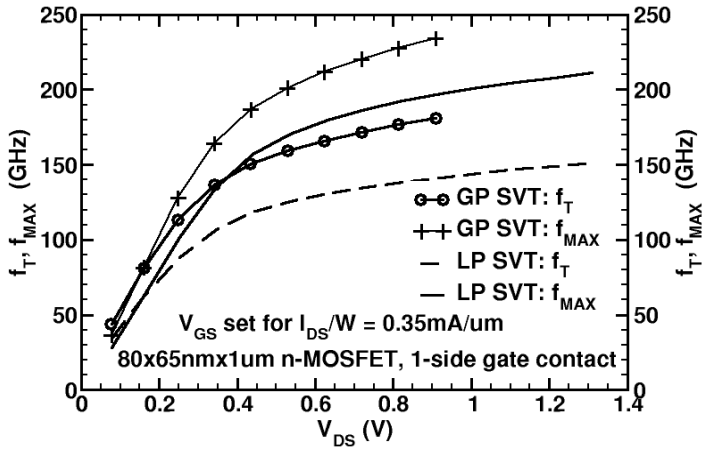


Figure 3.4: f_T and f_{max} of 65 nm NMOS transistors with 80 fingers of 1 µm width versus drain-source voltage, adopted from [150] with permission, Copyright IEEE 2007.

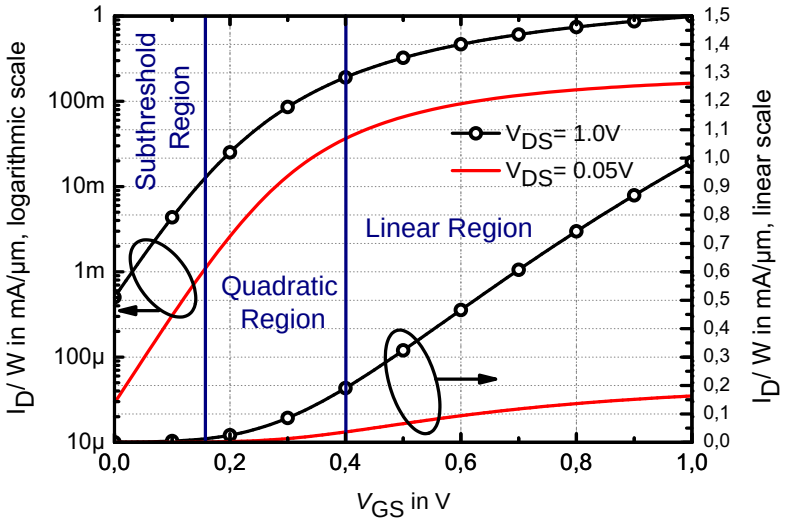


Figure 3.5: Normalized DC transfer characteristic of a 65 nm LVT GP n-channel MOSFET, based on the simulation using DK models

about 190 GHz and an f_{max} of about 245 GHz. Note that these values are layout-dependent and can differ with respect to the number of gate contacts and the transistor's geometry. Subsection 3.2.2.4 gives analytical expressions for the calculation of these characteristic frequencies that show how they are influenced by the different device parameters. To allow a V_{DS} above 0.5 V per transistor to maximize performance when stacking two of them (as e.g. in a cascode amplifier), the deep n-well feature of the 65 nm CMOS process can be used. It isolates the channel from the substrate as illustrated in section 3.2.2.5.

3.2.2.2 *MOSFET noise performance*

To accurately characterize the noise performance of the 65 nm MOSFETs at 60 GHz, the models provided by the DK are not sufficient. This is because all transistor models given in the process DK are based on measurements up to maximally 50 GHz. To nevertheless get an idea about the noise performance to expect from the MOSFETs, in [149] the measured values of the minimum noise figure NF_{min} given for a LP n-channel 65 nm device have been extrapolated, yielding about 2 dB at 60 GHz. According to [153], GP devices shall yield even better results. Further information on noise characteristics of the 65 nm GP and LP transistors at slightly higher frequencies can be found in [153].

3.2.2.3 *The short-channel MOSFET's DC characteristics*

Figure 3.5 shows the simulated DC transfer characteristic of a LVT GP n-channel MOSFET with $L = 65$nm gate length. The curves are plotted both logarithmically and linearly [148], and two different drain-source voltages are indicated. The figure shows that the square-law behavior, which results from the fact that I_D saturates due to channel pinch-off, is present only for small gate-source voltages here. If V_{GS} increases, the transfer characteristic becomes linear.
This effect is often attributed to velocity saturation [148, 154]: it occurs in short-channel devices, when the charge velocity in the channel attains its saturation value due to the strong *lateral* drain-source field before the

channel is pinched off. As saturation velocity does not depend on V_{GS}, this effect reduces the quadratic transfer characteristic to a linear one. However, there is a second effect present in short-channel devices that, according to the discussion by T. O. Dickson *et al.* in [152], creates the linear transfer characteristic well before the onset of velocity saturation. This effect is the mobility degradation due to the *vertical* field: As this field is an order of magnitude stronger than the lateral field, its impact of the MOSFET's characteristic is dominant in nanoscale CMOS technologies [155].

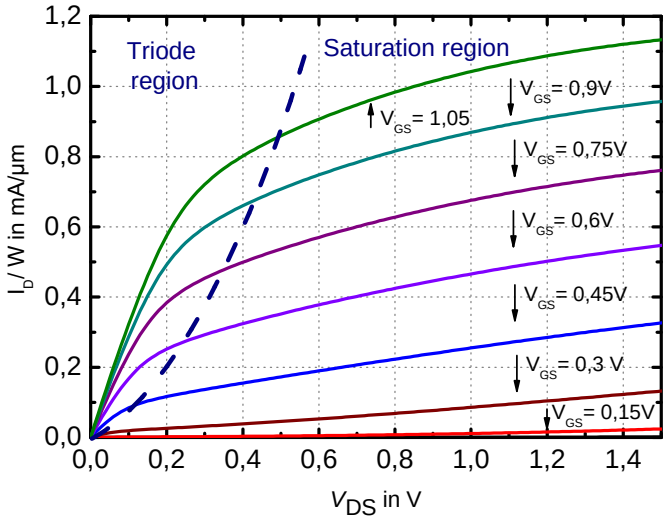


Figure 3.6: Output characteristic of a 65 nm LVT GP n-channel MOSFET, based on the simulation using DK models.

Figure 3.6 plots the DC output characteristic of a 65 nm n-channel LVT GP transistor. The afore-mentioned linear transfer characteristic of the MOSFET is embodied in this graph due to fact that I_D achieves lower values as it would in the case of a quadratic characteristic. Thus, the triode region is reduced to drain-source voltages well below the long-channel limit of $V_{GS} - V_{th}$.
Another effect, which has considerable impact on the design using short channel devices, is also clearly observable in figure 3.6: in contrast to the ideal MOSFET, the drain current depends heavily on the transistor's drain-source voltage even in saturation. The MOSFETs output port can thus not be considered as an ideal controlled current source. In fact, it must be modeled with a resistor $r_0 \approx \frac{1}{\lambda I_D}$ in parallel to the ideal output as shown in the equivalent circuit discussed in section 3.2.2.4. The intrinsic voltage gain of a transistor is severely limited by this quite small output resistance. Physically, the influence of V_{DS} on I_D originates from channel length modulation [148, 154]: the effective channel length L_{eff} is not constant and equivalent to the geometrical channel length L, but varies with V_{DS}. This is characterized by the channel length modulation coefficient [154]

$$\lambda = \frac{\Delta L}{L} \frac{1}{V_{DS}}. \tag{3.1}$$

Because the absolute channel length variation ΔL is independent of the geometrical channel length L, the (relative) effect of channel length modulation is much more pronounced for short channel devices. Hence

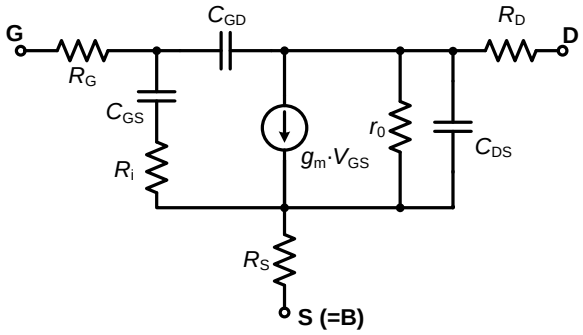


Figure 3.7: Typical small signal equivalent circuit model of a MOSFET valid up to mm-waves.

the quite non-ideal behavior of the $I_D - V_{GS}$ characteristic given in figure 3.6 for the 65 nm NMOS device.

This section treated the basic properties of the transistors included in the DK and showed that the minimum gate-length n-channel LVT GP transistor is the best choice for low-power high-performance mm-wave design. Further information on 65 nm MOS transistors are given in subsection 3.2.2.4, which introduces a small-signal equivalent circuit for the MOSFET and sub-section 3.2.2.5, which shows the transistor's multifinger layout. In a later section 3.6, more design-related issues like transistor biasing or source degeneration are discussed.

3.2.2.4 *Modeling the MOSFET's behavior*

To accurately represent the transistors' behavior in circuit simulations (which are done using SPECTRE (RF) of the Cadence[1] design framework), BSIM4[2] models are used. They are available in the DK with parameters accurate up to 50 GHz for all types of MOSFETs, and also simulate the effect of the polysilicon gate resistance R_G. To take into account the parasitics of the metal layout, for each transistor a parasitic extraction is done. It yields a netlist representing the extracted transistor's behavior based on its layout and also includes all metal interconnects up to the terminals. This netlist, typically composed of several hundred elements per transistor, is subsequently taken into account during simulation.
To gain insight in the dominating parasitic effects and for manual first-order calculations, however, BSIM4 models are much too complex . A more instructive means to characterize the behavior of the transistor at a given bias point is its small signal equivalent circuit: figure 3.7 gives such a equivalent circuit of a MOSFET suited for hand analysis at mm-waves. It is the combination of more or less complex equivalent circuits found in [12, 12, 61, 148, 154].
The equivalent circuit contains the resistors at the gate, source and drain contacts, R_G, R_S and R_D, the intrinsic gate resistance R_i (which is the distributed channel resistance seen from the gate [157]), and the drain source resistance r_0 (which originates from channel length modulation as explained in section 3.2.2). The capacitors C_{GS}, C_{GD} and C_{DS} denote

[1] Version 5.10.41.500.4.73

[2] Developed by the Device Research Group of the Department of Electrical Engineering and Computer Science, University of California, Berkeley. Available at http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html

Normalized Parameter	Value	unit
$R_G \cdot W$	45 (2 contacts)	[Ω·µm]
$R_S \cdot W$	$200 - 250$ [156]	[Ω·µm]
$R_D \cdot W$	$200 - 250$ [156]	[Ω·µm]
$R_i \cdot W$	≈ 15.5 [157]	[Ω·µm]
r_0	7300	[Ω·µm]
C_{GS}/W	1.14	[fF/µm]
C_{GD}/W	0.39	[fF/µm]
C_{DS}/W	0.6	[fF/µm]
g_m/W	1.25	[mS/µm]

Table 3.1: Normalized values for the equivalent circuit's elements, simulated, estimated by manual calculations, or obtained from literature. The given values correspond to a 26×1µm wide 65 nm LVTGP n-channel transistor with gate contact on both sides, biased at a drain current density of 0.2 mA/µm and with $V_{DS} = 1$ V.

the capacitances present between the indicated terminals. They include the parasitics added by the metal back-end. C_{DS} also contains coupling to the bulk that is assumed to be shorted to the source. The transistor's transconductance is given by g_m.
The equivalent circuit can be extended to gain accuracy (e.g. by adding parasitic contact inductances) or simplified for more basic considerations (e.g. by removing the intrinsic gate resistance R_i). The typical values of all elements for 65 nm LVT GP n-channel transistors with dual gate contact are given in table 3.1. They have either been simulated using the extracted DK models described above (assuming a transistor with 26 fingers of 1 µm width), been estimated using simplified calculations based on technology parameters, or been adopted from [156].
To understand the influence of the elements of the equivalent circuit on the transistor performance, it is instructive to use them in order to write down equations for the cutoff frequency f_T and the frequency of maximum oscillation f_{max}. A variety of equations have been published to this end, using different simplifications [12, 148, 158–161]. The expressions given here are extracted from [160] and [158]. Based on a definition of the *intrinsic* cutoff frequency

$$f_c = \frac{g_m}{2\pi C_{GS}}, \tag{3.2}$$

which gives the intrinsic ability of a FET to amplify high frequency signals [160], the transient frequency can be expressed as

$$f_T \approx \frac{g_m}{2\pi C_{GS}\sqrt{1 + 2\frac{C_{GD}}{C_{GS}}}} = \frac{f_c}{\sqrt{1 + 2\frac{C_{GD}}{C_{GS}}}}, \tag{3.3}$$

which simplifies to f_c in the unilateral case ($C_{GD} \to 0$).
The formula to calculate f_T given in equation (3.3) does not take into account the resistive parasitics. This is a common simplification that originates from the fact that f_T is based on current gain: thus, the voltage drop over gate, drain and source resistors do not have an immediate effect on f_T. However, this simplification is not always justified. For certain device geometries and bias points, the resistors *do* have a non-negligible effect on f_T. A more accurate formula for f_T that takes into account the resistances at gate, drain and source is given by P.J. Tasker

et al. [161]. The influence of the resistive elements on the measured f_T is discussed in detail in their paper.
Nevertheless, the performance that exhibits a transistor used in an amplifier or oscillator circuit is not adequately represented by f_T, as it is power gain rather than current gain which is exploited in these components. The more adapted figure of merit is in this case is the maximum frequency of oscillation f_{max}. It can be defined by [158]

$$f_{max} \approx \frac{f_c}{2\sqrt{R_G\left(g_m \frac{C_{GD}}{C_{GS}}\right) + \frac{1}{r_0}\left(R_G + R_S + R_i\right)}}. \tag{3.4}$$

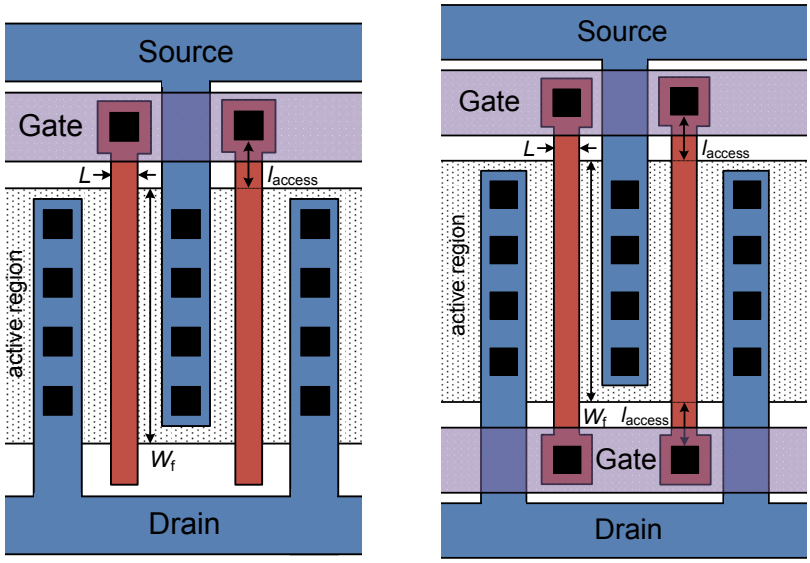
This equation shows the considerable impact of the extrinsic gate resistance R_G. Because R_G can be easily influenced by the transistor layout, also f_{max} is very layout dependent and can be optimized using multiple fingers of appropriate size [61, 158]. Section 3.2.2.5 discusses this topic. While the other elements used in (3.4) also have a decisive impact [160], their values are less layout dependent. Thus, the most important means to influence them is an optimal choice of the bias point as detailed in the previous subsection 3.6.1.

3.2.2.5 *The MOS-transistor layout*

The physical implementation of MOSFETs with identical gate width W and gate length L can differ a lot by its layout. The layout, in turn, influences the transistor's performance via the elements of the transistor's equivalent circuit (see section 3.2.2.4). Thus, its optimization is crucial during RFIC design, especially at mm-waves. In the following, some of the key aspects in this regard are addressed and the transistor layout adopted for this thesis is shown. More details on analog MOSFET layout can for instance be found in [154].

THE MULTIFINGER LAYOUT Rather than using a single gate of width W and one source and one drain contact on its sides, folded structures are usually employed when laying out a MOS transistor. They comprise N_f fingers of width W/N_f to reduce the source-drain junction area and the gate resistance R_G. The former reduction is due to the fact that one drain (or source) finger inside the multifinger layout serves two gates. The latter, namely the reduction of R_G, is discussed in the following.
Figure 3.8 shows two basic multifinger layouts of MOS transistors. The source and drain areas are directly contacted to the first metal layer. Due to the low resistivity of these metal fingers ($R_{sheet} \approx 0.15\,\Omega/\square$[1]), the added parasitic source and drain resistance remain small with respect to the channel sheet resistance [148].
On the other hand, the gate fingers are made of silicided polysilicon and contacted to a metal strip only at their end(s). Because the poly sheet resistance ($\approx$ 15 $\Omega/\square$) is about a hundred times higher as in the case of the drain and source metal contact strips, the finger width $W_f = W/N_f$ needs to be kept small: according to A. Cathelin *et al.* [162], and in agreement with most designs found in literature [61, 153], the most common compromise is $W_f = 1\mu m$. Further reducing W_f does not considerably improve transistor performance, because other resistive parasitics (cf. section 3.2.2.4) then dominate the transistor's behavior. For very wide devices, slightly longer finger widths should be adopted

[1] given in Ohm per square, denoted $\Omega/\square$



(a) MOSFET layout with one-side gate contact

(b) MOSFET layout with two-side gate contact

Figure 3.8: Illustration of MOSFET multifinger layouts using single or double gate contacts

to avoid too long, narrow devices, because otherwise the gate excitation is not uniform any more. Except for these cases of very wide transistors (i.e. $W \geqslant 50\mu m$), 1 µm is used in the designs of this thesis.
Two possibilities exist to contact the very resistive polysilicon gate stripes to the metal layer that leads to the gate terminal: the first possibility, illustrated at the left side of figure 3.8, is to connect the gates on one single side. Advantages are that parasitic coupling from gate to source (or drain) is minimized [156] and less area is required for the interconnect. However, the gate resistance can further be minimized: the second possibility consists in connecting both sides of the gate, leading to much lower gate resistance but increasing coupling from the gate metal to other interconnect lines.
The polysilicon gate resistance of a MOSFET with N_f fingers of width $W_f = W/N_f$ with single sided contact (see figure 3.8) is given in [156] by

$$R_G = \frac{1}{N_f}\left[\frac{R_{sheet}}{L}\left(\frac{W_f}{3} + l_{access}\right) + \frac{R_{cont}}{N_{cont}}\right], \tag{3.5}$$

where l_{access} is the length between the active region and the poly-to-metal contact, R_{cont} is the resistance of this contact, and N_{cont} the number of contacts per gate finger. To use (3.5) for gates with dual gate contact, N_f has to be taken as twice the number of fingers, and W_f has to be divided by two.
According to (3.5), for a gate width of 1 µm the normalized gate resistance $R_G \times W$ of a MOSFET with single-side gate contact is about $127\,\Omega\times\mu m$, reducing to $44\,\Omega\times\mu m$ for a double-side gate contact. The latter possibility is adopted for transistors used in this thesis due to its considerably lower gate resistance.

THE MOS-TRANSISTOR'S METAL BACK-END Figure 3.9 shows a three-dimensional view of the metal back-end that connects the drain,

source and gate contacts of a multi-finger MOSFET to three terminals on the highest copper metal layer (metal 7). The substrate is contacted to a ring in the metal 1 layer by p^+ taps. This ring closely surrounds the transistor and is contacted all along its edge to the groundplane that covers the entire substrate of the mm-wave circuit (cf. section 3.7.2).
The individual polysilicon gates are contacted on both sides and connected to two metal 2 strips that lead to the gate contact. The drain and source contacts of each finger are raised by a horizontal stack of vias and metals. Their mutual distance increases with the height over substrate to minimize the parasitic drain-source capacitance. Starting from metal 4, all drains and all sources of the individual fingers are interconnected.
Note also the presence of dummy transistors, whose gate fingers and outer terminals (either gate or source) are connected to the ground ring. They are added at each end of the multifinger layout to provide a uniform environment for all fingers, including the outermost ones [154].
Alternative transistor layouts are presented in literature, where the kind of structure shown in figure 3.9 is considered a unit cell that is repeatedly used: this allows a more regular excitation of the individual fingers and may provide better access to the transistor terminals by transmission lines. B. Heydari *et al.* arrange six of these unit cells to form a round-table layout for mm-wave power amplifiers [163]. B. Martineau *et al.* use two of these cells aligned next to each other, connecting the drain and gate access and providing two source terminals pointing towards the outside [164]. This facilitates integration in coplanar waveguides.
However, these more specific layouts increase area consumption and the overall improvements are usually small compared to an optimized multifinger layout. Hence, the transistors used for the circuits presented in this thesis employ the kind of layout presented in figure 3.9.

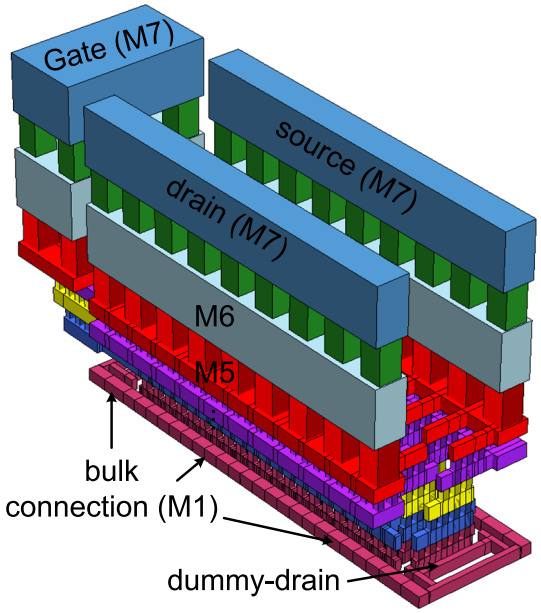


Figure 3.9: Three-dimensional view of the metal-backend of a multifinger transistor with 1 µm finger witdh and 10 effective gates.

EMBEDDING THE MOSFET IN A DEEP N-WELL As mentioned in section 3.2.2, the 65 nm CMOS technology provides the possibility of creating deep n-wells. This allows the isolation of an n-channel MOSFET from the grounded substrate, and thus the shifting of all its terminal potentials. Hence, supply voltages exceeding 1 V can be employed in circuits using stacked LVT GP transistors.

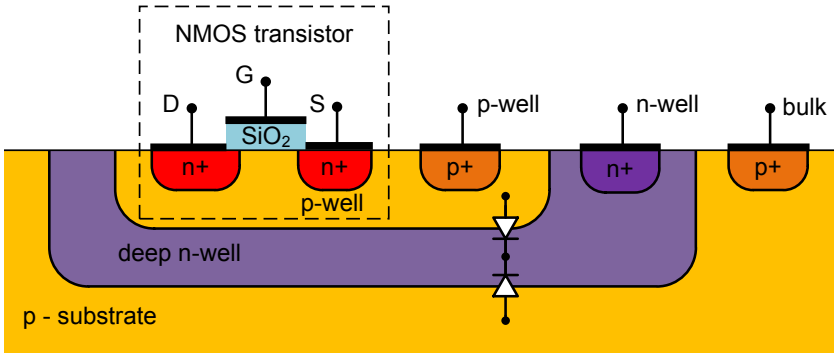


Figure 3.10: n-channel MOS transistor embedded in a deep n-well (parasitic diodes between the wells and the substrate are indicated)

Figure 3.10 shows an NMOS transistor inside a deep n-well. As p-n junctions form at the interfaces between the regions of different doping, parasitic diodes are created. Their influence on the circuit must be minimized by appropriately biasing the well's contacts. The presented structure is used in the LNA circuit to isolate the cascode device, thus permitting an increased supply voltage of 1.5 V.

3.2.3 *Capacitors*

The 65 nm CMOS DK contains different types of capacitors, either based on active devices or constituted by the back-end metalization. Due to the fact that a high quality factor, low parasitics and good linearity are essential for capacitors used in 60 GHz design, only the latter ones are of interest for this thesis. Their capacitance density is sufficient for providing the required capacitance values (ranging from 10 fF to 200 fF for matching purposes, and up to 1 pF for decoupling) with reasonable size. In the following, Metal Insulator Metal (MIM) and Metal On Metal (MOM) capacitors, which are both available in the DK, are introduced.

The **MIM capacitor** is a parallel plate capacitor implemented using two additional, thin metal layers and a special MIM dielectric as illustrated in figure 3.11. This structure is necessary due to the physical relationship that governs the capacitance of two parallel plates: It is (without taking into account fringing fields) given by

$$C_{plate} = \epsilon_r \epsilon_0 \frac{A}{d}, \tag{3.6}$$

where A is the plate area, d the plate distance and ϵ_r the dielectric's relative permittivity. To achieve a sufficiently high capacitance density, d has to be smaller than the distance between two metal layers of the standard metal back-end, and the permittivity should be increased with respect to the one of the low-k dielectric. Due to these measures, the DK's MIM capacitors achieve a capacitance density of about 5.0 fF/µm^2.

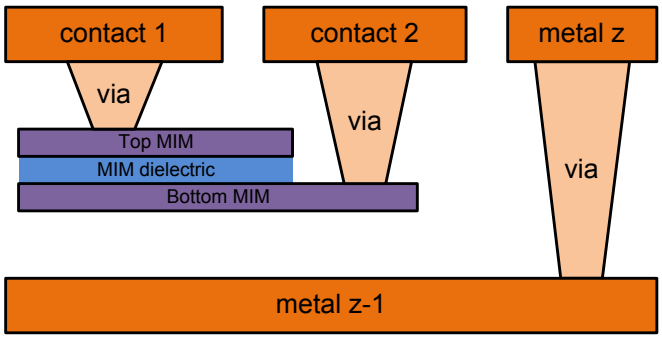


Figure 3.11: Illustration of a MIM capacitor inserted between two thick metal layers

The **MOM capacitor** is implemented without using special metal and dielectric layers. To nevertheless achieve a high capacitance density, a large number of metal fingers are employed. The fingers connected to the first contact of the capacitor are surrounded by fingers connected to the second contact, and vice versa. This creates a multitude of lateral and horizontal, as well as fringing capacitances. Figure 3.12 shows a typical implementation of such a capacitor. The MOM capacitors given in the 65 nm CMOS DK achieve a capacitance density of about $2.5\,\mathrm{fF}/\mu\mathrm{m}^2$, which is half of the value achieved for MIM capacitors.

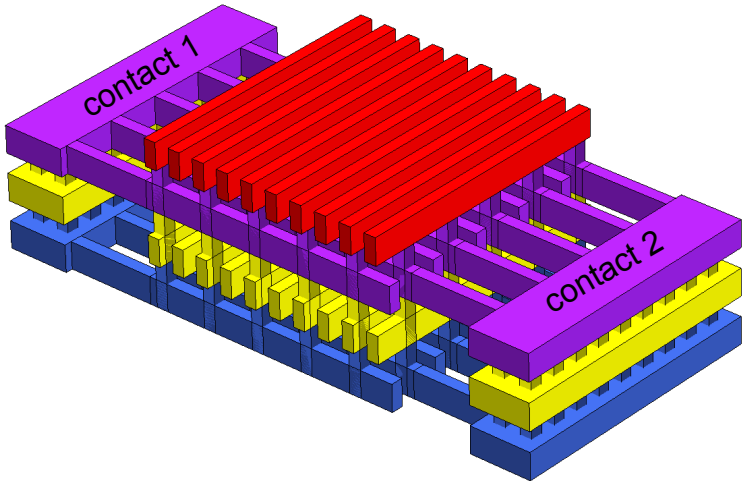


Figure 3.12: Typical structure of a MOM capacitor

3.2.3.1 *The quality factor*

Besides the capacitance density, the parasitic losses accompanying a desired capacitance value need to be evaluated. The quality factor Q of a reactive component is given by the ratio between the maximum stored reactive energy and the energy lost per unit time [133, 165] (times 2π for mathematical convenience). In the case of a capacitor, the quality factor is decreasing with frequency ($Q_C = 1/\omega R_s C$, where R_s is the series resistor representing loss). The effective quality factor,

$$Q_{\mathrm{eff}}(f) = \frac{\Im\{Z(f)\}}{\Re\{Z(f)\}}, \tag{3.7}$$

is used in the following to quantify the Q of a single reactive element. The frequency-dependent impedance $Z(f)$ is obtained by measurements of the scattering parameters.

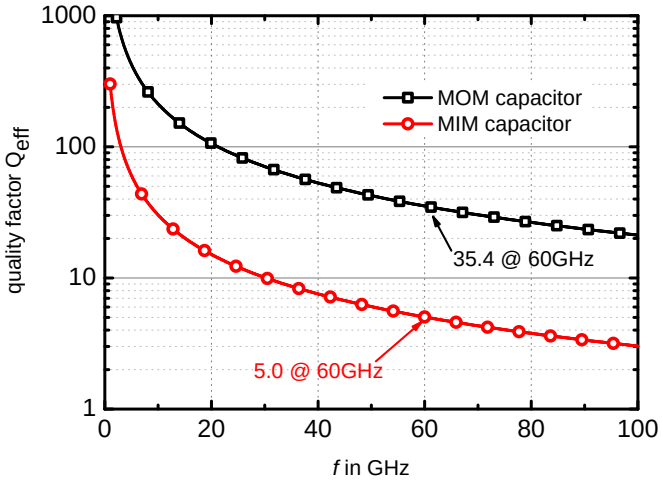


Figure 3.13: Comparison of the effective quality factors of MOM and MIM capacitances of value 100 fF. Plots obtained by DK simulation in accurate mode.

Figure 3.13 plots the effective quality factor of both MIM and MOM capacitors. A drastic difference in favor of the MOM capacitance can be observed, while the MIM capacitor is practically useless at mm-wave frequencies due to the high associated loss. Thus, MOM capacitors are exclusively used for circuit design in this thesis.

3.2.4 *Resistors*

In CMOS technology, stripes made of polycrystalline silicon (also called polysilicon or poly) of defined geometry are commonly used to create resistors [154]. The principle structure of such a resistor is given in figure 3.14. In the 65 nm CMOS DK, a variety of such resistors are available, made of N^+ silicided and non-silicided polysilicon, P^+ non-silicided polysilicon or special high resistivity polysilicon. The non-silicided resistors are fabricated by blocking the silicide deposition on top of the poly layer, thus achieving high resistivity [154].

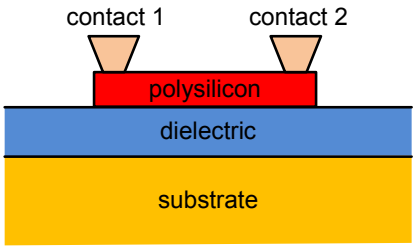


Figure 3.14: Principal structure of a polysilicon resistor

For the circuits designed in this thesis, N^+ poly silicided resistors[1] are used if low resistance values are required. A 0.25 µm x 5 µm stripe has a resistance of 273 Ω, which increases to 310 Ω if contact parasitics

[1] called *rnpo* in the DK

are included. For larger values, P^+ poly non-silicided resistors[1] are employed. A 0.25 µm x 5 µm stripe has a resistance of 3743 Ω, which grows to 3816 Ω with contact parasitics.
In order to obtain resistors that work in the mm-wave range, their width has to be minimized and the resistance values are limited to low values (typically below 1 kΩ). Otherwise, parasitics become dominant. In the circuits presented in this thesis, resistors were not used directly in the 60 GHz signal path, but only for bias circuitry (which touches the gates of the 60 GHz transistors) and baseband building blocks.

3.3 FULL-CUSTOM VARIABLE CAPACITORS

In order to dynamically change the frequency of operation of microwave components during operation, variable capacitors (also called varactors or varicaps) are usually used. They are especially important to change the oscillation frequency of VCOs. Since the 65 nm design kit does not contain varactors optimized for mm-wave operation, a full-custom varactor has to be designed. Its most important metrics are the quality factor Q_{eff} (as defined in (3.7)) and the tuning range $\frac{C_{max}}{C_{min}}$ [12].
Variable capacitors have traditionally been realized as **reverse-biased diodes** [166]. However, for them to exhibit a high tuning range, the junction depletion capacitance (whose value is influenced by the reverse bias voltage) has to be maximized. This is done using hyper-abrupt doping profiles, which are not available in digital CMOS technologies for cost and fabrication reasons [78]. Nevertheless, diode varactors can be realized in the 65 nm CMOS technology, for example using adjacent p^+-n^+ implants isolated from the substrate by placing them in an n-well. However, the performance of this kind of diode varactors, especially with respect to the achievable quality factor, remains inferior to MOS-based solutions in submicron CMOS technologies [166–168]. Hence in the following the different possibilities of varactors employing MOS technology are analyzed, based on more detailed explanations found in [166, 167]. The variable capacitance C_{var} of these kind of devices is constituted of the polysilicon gate of size $W \times L$, the gate oxide of thickness t_{ox} and the doped substrate. The capacitance C_{var} is a function of the density of free charges in the substrate, which depends on the applied voltage V_{tune}. Its maximum value $C_{var,max}$ is given by $C_{ox} = \epsilon_0 \epsilon_{ox} LW/t_{ox}$, where t_{ox} is the gate oxide thickness and ϵ_{ox} its relative permittivity.
The straight-forward possibility to realize a **MOS varactor** is to short-circuit the source, drain and bulk terminals of a MOS transistor. The control voltage $V_{control}$ is applied between this common terminal and the gate terminal. As illustrated qualitatively in figure 3.15, the different regions of operation of the MOSFET exhibit different C_{var} values [167]. If $V_{control}$ (i.e. the voltage between the source-drain-bulk terminal and the gate) is zero, the channel is depleted, and few mobile charge carriers exist at the channel to oxide interface. Thus, one can imagine an additional capacitance representing the extension of the depletion region in series to C_{ox}. When the device is gradually entering inversion (from weak over moderate to strong inversion), more and more minority carriers are attracted to the oxide-channel interface. They form a second capacitance in the substrate that gradually short-circuits the capacitance formed by the depletion region. Summing up, the increase

[1] called *rpporpo* in the DK

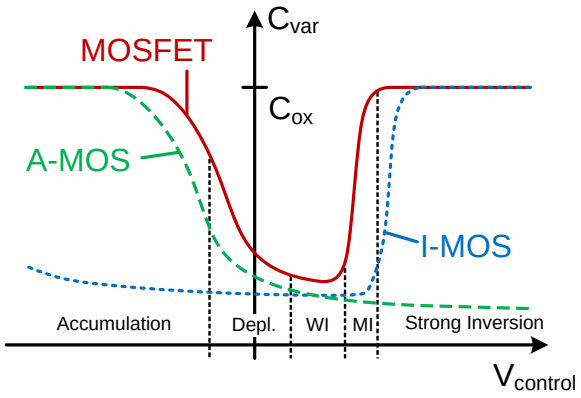


Figure 3.15: Principal capacitance variations of varactors based on MOS technology versus tuning voltage as given in [167] (indicated regions of operation are only valid for the MOSFET, which is of p-channel type if the tuning voltages is applied from the common terminal to source as for the other varactors.)

in C_{var} from depletion region to strong inversion stems from minority carriers populating the channel.
The opposite is the case for an inversed control voltage: majority carriers accumulate in the depleted channel, gradually removing the effect of the series capacitance representing the depleted substrate. The value of C_{var} here also approaches C_{ox} when the number of majority carriers is sufficiently high at the oxide interface. Note that for the accumulation effect the potential difference between the gate and the bulk (and not the source and drain implants) is decisive, because this is where the accumulated majority carriers are attracted from.
Figure 3.15 qualitativly shows the resulting $C-V$ characteristic of this MOSFET varactor: the capacitance C_{var} does not change monotonically, but exhibits is maximum value for very positive *and* very negative tuning voltages. This poses problems for large-signal applications like VCOs [167, 169]: because the RF signal applied over the varactor has a large amplitude in this case, the effective capacitance is not the small-signal value at a given $V_{control}$. Rather, it is the mean value around this point. Hence, in the case of the MOSFET varactor the minimum value is never achieved under large-signal excitation, because it is too close to higher values that have also to be taken into account during averaging (for curves illustrating this behavior, see [169]).
To obtain a monotonic behavior, one of the two regions that are characterized by a high charge density at the oxide-substrate interface has to be avoided. As illustrated in figure 3.15, this can be achieved either by an Inversion-mode MOS (IMOS) varactor (avoiding accumulation) or an Accumulation-mode MOS (AMOS) varactor (avoiding inversion).
The **IMOS varactor** can be realized e.g. based on a standard p-channel MOSFET [167]. Like discussed above, drain and source are connected together to form one of the capacitor's terminals. However, to ensure that the transistor does not enter the accumulation region for normal control voltages, the bulk contact of an IMOS varactor is not connected to the common source-drain terminal, but to a fixed, high potential like the supply voltage V_{DD}. This avoids the accumulation of majority carriers that would be attracted by a positive gate-bulk voltage. (Note that n-channel versions are also possible, but they are not isolated from the

circuit's substrate by an n-well like in the p-channel case). The resulting curves are shown in figure 3.15, where the shift of the IMOS varactor's $C-V$ curve stems from the slightly increased threshold voltage of this device.
The advantage of the above described varactors is that they make use of standard (usually p-channel) MOSFETs. The drawback they have in common is the high parasitic resistance associated with the FET's channel: this resistance originates from the R_{on} resistance of the MOSFET in the linear region [154, 167]. To avoid this resistance, the MOS capacitance exploited in the varactor has to be realized without the use of a transistor.
To realize an **AMOS varactor**, i.e. a structure that does not contain an inversion channel, the typical drain-bulk-source structure of a MOSFET is replaced by an n-well with contacts realized by n^+-implants. Figure 3.16 shows this device, which closely resembles a MOSFET. This permits the use of the same geometrical parameters (gate length L, gate width W, etc.) and nomenclature as for transistors.

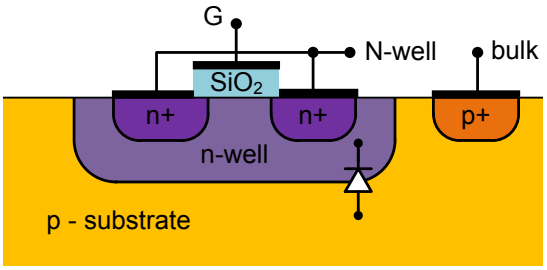


Figure 3.16: Principle structure of an accumulation-mode MOS varactor in an n-well

The value of the AMOS varactor's capacitance C_{var} is solely controlled by the number of majority carriers in the otherwise depleted channel. As no source of minority carriers exist, an inversion of the channel is avoided. According to the control voltage applied between n-well and gate, more or less charges are accumulated at the n-well - oxide interface. The result is the tuning curve given qualitatively in figure 3.15. Figure 3.16 also shows the parasitic diode that forms between the n-well and the p-substrate: to avoid that this diode interferes with the varactor's behavior, the n-well potential should not fall below $\approx -0.6\,\mathrm{V}$ (given that the substrate is grounded). Alternatively, the p-type substrate could be used to implement the varactor. However, that solution implies one node at substrate potential and inferior Q factor due to lower carrier mobility of the holes that are the majority carriers in this case [12, 170].

The AMOS varactor can either be optimized for high Q or for high tuning range. To understand how to influence the former metric, it is instructive to consider an analytical expression of the transistor's quality factor. Because Q is principally limited by the resistance of the gate and n-well contacts, according to [171, 172] it can be approximated by

$$Q \cong \frac{1}{\omega R_s C} = \frac{12}{\omega C_{ox}\left(R_{\square,n-well} L^2 + R_{\square,poly} W_f^2\right)}. \tag{3.8}$$

A two-sided gate contact and a multifinger-layout is assumed, and contact and metal resistance are neglected (cf. section 3.2.2.5 for a more exact description of a transistor's multifinger layout and the more complete calculation of its gate resistance).
Note that $R_{\square,poly}$ is about 50 times lower than $R_{\square,n-well}$, whose value amounts to approximately 800 $\Omega/\square$. In the available 65 nm CMOS technology, the latter resistivity can still be decreased by about a factor of two, if using a deep n-well below the n-well the varactor is embedded in.
In technologies with minimum gate lengths well above 65 nm, the optimization of the Q factor according to (3.8) essentially consists in the minimization of L [49, 171]. This permits W_f values of several microns, because the gate resistance term can be considered negligible. However, if L=65 µm, the gate resistance becomes the dominant term even for gate finger widths W_f well below one micron. Thus, if the focus is on Q optimization, both L and W_f need to be minimized.
Equation (3.8) also shows that a lower oxide capacitance C_{ox}, for example obtained by using LP instead of GP gate oxide, could increase Q. J.L. Gonzalez *et al.* even suggest the use of a special *thick* gate-oxide that usually is used for the output transistors in digital circuits, to further decrease C_{ox} [173]. The penalty is the relative increase of parasitics due to lower capacitance density.
To further increase the differential Q of a varactor e.g. applied in differential VCO, A.-S. Porret *et al.* [166] propose the implementation of two varactors in the same n-well with two distinct gate electrodes between which the capacitance appears. If this varactor is excited in odd mode, a virtual ground appears inside the n-well at the symmetry plane between the fingers of the two varactors. Due to the short, low resistance path to this ground, the Q in odd mode can be considerably increased.

The considerations above aim to maximize the varactor's quality factor. However, this can result in quite low tuning ranges, which may be undesired. To increase the tuning range, the parasitic capacitances that do not vary with the tuning voltage because they originate from capacitive coupling between adjacent metal or polysilicon structures need to be minimized. C. Cao *et al.* give some hints on this optimization in [171]: one important point is to avoid the use of minimum allowed distances, which can be very small in deep sub-micron CMOS technologies. For example, the n-well to metal contacts on both sides of the polysilicon gate fingers shall maintain a certain distance to the gate. Furthermore, the metal layout that connects the gate and n-well fingers to the two varactor terminals on higher metal layers has to be done in a way to minimize capacitance.
If the Q factor is less critical, L and/or W_f can be increased, resulting in a higher tuning range. As illustrated by the plot of Q and $\frac{C_{max}}{C_{min}}$ over L given in [171], a chosen finger size results in a specific tradeoff between these two key figures of merit of the varactor.
Figure 3.17 shows the metal layout of the AMOS varactor adopted in this thesis. It is used to connect the active part of the varactor, which is illustrated in figure 3.16, to common terminals on a thick copper metal layer. To maximize Q, the minimum gate length and a finger width of W_f=0.78 µm are chosen. All gate fingers are interconnected on both sides by polysilicon and metal 1, but only one of these sides is contacted to the gate terminal that unites all fingers one side of the

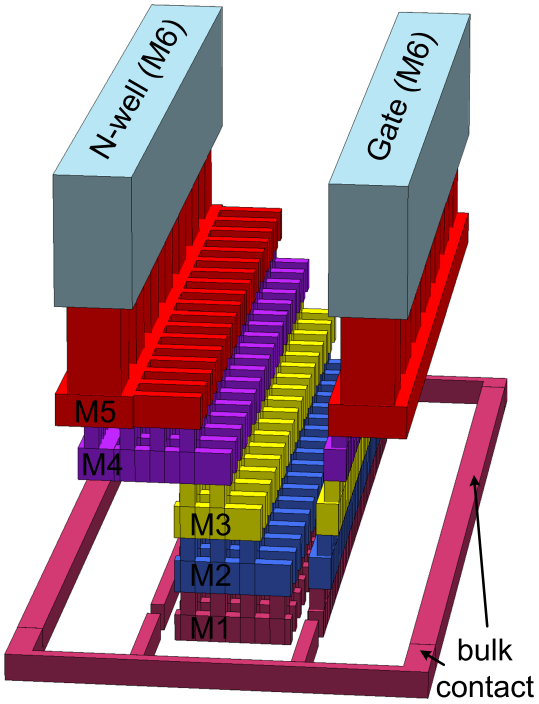


Figure 3.17: Metal back-end of the multifinger varactor layout based on a SVT GP device. Minimum-length fingers with W_f=0.78 µm width are used.

varactor. The n-well contacts are interconnected on the other side. Note that, like in the case of the transistor, dummy fingers are employed. However, their n-well contacts are floating, because a connection to a fixed potential (e.g. ground) would connect the whole n-well to this point.
Due to the full-custom nature of the presented varactor, appropriate models are not available in the DK. While methods exist (for instance by K. Molnar *et al.* [174]) to model AMOS varactors based on BSIM transistor models , the access to the parameters of these models for the

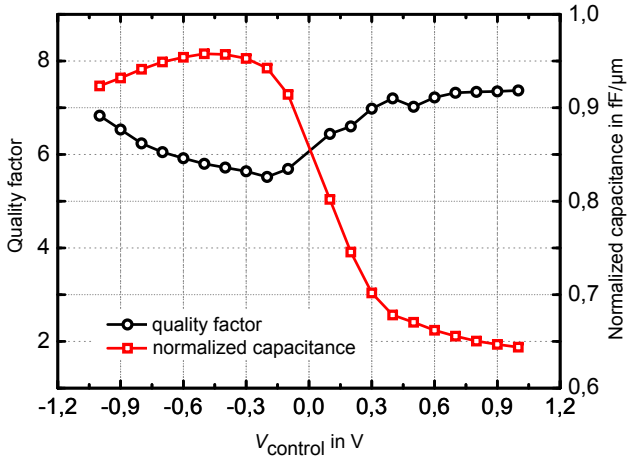


Figure 3.18: Measured normalized capacitance and effective quality factor versus $V_{control}$ of the realized test-varactor at 60 GHz (width 51 × 0.78 µm)

65 nm technology was not possible. Thus, either simple, linear $R-C$ equivalent circuits are used for circuit design, or, if the nonlinear tuning behavior has to be simulated, the MOSFET models with shorted $D-S-B$ terminals are employed. Note, however, that varactors modeled by the latter means are not of the AMOS type.
Figure 3.18 shows the results obtained by measuring a test structure of the full-custom AMOS varactor at 60 GHz. Their accuracy is ensured by the use of the de-embedding approach presented in section 3.5. The effective quality factor (cf. section 3.2.3 for its definition) is about $Q_{eff} = 6.5 \pm 1$, while the normalized capacitance varies between $C_{var,min}$=0.64 fF/µm and $C_{var,max}$=0.96 fF/µm. The tuning ratio $\frac{C_{var,max}}{C_{var,min}} = 150\%$ shows that the variation of the capacitance remains quite limited. This is due to parasitic capacitances that arise from the proximity of the gate fingers to the n-well contact. These parasitics can be further decreased if optimizing the varactor layout as detailed above or increasing the gate length L. However, a compromise between tuning range and quality factor had to be found. Thus, for the VCO presented in this thesis, the varactor presented above is adopted.

3.4 FULL-CUSTOM PASSIVE DEVICES

The main purposes of the passive devices presented in this section are to serve as inductive elements for matching networks, provide single-ended-to-differential conversion and bridge distances between devices and contact pads.
In **Monolithic Microwave Integrated Circuits (MMICs)**, which are based on compound semiconductors and usually exhibit circuit sizes comparable or superior to the wavelength of interest, distributed elements are commonly employed to provide the above-mentioned functionality. They prove advantageous with respect to lumped elements due to the features of MMIC technologies (e.g. realizable distances and tolerances, low-loss substrate, lower cost per area, etc.).
However, for the design of mm-wave circuits in nanoscale CMOS technologies, the premises above become obsolete and should be replaced by the ones of the RFIC paradigm.
In **Radio Frequency Integrated Circuits (RFICs)**, which are based on silicon technologies like CMOS or SiGe and usually exhibit circuit sizes smaller than the wavelength, the use of lumped elements becomes advantageous. Very small-size passive devices are feasible due to the extremely small metal widths and distances that can be realized in the available multi-layer metal back-end. The associated, very tight fabrication tolerances ensure an excellent repeatability of the achieved performance. The small size helps to enhance the device's performance, as the magnetic field is concentrated (due to loops), the area over the lossy substrate is minimized, conductor loss is reduced (due to shorter conductors) and distributed effects become negligible. Furthermore, die area is minimized when using lumped elements, which is mandatory for low-cost applications.

While especially at the beginning of the research on 60 GHz CMOS design, distributed elements were commonly employed following the MMIC paradigm, work based on spiral inductors regularly exhibits superior performance and smaller circuit size [51, 69, 175, 176].
As a consequence, the work presented in this thesis follows the RFIC paradigm. Thus, in the following, the emphasis is on the design of spiral inductors, which is discussed in detail in subsections 3.4.1 to 3.4.4. For single-ended-to-differential conversion, transformers are proposed in sub-section 3.4.5. The use and performance of transmission lines is only briefly discussed in subsection 3.4.6.

3.4.1 *Spiral Inductor Design Flow*

Unlike RFIC design at low GHz frequencies, where mature spiral inductor layouts and models are usually included in the DK, the design at 60 GHz necessitates the creation of full-custom devices from scratch. Figure 3.19 shows the design flow starting from the specifications up to a complete, validated circuit model of the inductor:
Once the requirements on an inductor are established, its geometry is fixed according to the design guidelines. Then, its exact behavior is simulated. If necessary, the geometry is adjusted until the simulation results are satisfactory. Alternatively, a simulation with the goal of optimizing certain aspects of the inductor is launched. Then, an equivalent circuit model of the inductor is created for use in circuit simulation.

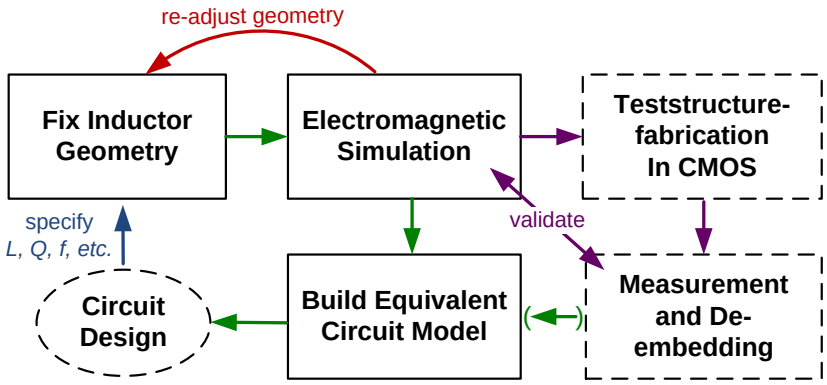


Figure 3.19: Design flow for mm-wave full-custom spiral inductors

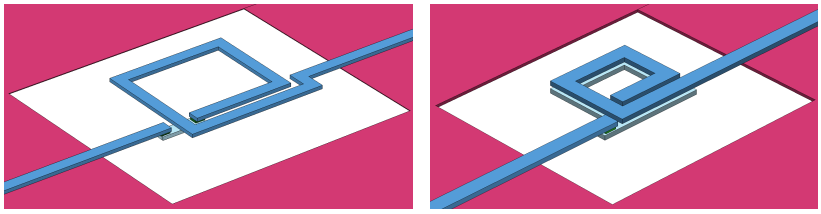
The validation of the simulations by the characterization of a fabricated test structure is necessary only at the beginning, to ensure that the simulations yield accurate results for the type of passive device used. The design flow of figure 3.19 is followed in this thesis. Its different steps are described in the following subsections:

- 3.4.2 discusses design guidlines that need to be respected when **fixing the geometry** of the spiral to achieve high Q inductors with high self-resonance frequencies
- 3.4.3 describes how **electromagnetic simulations** must be conducted to achieve accurate results. It also analyzes different types of Electromagnetic (EM) simulation software suitable for this task.
- 3.4.4 shows the **equivalent circuit model** used to represent the inductor's behavior in circuit simulations.
- 3.5.1 discusses the properties of a typical **test-structure** suitable for the characterization of test inductors.
- 3.5.2 discusses how to accurately remove the influence of test-structure parasitics from mm-wave inductor **measurements**.

3.4.2 *Spiral Inductor Design Guidelines*

The design of mm-wave spiral inductors follows many of the guidelines developed for RFIC spiral inductors at lower frequencies [177–181]. Nevertheless, some modifications and extensions of these rules are necessary to get optimal spirals at mm-waves. The landmark paper of T.O. Dickson *et al.* proposes such modified guidelines valid for CMOS inductors in the 30 to 100 GHz range [51]. Its most important observation is that substrate coupling, and not series loss, is usually limiting the quality factor of 60 GHz spiral inductors.
In the following, the design guidelines applied in this thesis are summarized. They originate from the above-cited references as well as extensive simulations and measurements. They are tailored to the 65 nm CMOS metal back-end described in sub-section 3.2.1.

PLANAR VERSUS STACKED INDUCTORS Spiral inductors can be implemented either as planar inductors or stacked inductors as illustrated in figure 3.20.



(a) planar inductor (b) stacked inductor

Figure 3.20: Planar inductor geometry versus stacked inductor geometry

The planar version, shown in figure 3.20a, is implemented in a single (usually the top-most) metal layer with underpasses in the layer below for metal crossing. It maximizes distance to substrate.
A stacked inductor is shown in figure 3.20b. Two turns implemented in the two topmost copper layers are used to form this spiral. While the distance to substrate decreases, this kind of inductor drastically reduces area over substrate, as the inductance is proportional to the squared number of turns. The reduced area results in a lower parasitic capacitance to substrate (at least if the employed metal layers remain far from substrate).
Both inductor types are employed in this thesis:

- Single-turn planar inductors are beneficial for low inductance values (below about 150 pF), as their surface remains small enough and stacking would cause the opposed, parallel conductors to be too close to each other.
- Stacked inductors, implemented in the thick copper metal layers (M6 and M7), are used for larger inductance values. In these cases, the opposed conductors are far enough from each other, avoiding considerable canceling of their magnetic fields (the inductor is hollow as recommended by [177]).

DESIGN OF THE SPIRAL The design of the spiral is done according to the following guidelines that in particular aim to minimize the influence of the lossy substrate:

- The topmost, thick copper metal layers M6 and M7 are used to implement the conductors. Only these layers have a sufficient distance from substrate (about 3 to 4 µm) and at the same time minimize series resistance due to their thickness and conductivity. While the alucap layer lies even higher, the lower conductivity is in disfavor to its use.
- A very narrow inductor width of about w=3 µm is employed to reduce the capacitance to substrate [51, 177]. (The width's upper bound is given by the horizontal skin effect. The lower limit is imposed either by the electromigration reliability rules or, if the differential quality factor Q_{diff}, which depends less on substrate coupling, is important, on the conductor series loss.)
- Inter-turn spacing is larger than required by design rules to reduce proximity effect (usually, s=2µm is chosen).
- The metal layers should not be shunted like sometimes suggested at lower frequencies as the increase in conductivity (limited by

the skin effect) does not justify the increase of substrate coupling by adding a lower metal layer.

- A squared spiral shape is employed due to the resulting ease of simulation and layout creation. The penalty in Q-factor with respect to an octagonal inductor usually remains below 5 %. Only for the VCO's tank inductor an octagonal shape, optimized for differential Q, is chosen (cf. section 4.3.2.3).

DESIGN OF THE GROUNDING STRUCTURE All inductors in this thesis are surrounded by a ground ring to reduce coupling to adjacent devices in the final circuit [51, 175] and to provide a low-loss, low inductance ground return path (cf. section 3.4.3.3). This ground ring either is realized by the ground plane or the cage structure presented in sub-section 3.7.2.
The distance between the ground ring and the inductor is subject to a compromise between different requirements: close proximity to the inductor reduces both total device size and the resistivity of the grounding structure. However, the ground ring can be considered a short-circuited second winding of a transformer that has as first winding the spiral inductor. A small distance to this ground ring would increase the coupling coefficient of this transformer. The induced current circulating in the grounding structure would be quite considerable, decreasing both inductance and quality factor of the spiral inductor. Thus, the distance between spiral and ground ring must remain above about half the spiral diameter.

Note that a ground shield, which is usually patterned to avoid eddy currents, is not beneficial for 60 GHz inductors implemented in the metal back-end of the employed 65 nm technology. This is due to the high capacitance between the spiral structure and this shield, which severely limits the achievable Self Resonant Frequency (SRF) and shifts the peak quality factor to lower frequencies.

The inductors used for circuit design in this thesis follow the above described rules, while adapting them to the requirements of the different circuits (favoring either high Q, high SRF, small size or in- and outputs at specific locations).

3.4.3 *Accurate Simulation of Spiral Inductors*

To characterize and improve the inductors designed following the guidelines given above, EM simulations are essential [177]. They are more problematic at mm-wave frequencies, because skin depth δ is much smaller compared to lower frequencies and substrate coupling is more pronounced. This sub-section deals with these simulation-related issues. After general considerations, it gives guidelines for the use of the inductance simulator ASITIC [182], the method-of-moment based planar EM software Sonnet V.12[1] and the finite element simulator HFSS V.12[2].
The results obtained from simulations carried out using the three soft-

[1] by Sonnet Software Inc.
[2] by Ansoft, LLC, a subsidiary of ANSYS, Inc.

ware tools are compared to measurements (cf. section 3.5 for their accurate de-embedding) of an inductor test structure, confirming the validity of the considerations given in this sub-section.

3.4.3.1 *A typical mm-wave inductor*

For the following considerations, the inductor test-structure of figure 3.21 is utilized. The inductor is designed for the use in the 60 GHz LNA described in section 4.2 and has a nominal value of about 150 pH. It was designed according to the guidelines given in subsection 3.4.2 as planar inductor on metal layer 7 with underpasses on metal 6. The access lines are drawn in the alucap layer and are de-embedded both in simulations and measurements.

3.4.3.2 *Inductor-simulation*

To accurately calculate the inductor's behavior, all kind of loss and coupling mechanisms have to be incorporated. Many of them are automatically taken into account, if the geometry and material properties are correctly entered to the EM software (like for example the magnetic and capacitive coupling between the turns of the spiral or the ohmic losses in silicon substrate). Depending on the solver type, some effects are neglected (ASITIC, for example, implements a quasi static solver and neglects substrate eddy currents. However, due to small inductor size ($\ll \lambda/10$) and moderate substrate conductivity of 65 nm CMOS, these are negligible in the present case).
The discussion in the following subsections concentrates on two important phenomena, namely the skin/proximity effect and currents in the grounding structure. They are essential for a correct simulation of the spiral inductors at mm-waves.

SKIN AND PROXIMITY EFFECTS The skin effect in the conductor has always been an issue in RFIC inductor design [177]. However, the skin depth

$$\delta = \sqrt{\frac{2}{\mu\sigma\omega}} \tag{3.9}$$

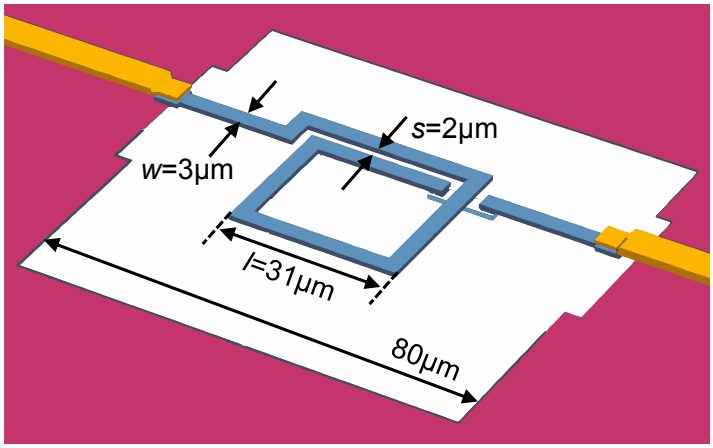


Figure 3.21: 3D view of the inductor used for the following analyses

Figure 3.22: Current displacement in the conductor cross section of the two turn side of the test inductor. Plot obtained by HFSS-simulation of the test-inductor, current density in logarithmic scale increasing to darker colors (see figure 3.23). The slightly higher current in the very inside of the metal is due to simulation artifacts.

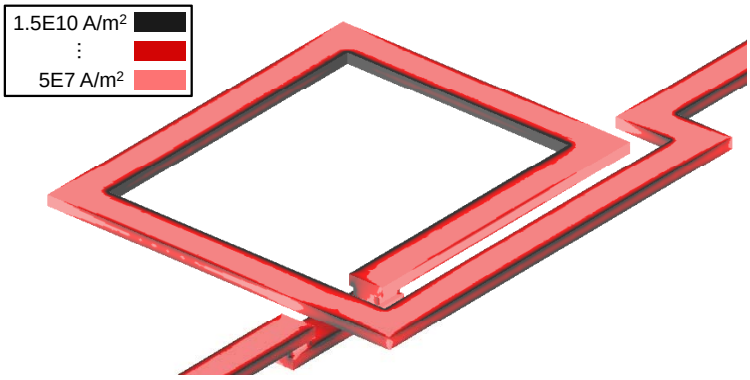


Figure 3.23: Plot of the current densities on the conductor surface. Plot obtained by HFSS-simulation, current density in logarithmic scale increasing to darker colors.

in copper ($\sigma = 5.8 \times 10^7$ Sm^{-1}) at a low frequency like 2 GHz is $\delta_{2\,\mathrm{GHz}} = 1.48$ µm, while at 60 GHz, $\delta_{60\,\mathrm{GHz}} = 0.27$ µm is obtained. Compared to the inductor thickness t of about 1 µm, $\delta_{60\,\mathrm{GHz}}$ presents a worst case for simulation: at the one hand equivalent surface resistance models are not yet applicable because the inductor is not thick compared to the skin depth. On the other hand, a coarse mesh (or a two-metal model) inside the conductor, while sufficient at lower frequencies, is not fine enough to resolve the skin effect. Figures 3.22 and 3.23 illustrate the low skin depth inside the inductor: it is clearly visible that the current is confined to the very edges of the inductor.
In addition to that, a similar physical phenomenon leads to the proximity effect, if more than one inductor is implied. It is represented in figures 3.22 and 3.23 by the fact that the current is pushed to the edges facing opposite directions. The adjacent sides carry virtually no current. The extreme current distribution due to these effects needs to be respected by the EM simulation, otherwise conductor loss is not modeled correctly and even the inductance is slightly overestimated.
Accurate representation of these effects in the considered simulators is achieved in the following ways:

HFSS Meshing inside metals has to be activated. An iterative algorithm is used to refine the mesh. Besides the S-parameters' relative change ΔS, other criteria like the effective quality factor Q_{eff} can be specified. In figure 3.24 convergence is illustrated in case of the test-inductor. An acceptable accuracy is achieved for about 120000 *2nd order* tedraheda, showing the computational effort it takes to correctly simulate Q.

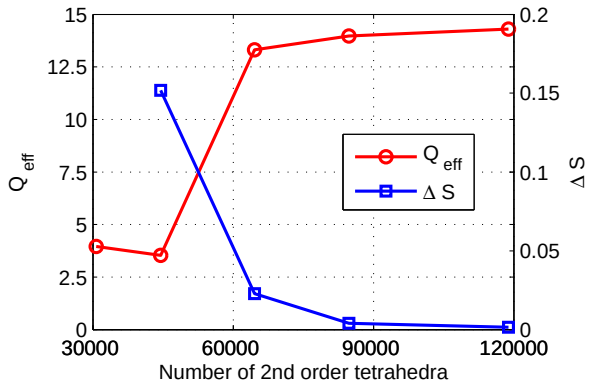


Figure 3.24: Convergence of the adaptive mesh refinement process in HFSS

SONNET The thick metal model allows to discretize the inside of the metal by N layers, where N has to be chosen to obtain a resolution of several layers per skin depth. A convergence analysis helps to find out when Q factor accuracy is achieved (here $N > 10$ in metal 7 for good accuracy).

ASITIC The metal is modeled by the Partial Element Equivalent Circuits (PEEC) approach, where the metal is discretized in all dimensions. The above described effects are taken into account, if the Finite Fourier Transform (FFT) size and the parameters *alpha* and *beta* (defined as the ratio between conductor thickness t and skin depth δ, i.e. t/δ, set to $\leqslant 0.3$) are correctly chosen.

In all solvers, meshing inside the conductor metal creates very large matrices. Their solution on personal computers is a task that became possible only recently due to their increased computational power and memory.

3.4.3.3 *Ground return currents*

A ground ring or even a ground-wall around the inductor is essential if coupling between the components in a circuit is to be avoided. In order to characterize the inductor in an environment close to the one encountered in the circuit, the grounding structure should be part of the simulation.

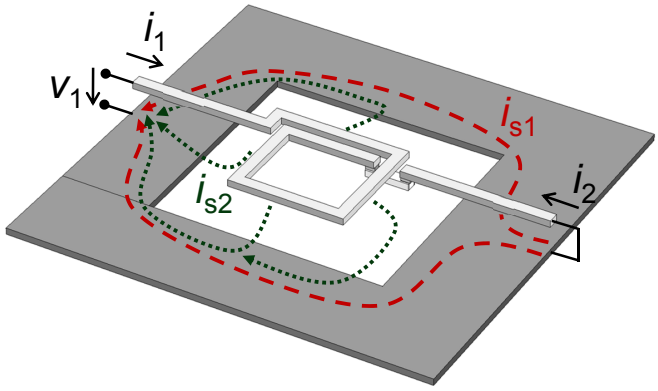


Figure 3.25: Illustration of ground return currents in a configuration used for the calculation of Y-parameters

In figure 3.25 the currents in the grounding structure are illustrated. The short-circuit termination shown in this figure is the one used for Y-parameter calculation, as inductance and effective quality factor are usually obtained from Y-parameters according to [51].
The return current i_{s1} takes the optimum path from the ground contact of port 2 to the ground contact of port 1. As the grounding structure has finite conductivity and non-zero dimensions, resistive loss R_{gnd} and inductance L_{gnd} is added to the inductor by this grounding structure. Approximations where these two grounds are at the same potential have to be carefully verified, especially at mm-wave frequencies. By optimizing the grounding structure, R_{gnd} and L_{gnd} can be greatly reduced.
Note that in circuits where many inductors and other devices are connected between the input and output port, the current i_{s1} is in general taking other ways as in the structure used to characterize the inductor. Thus in simulation of inductors it can be an option to remove L_{gnd} and R_{gnd} on device level and add these elements later on circuit level.
The second current i_{s2} is created by capacitive coupling from the spiral to the grounded silicon substrate below. From the substrate it flows to the metal grounding structure and back to the exciting port. Note that the sooner this current reaches the grounding structure, the lower the loss due to substrate resistivity is. However, approaching the ground ring too much reduces the inductor's SRF because of an increased capacitance to ground. Furthermore, eddy currents are induced in the ring structure. They are not added to figure 3.25 because they are no ground return currents. However, they increase loss and lower the inductance value, thus the ground ring needs to respect a certain minimum distance (about half its diameter) from the spiral.
If loss and inductance created by i_{s1} and i_{s2} are taken into account in simulations depends mainly on the port excitation of the test structures:

HFSS The excitation is done by wave ports. When no common, lumped ground reference is used, the ground conductors of port 1 and port 2 are distinct, and the loss and inductance of the grounding structure is taken into account according to its geometry and material properties.

SONNET Push-pull ports have to be used to achieve a differential excitation independent of the common ground. In this case, loss and inductance due to ground return currents are simulated according to geometry and conductivity. The grounding structure must not touch the sidewalls.

ASITIC A grounding structure can be specified to fix a reference for capacitive substrate coupling, but its resistivity and inductance are not taken into account correctly. A differential excitation is not possible. Using ASITIC thus implies neglecting R_{gnd} and L_{gnd}. Furthermore, eddy currents in the ground ring are neglected, leading to overestimated Q and inductance if the ground ring is too close.

3.4.3.4 *Simulation versus measurement results*

In figure 3.26, both measurements and simulation of the differential inductance L of the test-inductor are shown. While the measured inductance value is reproduced with an accuracy of better than 5 pH by Sonnet and HFSS, ASITIC's inductance values lie slightly higher,

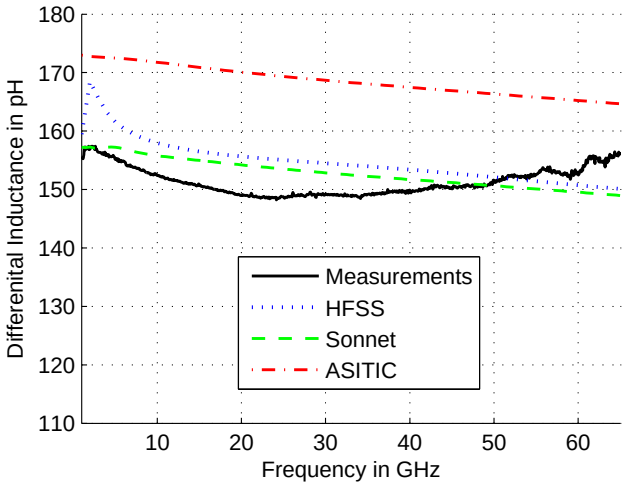


Figure 3.26: L of the test-inductor

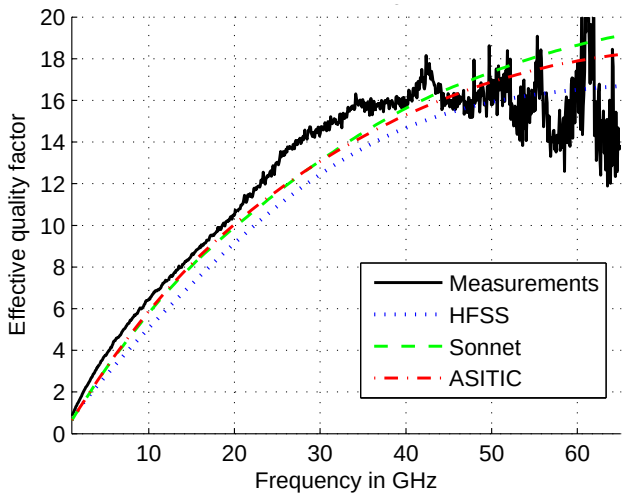


Figure 3.27: Q_{eff} of the test-inductor

probably because L_{gnd} and eddy currents in the ground ring are not taken into account.

The quite small discrepancy in Q_{eff}, which is visible from the plot in figure 3.27 can be explained for one part by measurement tolerances, especially at high frequencies. The difference in Q_{eff} corresponds to S-parameter differences of less than 0.1 dB. On the other hand, the groundplane is considered to be homogeneous as shown in figure 3.21. However, due to design rules, a sophisticated pattern containing 2 metal layers is actually used (cf. section 3.7.2). The equivalent thickness and conductivity of this ground plane is not known very well and can be decisive for accuracy at mm-waves.

3.4.3.5 *Conclusion on inductor simulation*

When designing spiral inductors for mm-wave RFIC, simulation require special attention. The previous section provides insight in two important phenomena at 60 GHz, namely skin/proximity effect and ground return currents. Consequently, guidelines are given for the application of these insights to simulations of inductors in three popular

EM solvers.
In this thesis, Sonnet was the software predominately used for the simulation of passive elements, especially to build the models later used in circuit simulation. This is due to its high accuracy and the ease of use compared to HFSS, which was only used for visualization of fields and currents and occasional verification of Sonnet results. ASITIC was frequently used due to its speed for inductance calculations, but avoided for other passives like interconnect lines where the influence of the ground plane is not small.

3.4.4 *Modeling of Inductors in Circuit Simulations*

To accurately take into account the behavior of inductors in circuit simulations, two possibilities exist. Both make use of the scattering parameters obtained by the simulations described above.
The first possibility is the direct use of the S-parameters via an appropriate data component available in most circuit simulators. However, this method has considerable drawbacks: in frequency domain simulations, extrapolation outside the validity range of the S-parameters quickly becomes unphysical. In time domain simulations, the circuit simulator has to translate the (frequency-domain) scattering parameters into a time domain model. This process is often inaccurate, includes unjustified extrapolations and results in convergence problems.
The second possibility is an equivalent circuit consisting of magnetic and electric storage element as well as loss elements to approximate the electromagnetic phenomena governing the behavior of the inductor in a circuit simulation [183]. A multitude of different equivalent circuit models for inductors exists. A very basic one is the π model, consisting of only the inductor and an associated series resistance plus R-C series connections to ground at the input and output of the circuit. However, this model is only valid over a small bandwidth and does not sufficiently represent the physics of a mm-wave inductor.

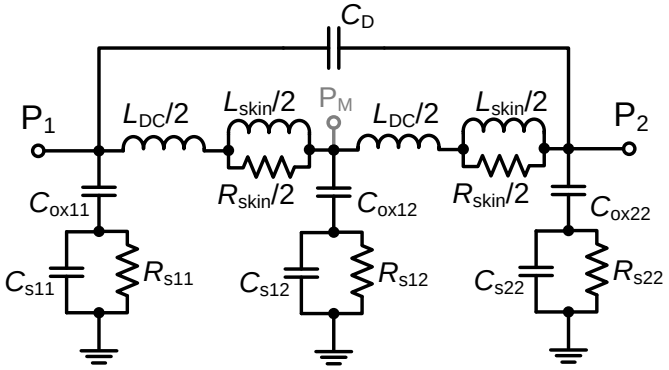


Figure 3.28: 2-π equivalent circuit for spiral inductors

In this thesis, the well known 2-π model with skin effect components as shown in figure 3.28 is employed. T.O. Dickson *et al.* propose to calculate some of its components based on low frequency Y parameters (usually obtained by transformation from scattering parameters) [51]: The low frequency inductance and the associated loss are given by

$$L_{DC} = \frac{\Im\{-y_{12}^{-1}\}}{\omega} \tag{3.10}$$

and

$$R_{DC} = \Re\left\{-y_{12}^{-1}\right\}. \tag{3.11}$$

The oxide capacitances, which represent the capacitive coupling between the spiral and the substrate are given by

$$C_{ox11} = \frac{1}{2\omega\Im\left\{\frac{1}{y_{11}+y_{12}}\right\}}, \tag{3.12}$$

$$C_{ox22} = \frac{1}{2\omega\Im\left\{\frac{1}{y_{22}+y_{21}}\right\}}, \tag{3.13}$$

and

$$C_{ox12} = C_{ox11} + C_{ox22}. \tag{3.14}$$

The substrate is modeled by a capacitance C_{sxx} and a resistance R_{sxx} in parallel, due to the fact that at mm-waves its relaxation time cannot be neglected [51]. The product $R_{sxx}C_{sxx}$ corresponds to the relaxation time

$$\tau = \epsilon_r\epsilon_0\rho_{SI}, \tag{3.15}$$

where the relative permittivity ϵ_r is the one of silicon (i.e. 11.7) and the substrate resistivity is $\rho_{SI} = 0.15\Omega m$ here (cf. section 3.2.1). This relation allows to calculate the capacitors C_{sxx} from the resistor values obtained from Y-parameter simulations by

$$R_{s11} = \frac{2}{\Re\{y_{11}+y_{12}\}}, \tag{3.16}$$

$$R_{s22} = \frac{2}{\Re\{y_{22}+y_{21}\}} \tag{3.17}$$

and

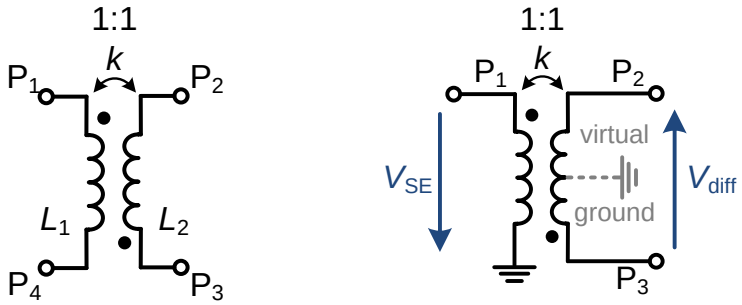
$$R_{s12} = \frac{R_{s11}R_{s22}}{R_{s11}+R_{s22}}. \tag{3.18}$$

The remaining elements model the capacitive coupling from input port to output port (C_D) and the increase of conductor loss with the square root of frequency due to the skin effect (L_{skin} and R_{skin}). These elements are found by fitting the equivalent circuit's scattering parameters to the simulated ones over the whole bandwidth over which the model shall be used (e.g. 1 GHz to 70 GHz). The same procedure also fine-tunes the other element values, while the equations above serve to find the initial values of the optimization.
The $2-\pi$ model parametrized that way provides an excellent broadband agreement with the simulation data for typical on-chip inductors that can be considered lumped elements due to their small size with respect to the wavelength. The fact that the model uses two sections takes into account the distributed nature of the spiral, especially if one of its terminals is connected to ground [51]. In addition to that, it allows the modeling of inductors with a center contact P_M as indicated

in figure 3.28. In balanced circuits, this terminal is located at the odd mode's virtual ground and can be used to inject a bias current.
The advantage of this physical equivalent circuit model is that extrapolations to both DC and towards (and even beyond) the self resonant frequency of the structure yield meaningful results. Furthermore, it can be used in time and frequency domain simulations equally well. Note that an extension of the model towards the representation of spiral transformers is possible. Basically, this extension requires a second equivalent circuit modeling the secondary coil, and appropriate capacitive and inductive coupling between them (see [183] for details).

3.4.5 *On-chip Transformers*

In RFICs that use single-ended and differential building blocks, single-ended-to-differential conversion (and the inverse) is often required. Especially when testing differential circuits at 60 GHz, the externally available 60 GHz signal is usually single-ended, and has to be converted to a differential signal.



(a) ideal transformer (b) transformer used as balun

Figure 3.29: lumped 1:1 transformer with coupling factor k employed as single-ended-to-differential converter

A small-sized lumped element that can accomplish this task is a on-chip transformer [78, 183]. Figure 3.29a gives the annotated symbol of such a device with winding ratio 1:1 and coupling coefficient k. If the input of such a transformer is connected to a single-ended signal as illustrated in figure 3.29b, at the output a differential version of this signal, attenuated if $|k| < 1$ and inverted if the spirals are wound in opposite direction, can be obtained. If a symmetric circuit is attached to this differential output, a virtual ground potential forms in the center of the output inductor. To increase common-mode rejection in the case of an assymetric circuit or a transformer with parasitics, the virtual ground node can be connected to the actual ground node of the circuit. In the following, two different possibilities to realize a transformer-based single-ended-to-differential converter (also called transformer *balun*[1]) are discussed. While in the case of the first, single-coil implementation the strong capacitive coupling between the two windings of the transformer greatly impacts the symmetry of the two outputs [184, 185], the two-coil version is designed such as to benefit equally well from capacitive coupling at both outputs [186]. A performance

[1] As bal-un stands for balanced-unbalanced, this name actually denominates the inverse conversion

comparison of these two balun architectures in the context of mixer design can be found in [185].

3.4.5.1 *Single-coiled transformer*

Like in the case of inductors, mm-wave transformers can be implemented either as planar type on a single metal layer, or as stacked type on multiple metal layers [51]. The latter version exhibits a considerably higher coupling factor due to the fact that the magnetic flux common to both spirals is higher and due to capacitive coupling that adds to the inductive coupling (at least if the windings are used in a inverting configuration [184, 186]). It is thus adopted here.

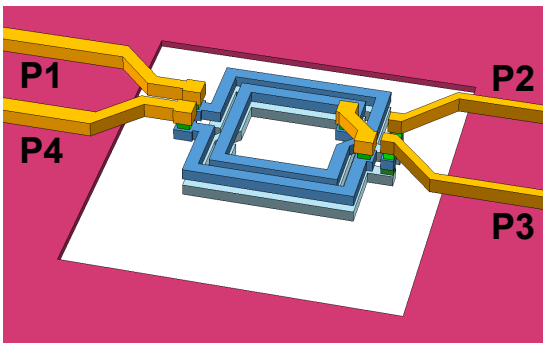


Figure 3.30: Three-dimensional layout of a single-coil stacked transformer, occupying metal layers M6 and M7 for the coils and M5 and alucap for over- and underpasses. The vertical dimensions are three times magnified.

Figure 3.30 shows a stacked transformer implementing the structure of figure 3.29a. The two coupled spirals are realized in the thick copper layers M6 and M7. The conductor dimensions are determined according to the guidelines presented for spiral inductors in sub-section 3.4.2, leading to w=3 µm and s=2 µm. The outer diameter is chosen to be $d = 40$ µm as a compromise between sufficient coupling at the one hand and high self-resonance frequency and Q factor on the other hand.
Figure 3.31 shows a test-structure to characterize the stacked transformer balun in an inverting configuration. According to [184], in this configuration a transmission zero due to the resonance between the coupling capacitance and the leakage inductance does not occur. Thus, capacitive and inductive coupling add up, minimizing conversion loss from port 1 to port 2.

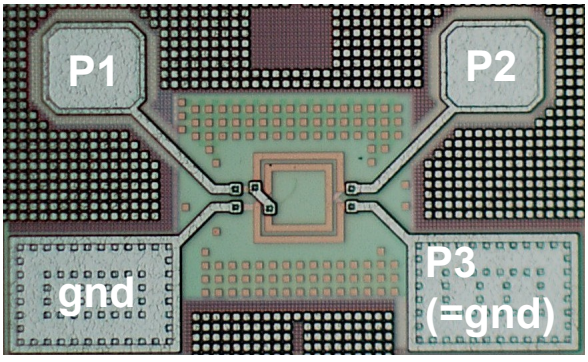


Figure 3.31: Die photo of the single-coil transformer test structure

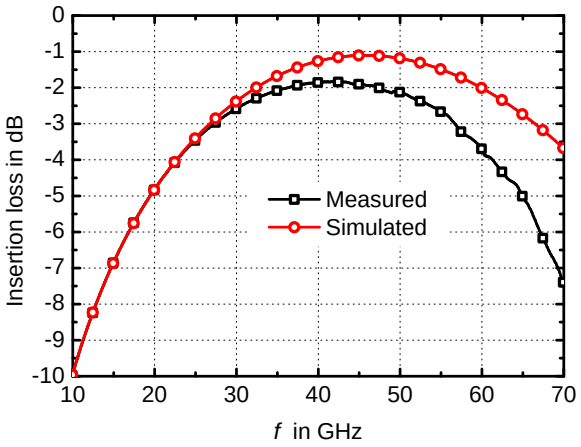


Figure 3.32: Measured versus simulated insertion loss of the one-coil transformer test-structure. The pad capacitance of 32 fF and a series inductance of 24 pH were de-embedded from the measured values at both ports, while the reference plane for the simulation is the limit of the ground ring

Figure 3.32 gives the measured and simulated insertion loss of the stacked transformer. Due to missing de-embedding structures, only an ideal pad capacitance of 32 fF and an ideal series inductance of 24 pH were removed from the measured S-parameters. Their reference plane is at the contact pads. Thus, loss is overestimated in the measured curve. The plotted insertion loss of the test-structure is on the order of the values found in literature for this kind of structure [51]. To move the minimum insertion loss of this test structure to higher frequencies, the transformer's diameter has to be reduced.
However, the measured values of figure 3.32 are not well suited to characterize the transformer's performance if utilized as single-ended-to-differential converter. Rather than characterizing the insertion loss from one grounded port to a second grounded port of the device, the transformer balun has to be considered a three-port. To this end, figure 3.33 gives the insertion losses of the transformer in the balun-configuration earlier considered (cf. figure 3.29b). The ports are either

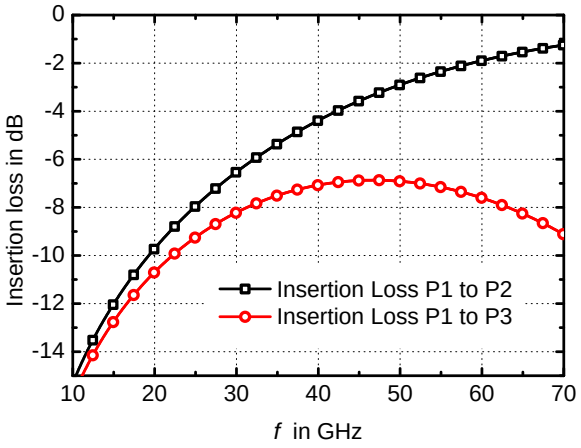
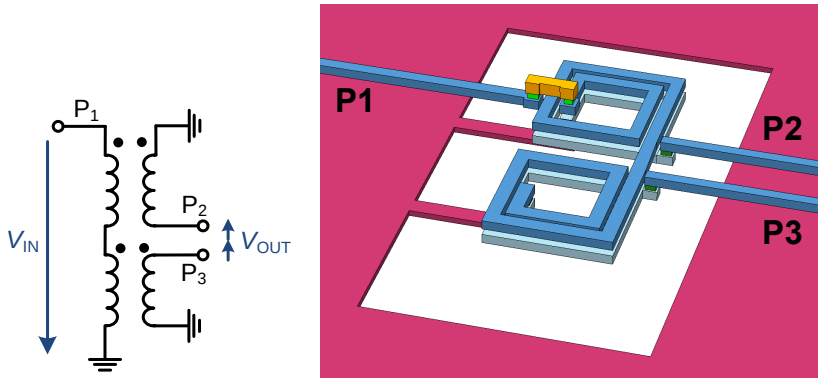


Figure 3.33: Simulated insertion loss from port P1 to ports P2 and P3, P4 at ground potential, P1-P3 terminated in 50 Ω

connected to a 50 Ω source or terminated in 50 Ω.
A huge asymmetry between the power transfer from port 1 to the two output ports can be observed, yielding an amplitude-imbalance of almost 6 dB at 60 GHz. This difference with respect to the ideal behavior can be explained by the large inter-winding capacitance of a real transformer [184, 187]. It results from the very small distance of only about 0.5 µm between the primary and secondary coil. While this proximity is not perturbing in the case of stacked inductors as both coils are connected and at approximately identical potential, in the case of transformers a large difference in potential exists.
To correctly analyze the behavior of a transformer if the inter-winding capacitance becomes important, it should be considered a distributed device. The spiral inductor acts not like a lumped element any more, but like a pair of broadside-coupled lines in spiral form [183]. The next section shows a transformer-based balun that is more appropriate if capacitive coupling becomes relevant, as it performs single-ended to differential conversion both when considered as lumped and distributed element.

3.4.5.2 *Twin-coil transformer balun*

To realize a transformer-based single-ended-to-differential converter with low amplitude and phase imbalance even at mm-waves, the twin-coiled balun illustrated in figure 3.34 is used [188]. It resembles the typical twin-coil transformers found in literature [185], but exhibits a smaller overall size (80 µm ×140 µm up to the ground ring). The improvement in amplitude and phase balance with respect to the single-coil transformer is due to the fact that even in the case of strong capacitive coupling, where this structure has to be considered as a connection of two coupled transmission lines, the outputs theoretically exhibit identical amplitude and 180 ° phase difference.



(a) Schematic of twin-coiled trans-former balun

(b) Three-dimensional layout of a twin-coil stacked transformer, occupying metal layers M6 and M7 for the coils and M5 and alucap for over- and underpasses. The vertical dimensions are three times magnified.

Figure 3.34: Schematic and geometry of twin-coil transformer

To be able to measure the balun's amplitude and phase balance, the three-port test-structure of figure 3.35 was fabricated. It allows the measurement of the insertion loss from port one to each one of the output ports (while terminating the other port in a 50 Ω precision load).

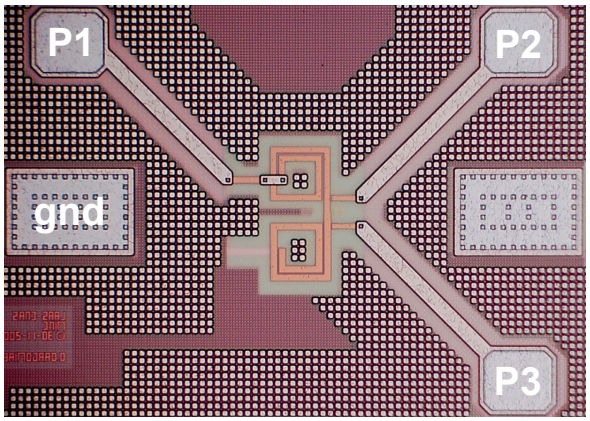


Figure 3.35: Die photo of the two-coil transformer test structure

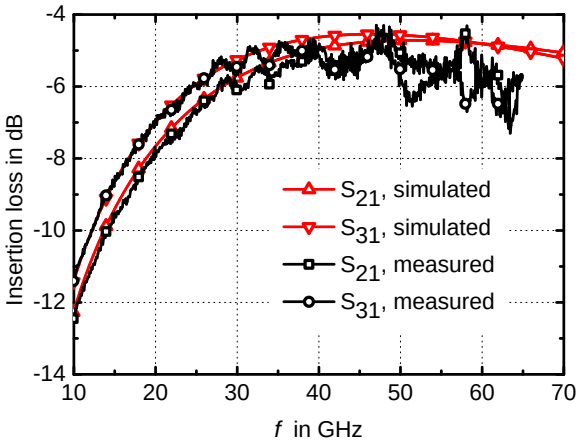


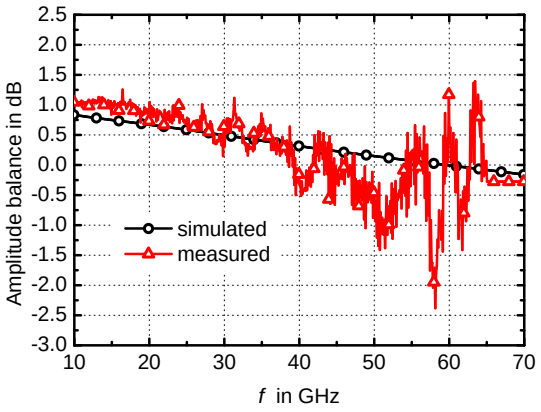
Figure 3.36: Simulated versus measured insertion loss from port P1 to ports P2 and P3, P1-P3 terminated in 50 Ω

The mixed-element de-embedding approach proposed in this thesis and described in section 3.5 is employed to remove the test structure parasitics.

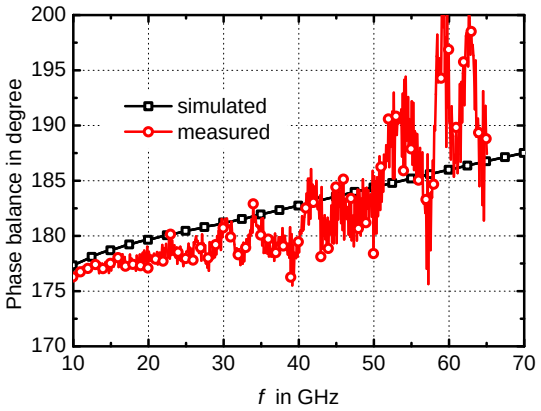
Figure 3.36 compares the measured to the simulated insertion loss from the input port to both of the transformer outputs. Very good agreement is observed, indicating the validity of the conducted simulations and the de-embedding approach. The measured insertion loss at 60 GHz is 5.8 dB to port two and 5.1 dB to port three, thus only 2.8 dB and 2.4 dB below the ideal 3 dB value for power division.

To evaluate the phase and amplitude balance of the two-coil transformer, figure 3.37a plots the difference in insertion loss and figure 3.37b the difference in insertion phase between the two output ports. In both cases, the simulation values are very well confirmed by the measurements. The variations of the measured performance are attributed to noise and measurement tolerance. While the amplitude balance is very well centered around 0 dB, the phase difference at 60 GHz differs by about six degrees from the nominal value of 180 °. This phase offset is attributed to the non-ideal ground contact of the balun.

The two-coil balun presented in this sub-section is thus a better solution as the single-coil transformer balun presented before, if excellent amplitude and phase balance and low combined insertion loss are desired. While in this thesis it is only used to provide a differential



(a) amplitude balance



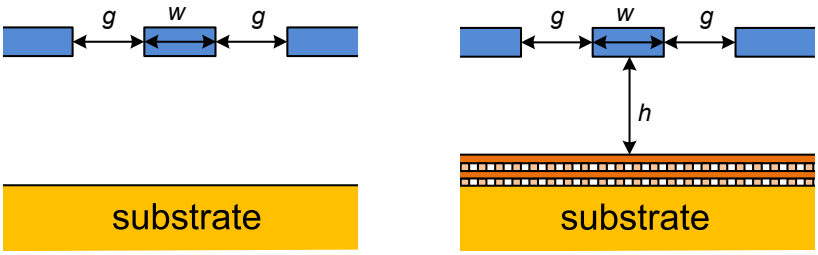
(b) phase balance

Figure 3.37: Measured versus simulated amplitude and phase balance of the twin-coil transformer balun

LO signal from a single-ended external synthesizer for down-mixer measurements, it is perfectly suited for circuit design that requires well-balanced internal single-ended-to-differential conversion.

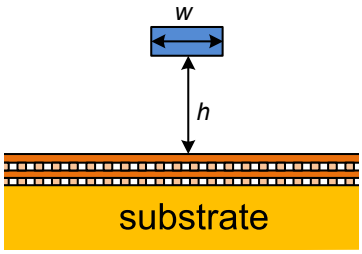
3.4.6 *Transmission Lines*

In this thesis TLs play only a minor role, because spiral inductors are exclusively used for matching purposes due to their much smaller size and their high quality factor. The use of TLs is limited to cases where two components cannot be connected directly due to their size, position in the circuit or geometry, and thus a small length of line has to be inserted.
Figure 3.38 shows the three most common line types used for RFIC design. The coplanar waveguide illustrated in figure 3.38a is limited to applications where either a high-resistivity substrate is available (e.g. in CMOS SOI technologies), or the height over substrate is much larger than the gap between the center conductor and the ground conductors. It is thus not employed in this thesis.
To reduce the influence of the lossy substrate, a grounded coplanar waveguide can be employed [189]. However, as in nanoscale CMOS technologies the distance h between ground plane and signal line is limited, but large gap withs w are necessary to achieve wide conductors



(a) coplanar waveguide

(b) grounded coplanar waveguide

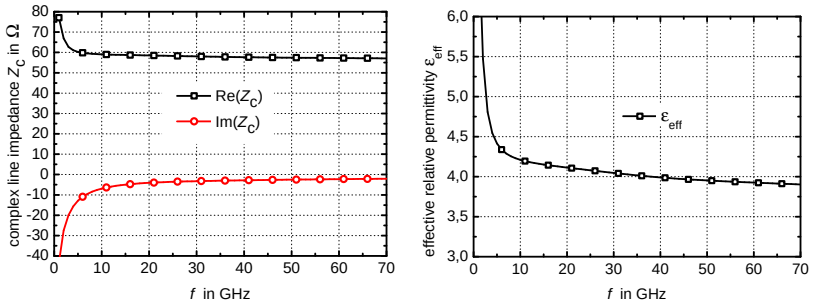


(c) microstrip line

Figure 3.38: Commonly employed line types

and thus low loss [189], the wave propagating on this kind of line is closer to the one of a microstrip line than to the one of a coplanar waveguide.
In this thesis, all transmission lines are considered to be microstrip lines, even though ground conductors are not infinitely far away due to the metal cage employed in all circuits (see subsection 3.7.2). Figure 3.38c shows the principle structure of a microstrip line. As indicated in the sketch, the ground plane that shields the substrate consists of two shunted metal layers (M1 and M2) that are connected to the substrate. This structure is necessary because design rules in nanoscale CMOS technologies prohibit the use of continuous metal planes (refer to subsection 3.7.2 for more details).
A typical microstrip line used in this thesis (e.g. to connect a DUT to the contact pads in a full-custom device test structure) uses the alucap layer to realize the signal conductor. While the conductivity is lower than in the case of the copper layers, the maximum effective height over the ground plane can be achieved this way. The thickness of this layer is only about $t \approx 1\,\mu m$, which is the reason that these kind of lines are also being called *thin film microstrip lines*. The effective height of the line above the M1/M2 ground plane is $h \approx 4\,\mu m$. This small a height requires narrow conductor widths w in order to keep the characteristic impedance reasonably high. Thus, w=6 µm is chosen, yielding the characteristic impedance given in figure 3.39a.
The fact that the magnitude of the real and imaginary part of the characteristic impedance increase considerably for frequencies below about 10 GHz is due to the fact that the series loss per unit length, R', is very high due to the small conductor cross-section $t \times w$. Thus, the high frequency approximation of the characteristic impedance,

$$Z_c = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \approx \sqrt{\frac{L'}{C'}}, \tag{3.19}$$



(a) Characteristic complex line impedance (b) Effective relative permittivity

Figure 3.39: Simulated parameters Z_c and ϵ_{eff} of a microstrip line with $w = 6\,\mu m$, situated in the alucap layer of STMicroelectronics' 65 nm CMOS technology

where L′, C′, R′ and G′ are the general transmission line parameters per unit length, holds only for frequencies above about 10 GHz in the case of the given line dimensions [190].

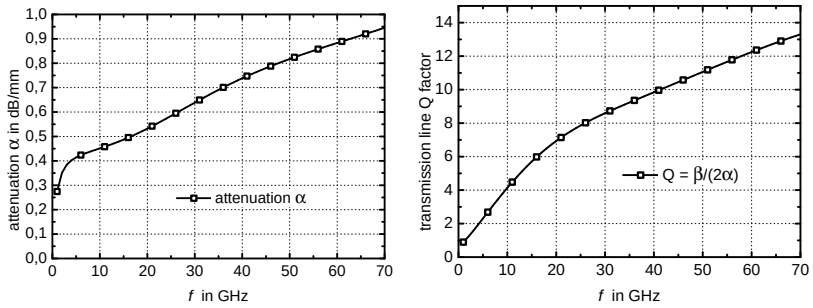
To further quantify the performance obtained by this kind of transmission line, its propagation constant

$$\gamma = \alpha + j\beta = \sqrt{(R' + j\omega L')(G' + j\omega C')} \tag{3.20}$$

is considered. Its imaginary part is related to the free space wavenumber $\beta_0 = 2\pi/\lambda_0$ via the effective permittivity ϵ_{eff} by

$$\beta = \sqrt{\epsilon_{eff}}\beta_0. \tag{3.21}$$

This allows to characterize the propagation on the line by a parameter that is frequency-independent for a TL without dispersion. Figure 3.39b plots the simulated effective permittivity for the line geometry taken as example throughout this section. As in the case of the characteristic impedance, the behavior below about 10 GHz is deteriorated by the high series loss, while around 60 GHz a nearly dispersionless behavior with $\epsilon_{eff} \approx 3.9$ is achieved.
Figure 3.40a plots the attenuation α versus frequency. The small conductor cross section results in very high loss perunit length, which



(a) attenuation factor (b) quality factor

Figure 3.40: Simulated line parameter α and associated Q-factor of a microstrip line with $w = 6\,\mu m$, situated in the alucap layer of the STMicroelectronics 65 nm CMOS technology

increases towards higher frequencies due to the skin effect. At 60 GHz, $\alpha \approx 0.88$ dB/mm, which corresponds to the values typically found in literature in this frequency range in a bulk CMOS technology [189, 190]. This high a value shows that even short TLs should be avoided in 60 GHz RFICs as they unavoidably decrease circuit performance.

To allow a performance comparison with respect to spiral inductors when used for matching, the general Q factor of open- and short circuited transmission lines can be calculated by [189]

$$Q = \frac{\beta}{2\alpha}. \tag{3.22}$$

Figure 3.40b plots the simulated Q factor of the considered microstrip line. The achieved value of 12.3 at 60 GHz lies well below the quality factor of the inductors realized in the framework of this thesis. Even though TLs that have been optimized for high Q can be found in literature yielding quality factors equivalent to these of spiral inductors [189], their circuit size is much larger. Thus, to achieve low die area and low cost, the use of spiral inductors as matching elements is mandatory in a bulk CMOS technology. A remaining advantage of using TLs is that once the parameters of a specific line type are determined, it can be accurately scaled without further tedious electromagnetic simulations.

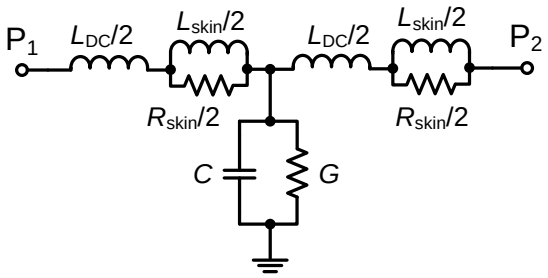


Figure 3.41: Equivalent circuit of a piece of transmission line

Most of the transmission lines used in the circuits of this thesis have almost negligible influence on the circuit's area and behavior. To account for their albeit small effect in simulations, the equivalent circuit given in figure 3.41 is employed to model TLs that have a length of more then some microns. At least every twentieth part of a wavelength one element of this equivalent circuit should be employed to catch the distributed nature of the line. Similar to the equivalent circuit for spiral inductors, which is described in section 3.4.4, the fact that the conductor loss is increasing with frequency due to skin effect is modeled by L_{skin} and R_{skin}.

3.5 DE-EMBEDDING OF FULL-CUSTOM DEVICE-MEASUREMENTS

The previous sections presented different full-custom mm-wave devices that are used for 60 GHz circuit design in this thesis. The 65 nm CMOS DK does not include models to represent their behavior in circuit simulations. In the case of passive devices like inductors, transformers and transmission lines, the accuracy of the EM simulations used to build equivalent circuit models needs to be validated by device measurements (see inductor design flow in figure 3.19). Measurements are also the only possibility available in the context of this thesis to accurately determine the behavior of the full-custom AMOS varactors described in section 3.3.
The discussion in the following concentrates on the measurements of spiral inductors, as they are most challenging due to the high Q factors achieved. However, as the proposed techniques do not depend on the DUT, they are directly applicable to the characterization of any other device, namely varactors, transmission lines and transformers.

In order to measure the performance of these devices over a very broad frequency range (typically from around DC up to 67 GHz), special test structures are used. They consist of the DUT, which is surrounded by a structure allowing to properly place on-wafer probes (cf. section 3.5.1.1) while respecting minimum distances recommended by the probe manufacturer.
The S-parameters of the DUT are obtained by measurements using a Vector Network Analyzer (VNA). They are corrected by a two-step calibration procedure:

- The first calibration is done by the VNA, and uses an Impedance Standard Substrate (ISS) with high precision calibration standards, like **S**hort, **O**pen, **L**ine and **T**hru in the case of the SOLT calibration. By this first calibration, the reference plane is shifted to the probe tips. However, the fact that the calibration is done on a substrate with gold metalization, while the pads on the CMOS chip are usually made of aluminum, has to be taken into account [191].
- The second step of the correction consists in moving the reference plane up to the DUT terminals or rather removing the parasitics of the test structure and accounting for the difference in contact resistance.

Note that the accuracy requirements are extremely high, because the typical inductor values at 60 GHz lie between 50 pH and 350 pH and the quality factors on low resistivity silicon vary from around 15 to 20. Hence, resistance values around one Ohm have to be determined precisely. If measurements and de-embedding are not done attentively, the tolerances (especially due to contact resistance repeatability) can exceed the series resistance value, yielding unphysical, even negative values.

This section reviews suitable on-chip calibration and de-embedding techniques. It proposes a technique that uses distributed *and* lumped elements to model the error two-ports. To allow the identification of the elements to de-embbed, a typical mm-wave test-structure, which is used to characterize the full-custom devices designed in this thesis, is

presented and analyzed in detail.
The results obtained by this novel de-embedding approach using test-inductors are compared to results of the other discussed methods and to simulation results. The obtained agreement proves the suitability of the proposed method for characterization of mm-wave inductors and other devices.

3.5.1 *A Typical Test-structure for CMOS Inductors*

3.5.1.1 *Test structure geometry*

The geometry of a typical test structure for inductor measurements is given in figure 3.42. It is symmetrical around the DUT in order to facilitate layout and de-embedding. Each side contains one signal pad and two ground pads. While the signal pads are implemented only in the topmost metal layer (alucap) shunted to M7 and float on the inter-metal dielectric, the ground pads consist of a stack of via-connected metal polygons that descend down to the lowest two metal layers (M1 and M2). They serve as ground plane and are well connected to the conductive substrate.

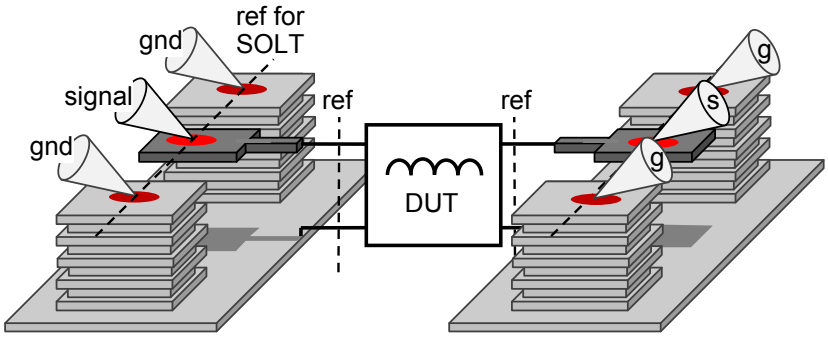


Figure 3.42: Perspective view of the test structure (with probes sitting on ground and signal pads) and illustration of the contact area

The terminals of the DUT are connected to the signal pads, while the DUT's grounding structure is joined to the test structure's ground plane all along the reference plane.
The tips on the on-wafer probes are also indicated in figure 3.42. The contact, whose resistance is particularly important for Q-accurate measurements (cf. subsection 3.5.1.3), is illustrated by the shaded area around the tip. Note the two reference planes in figure 3.42: The first one (at the probe tips) results from the calibration on ISS, the second one (at the DUT terminals) is obtained after applying the techniques detailed in this section.

3.5.1.2 *Test-structure parasitics*

The test-structure introduced in the previous subsection adds the following parasitics to the DUT:

- A pad capacitance between the signal pad and the ground, together with some (minor) associated dielectric loss
- The parasitics of the connection between signal pad and inductor. These parasitics include series inductance and loss as well as capacitance to ground

- The contact inductance, which depends on the distance between probe contact area and the boundary of the pad on the DUT side. It is negligible if this distance is very small.
- A contact resistance originating from the non-ideal contact between probe tip and aluminum pad

3.5.1.3 *Contact resistance on aluminum pads*

The parasitic contact resistance $R_{contact}$ plays a particular role for two reasons: First, $R_{contact}$ depends on the pad material, which is usually *gold* for the ISS, but *aluminum* for the CMOS chip [191]. Thus after having done the first calibration (here: SOLT), the difference

$$R_{contact,diff} = R_{contact,Al} - R_{contact,Au} \tag{3.23}$$

still has to be taken into consideration for the second de-embedding step.

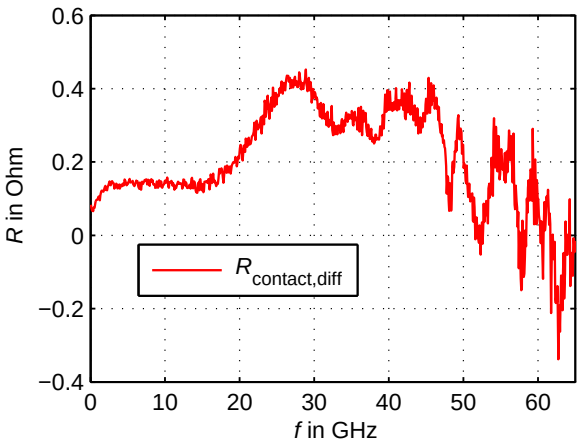


Figure 3.43: Difference between contact resistance on aluminum and on gold obtained from the measurement of microstrip line test-structures

Figure 3.43 shows a typical curve of $R_{contact,diff}$. Note that it is possible for $R_{contact,diff}$ to become negative (here at higher frequencies), due to the fact that for a particular measurement point the aluminum contact is better than the gold contact.
The second point which proves Q-accurate inductor measurements particularly critical is the repeatability of the contact resistance [191]. To get a repeatable contact, a well defined, large force has to be applied to the on-wafer probes (unfortunately wearing them off rapidly), and the position of the probe tips has to be defined as accurately as possible. For the particular probes used for the measurements presented in this thesis[1], a skate reaching from one rim of the signal pad to the other one, i.e. around 40 µm, ensures a good repeatability. To affirm a proper contact, multiple measurements, between each of which the probes are lifted, are done for each structure.
Note that the smaller the inductor value and the higher its Q factor is, the more important is the contact repeatability. Unrealistic quality factors, approaching very high values, result by mistake, if the contact during DUT measurement is better than it was during measurement of the calibration patterns.

[1] GGB Inc.'s Picoprobes made of Beryllium-Copper, pitch 100 µm

3.5.2 *Three methods for calibration and de-embedding*

Three different methods to remove the test structure parasitics in the second calibration step are discussed in this subsection. Two of them make use of a technique to accurately obtain the transmission line parameters (characteristic impedance Z_0 and complex propagation constant γ) of a pair of microstrip lines, as proposed by A. M. Mangan *et al.* [190]. Mangan's technique requires two microstrip line test structures of different length, and yields as by-product also the pad admittance of the test structure. The third method is based on lumped elements only and hence does not require the extraction of transmission line parameters.

3.5.2.1 *TRL-Calibration*

If no further assumptions about the test structure parasitics are made, two unknown error two-ports surround the device as illustrated in figure 3.44. The classical TRL calibration [192] can be used in this case. It requires three calibration standards: A **T**hru connecting both reference planes, a **R**eflect (e.g. short circuit) at each reference plane that provides no transmission, and a **L**ine between them.

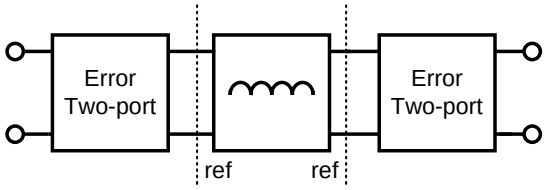


Figure 3.44: Error two-ports during TRL calibration are considered to be black boxes, no assumptions are made concerning the inside

The line standard is the critical element, because it has to provide the reference impedance for the correction. As the characteristic impedance of a Thin Film Microstrip (TFMS) line in a CMOS technology cannot be precisely set to 50 Ω between near DC and 67 GHz, the TRL-corrected results have a generally frequency-dependent, complex impedance $Z_0(f)$. To obtain $Z_0(f)$ from line measurements, the prior mentioned technique [190] is used. As one of the line standards for this extraction the thru can be used. Based on this extraction, the TRL results can be renormalized to 50 Ω.
In practice, the TRL calibration exhibits drawbacks if the used standards are small: Firstly, the line standard should have a certain electrical length (usually $> 20°$). Secondly, and more important in the present case, the thru standard should have negligible coupling between its input ports (i.e. the transmission from one port to the other one should take place exclusively by a quasi TEM-wave on the microstrip line). If this is not the case, the effective port impedances for thru standard and line standard are different (even if their geometry is the same at the reference plane), and the calibration is not valid. The described behavior is observed in the present case at higher frequencies, because the pads of the thru test structure are very close.

3.5.2.2 *Lumped-element de-embedding*

Lumped element de-embeding (e.g. [193]) assumes that the test structure parasitics can be approximated by a parallel admittance and a series impedance as illustrated in figure 3.45. The series element can be obtained by half of the series impedance of a through, while the parallel admittance can be obtained by the reflection measurement of an open standard.

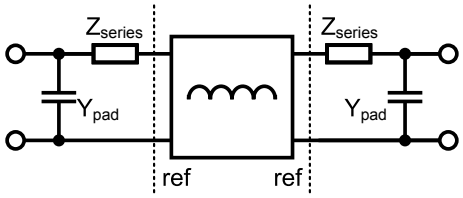


Figure 3.45: Lumped element de-embedding assumes a parallel admittance and a series impedance as error two-port

The drawback of this technique is that the lumped element assumption becomes invalid at mm-waves, where the series element is accompanied by distributed capacitances. Furthermore, the contact resistance is not de-embedded at the correct location. The consequences of these simplifications can be observed from the measurement results (cf. section 3.5.3).

3.5.2.3 *Newly proposed mixed-element de-embedding*

In order to get a more accurate correction, the parasitics illustrated in the equivalent circuit in figure 3.46 are proposed to be de-embedded. It resembles the one suggested in [194], however, a contact impedance $Z_{contact}$ is added. To obtain all the required element values, only two line standards of different lengths are required. First, the difference of their series impedances is used to estimate the contact resistance $R_{contact,diff}$. Then, the two line measurements are corrected with respect to these contact impedances using ABCD - parameters.

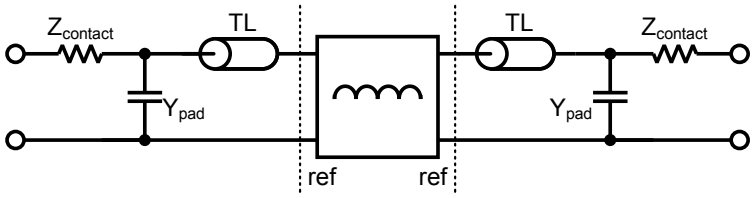


Figure 3.46: Proposed equivalent circuit model for the error two ports surrounding the inductor under test

The line parameters of these $R_{contact,diff}$-free microstrip lines are then extracted by the prior mentioned technique [190]. The ABCD matrix of the test structure's line element (the line lengths are known from layout) is subsequently found. A multiplication of the inverse matrix de-embeds the line segments. The pad admittances result also from the extraction according to [190], and can be de-embedded using Y-parameters.
Compared to the TRL-calibration and the lumped de-embedding technique, the proposed mixed de-embedding technique avoids the use of a thru standard, whose drawback is unwanted coupling between its input ports. In addition, two standards are sufficient to characterize all

the parasitics to de-embed. The distributed nature of the test structure is well taken into account, while at the same time the lumped contact impedance is correctly removed.

3.5.3 *Measurement Results*

To assess the performance of the presented de-embedding and calibration techniques, they are compared to each other and to simulation results. Identical S-parameters, obtained by VNA measurements after applying the first SOLT calibration, are the basis for all of the presented results.
The measured test inductor is shown in figure 3.47. The inductor under test has a diameter of 30 µm, a conductor width of 3 µm and is implemented in the top-most copper metal layer (metal 7). The structure corresponds to the one used as an example throughout the previous section.
The importance of de-embedding the pad capacitance is illustrated in figure 3.48. The return loss measured with and without de-embedding is very different, however, a difference between the presented de-embedding techniques is not observable when considering return loss.

The influence of the correction techniques on S_{21} is shown in figure 3.49. The two techniques that are expected to correct the series parasitics more accurately, i.e. TRL and mixed-element de-embedding, show results very close to each other (note the scale on the abscissa, indicating measurements close to achievable tolerances).
In order to asses the influence of the de-embedding techniques on the differential inductance

$$L_{diff} = \frac{\Im\{y_{21}\}}{2\pi f} \tag{3.24}$$

and the effective quality factor

$$Q_{eff} = \frac{\Im\{y_{11}\}}{\Re\{y_{11}\}} \tag{3.25}$$

(where y_{ij} are the Y-parameters), these quantities are compared to results obtained from HFSS simulations of the DUT in figures 3.50

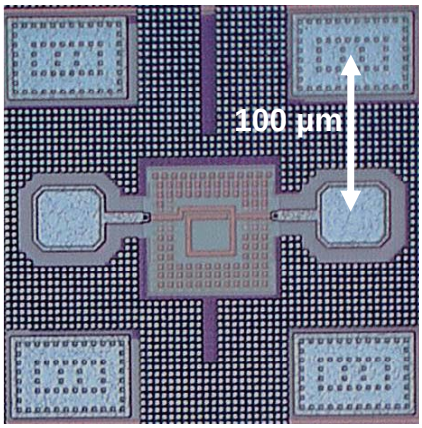


Figure 3.47: Die photo of the measured test structure containing two error two-ports and the IUT

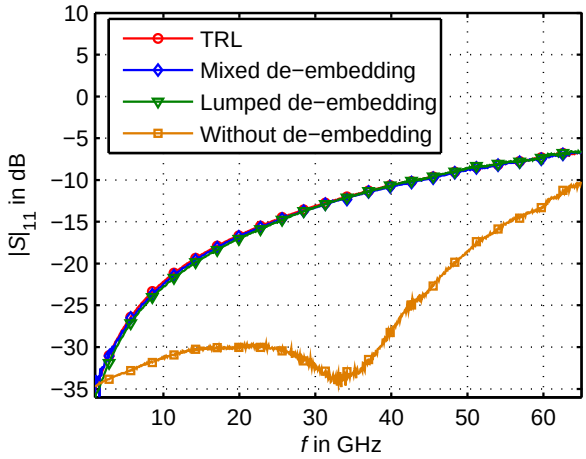


Figure 3.48: Reflection coefficient at port one of the test inductor, with and without de-embedding of the test structure

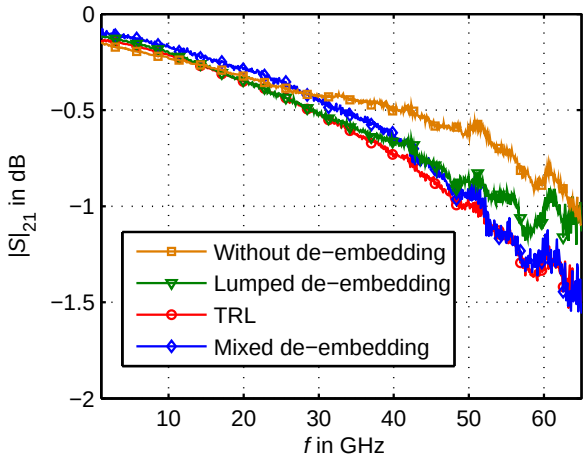


Figure 3.49: Transmission coefficient of the test inductor, with and without de-embedding of the test structure parasitics

and 3.51. The (very small) discrepancy of L_{diff} between the different measurement and simulation results can be explained by the use of a thru standard for TRL and lumped de-embedding: The series inductance between the ports of the thru is probably underestimated due to coupling effects.
Up to 40 GHz, the Q factor obtained using the discussed de-embedding techniques agrees exactly with simulations. Only the TRL method suffers somehow from the only 200 µm long line standard.
At higher frequencies, the VNA's measurement accuracy is the limiting factor, shown by the noisy, strong variation of the measured curve. The degree of accuracy already obtained becomes clear when noting that a change in series resistance of one Ohm changes the Q factor from 12 to 18.
Nevertheless, TRL and mixed de-embedding show a good proximity to the simulation results, while the mixed technique is slightly closer to simulations. Lumped-element de-embedding suffers from aforementioned limitations.

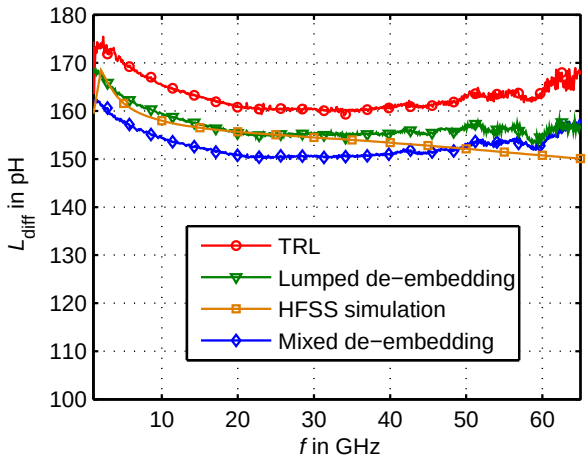


Figure 3.50: Comparison of differential inductance obtained using different de-embedding techniques and HFSS simulation

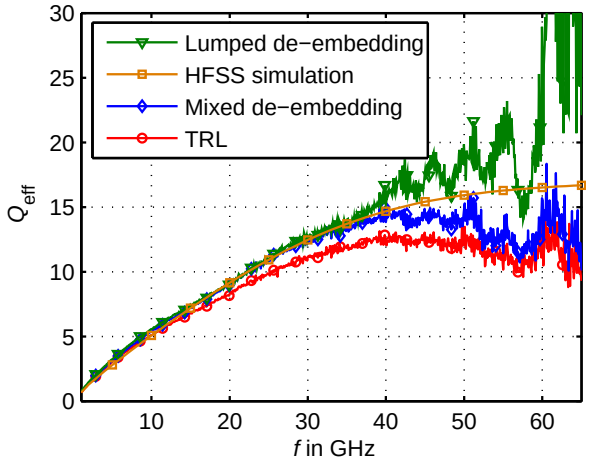


Figure 3.51: Comparison of effective quality factor from different de-embedding techniques and HFSS simulations

3.5.4 *Conclusion on de-embedding*

Techniques to remove the parasitics of typical test structures for RFIC spiral inductor measurements have been discussed and evaluated. A newly proposed mixed-element de-embedding technique that removes the contact resistance, the pad capacitance and a transmission line segment from the DUT yields better results than the classical lumped de-embedding technique. It requires only two transmission line test structures to obtain all parasitic elements. The novel approach is published in [195].
An important consequence of the results presented in this section is the validation of the EM simulations' accuracy. The confidence gained in the manner to set up and run EM simulations proposed in subsection 3.4.3 allows the design of 60 GHz circuits based on passive device models parametrized by these simulations, without further use of measurements.

3.6 DESIGN TECHNIQUES

This section presents RFIC design techniques that are used in most of the circuits of thesis. Namely, the biasing of the transistors, the design of 60 GHz matching networks using lumped elements and the use of inductive source degeneration are discussed in the following.

3.6.1 *Biasing of the MOS Transistors*

The small and large signal behavior of transistors depends on their bias point, i.e. the DC voltages and currents on which the AC signals are superimposed. The bias point of the MOSFET is given by its drain-source voltage V_{DS} and its drain current I_D. The latter depends both on the gate-source voltage V_{GS} and also on V_{DS} (even in saturation, as illustrated in section 3.2.2.3). This bias point is chosen to maximize the performance of the transistor.
Figure 3.4 (subsection 3.2.2, page 53) underlines that maximum performance is obtained for maximum V_{DS}. However, the choice of V_{DS} is quite restricted by the transistor's breakdown voltage (in the case of GP transistors the supply voltage recommended by the foundry is 1 V). The choice of I_D and V_{GS} depends on the property of the transistor that shall be optimized. Figure 3.3 on page 53 indicates that there exist *characteristic current densities* that maximize a given figure of merit (e.g. the peak of the f_T) for *different* types of transistors and under various environmental conditions. At the same time, the V_{GS} that is necessary to achieve these characteristic current densities can vary a lot. Thus, biasing at a constant current, rather than at a constant V_{GS}, seems appropriate. This is shown by T.O. Dickson *et al.* in [152] and detailed in the following.

3.6.1.1 *Constant Current-Density Biasing*

There exists evidence that the characteristic current densities at which the peak f_T, peak f_{max} and minimum noise figure is achieved are largely unchanged over technology nodes and foundries [152]. According to [152, 155], this is the result of mobility degradation due to the vertical field in the channel and by constant field scaling rules issued by the International Technology Roadmap for Semiconductors (ITRS).
In addition to their independence of technology, the characteristic current densities do not change with threshold voltage, temperature and gate length [156]. Even though the figures of merit (like f_T and f_{max}, cf. section 3.2.2.1 for their definition) degrade with temperature, their optimum value is always found at the same current density.
Consequently, and in agreement with the suggestions in [152, 155, 156], the circuits in this thesis are biased to achieve a certain optimum current, rather than a constant gate-source voltage, which can change a lot at a optimum bias point.
Table 3.2 gives the current densities that should be used to maximize the indicated properties. Due to the proximity of J_{opt} to J_{pfmax}, almost maximum power gain can be achieved even when biasing for minimum noise [156]. Furthermore, in addition to bias points optimizing the small signal behavior, a bias current density to achieve maximum linearity is also given: T. Yao *et al.* suggest to minimize the variation in f_{max}

property	characteristic current density [mA/µm]
peak f_T	$J_{pfT} = 0.3 - 0.35$
peak f_{max}	$J_{pfmax} = 0.2$
minimum noise figure	$J_{opt} = 0.15$
maximum linearity	$J_{lin} = 0.3$

Table 3.2: Characteristic current densities for optimum biasing according to [152, 156]

in order to achieve the highest 1 dB compression point for a given transistor width and drain-source voltage.

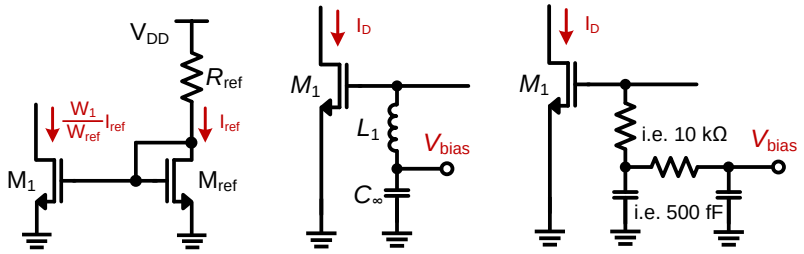
3.6.1.2 *Biasing circuitry*

According to the considerations in the previous subsection, the bias point of a transistor is fixed to the characteristic current density that maximize the performance being the most important for the component the transistor is employed in (i.e. J_{opt} in a LNA, etc.). In integrated circuits that are commercialized, reference current sources, e.g. based on bandgap references, provide these characteristic current densities with high precision [133, 154, 196]. besides the circuit's power supply, external bias voltages are not required. High compliance current mirrors are used to accurately transfer these reference currents to the transistors used in each circuit block [197].
In this thesis, constant current biasing is realized differently:

- Either, in non-critical parts of the circuit, a simple current mirror using a resistor to create the reference current from the supply voltage is used. Its principle is shown in figure 3.52a. However, because even in saturation the drain current is a strong function of the drain-source voltage due to the short-channel MOSFET's output characteristic (illustrated in figure 3.6), the reference current is only accurately mirrored if the transistor's drain potentials are the same. Tolerances in V_{DD} and the resistance value R_{ref} induce further errors.

- Or, to allow an influence on the current densities of critical circuits during testing, the gate of the transistor whose drain current shall be adjusted is connected to a bias pad. Rather then fixing the voltage at this pad to a certain V_{GS}, it is used to adjust the drain current density in order to achieve optimum biasing. If possible, the bias voltage is fed to the gate at an AC ground via a matching inductor (cf. figure 3.52b). Alternatively (or in addition to the matching inductor), a high-impedance bias filter like the one given in figure 3.52c is used to decouple the 60 GHz signal path from the biasing network. Furthermore, the capacitance from the bias voltage node to ground is maximized as described in section 3.7.2.

Note that in this second case a protection circuit against Electrostatic Discharge (ESD) might become necessary, because the gate oxide breakdown voltage at which the transistor is irreversibly destroyed is rather low. It is quite challenging to ensure that this voltage is not exceeded even in a laboratory environment.



(a) Current mirror with resistor to fix reference current

(b) Bias voltage applied via AC ground

(c) Bias voltage applied via decoupling filter

Figure 3.52: Biasing by externally applied voltage

3.6.2 *Design of Matching Networks*

In the design of 60 GHz RFICs, impedance matching between devices, amplifier stages, circuit components and in- or outputs is essential to achieve optimum power transfer, maximum output power or minimum noise figure. Thus, the 60 GHz interfaces encountered in this thesis are always impedance-matched. The matching networks usually employ MOM capacitors as capacitive matching element and spiral inductors as inductive matching element.
In the following, the general design procedure for a matching network is outlined. As in practice the matching depends much on the involved circuits, the outlined steps remain inevitably very general.

In a first step, the two impedances that should be matched to each other need to be determined. This step depends on the involved devices:

- If one impedance is the input or output of a transistor, this transistor has to be:
  1. sized according to the desired linearity or optimum noise impedance
  2. extracted (i.e. an extraction of the parasitics that are not included in the BSIM4 model and depend on the metal layout has to be done to ensure accurate matching)
  3. biased at the desired current density and bias voltages (employing ideal capacitors C_∞ and inductors L_∞ that have negligible effect at 60 GHz but allow the application of bias currents and voltages)
  4. source-degenerated (if applicable, employing the accurate model of the degeneration inductor)
  5. cascoded (if applicable, employing the accurate model of a potential middle inductor [156])
- If the match shall be done towards an off-chip input or output, the impedance of this port (usually 50 Ω) appears parallel to the pad capacitance (usually 26 fF, cf. subsection 3.7.3)
- If a balanced port shall be matched, the odd-mode impedance is used for matching in this thesis. The even-mode impedance shall remain mismatched to improve common-mode rejection.

- If a device's impedance (in the case of a two-port like a transformer, transistor or amplifier with low reverse isolation) is influenced by the impedance attached at its second port, the available gain or power gain circles give the impedance that must be used for conjugate matching
- If a noise match is desired, the optimum source impedance gives the impedance that must be used for matching
- If a large signal match is desired, a load-pull simulation yields the impedance that must be used for matching
- If a simple, small signal power match is desired, the conjugate complex input impedance is used for matching

Note that the above list is not exhaustive and various combinations, e.g. a simultaneous noise-power match with inductive degeneration, might become necessary.

In a second step, and once the two impedances that should be matched to each other have been determined, the Smith chart is used to determine the ideal, lumped components that realize the match at a given center frequency. To achieve a broadband match, the paths on the Smith chart need to stay close to the horizontal center line, as this ensures a low loaded quality factor. Alternatively, in a multistage design, the center frequencies of each interstage match might be shifted with respect to each other to increase bandwidth.

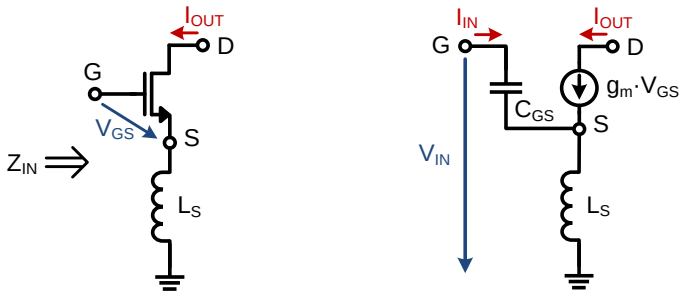
In a third step, the ideal matching elements are replaced by the more realistic equivalent circuits or design kit models. This also implies that if a RF ground node is realized by using huge capacitors that shunt a fixed DC potential to ground, the values of these capacitors need to be taken into account. The third step also has to include a verification whether the topology used in circuit simulation can be realized in layout, or if parasitic inductances due to additional connections need to be taken into account.

In a fourth step, circuit simulations are used to iteratively adjust the values of the lumped components (preferably the capacitors, whose dimensions depend less on their values) up to a point where the ideal match is achieved.

3.6.3 *Inductive Source-degeneration*

A very versatile design technique, which is particularly well suited for mm-wave CMOS design due to the resulting device sizes, is inductive source degeneration [133]. It is illustrated in figure 3.53.
The effect of inductive source degeneration on the input impedance Z_{IN} of a transistor can be calculated in a simplified way using the schematic shown in figure 3.53b. As the input voltage can be written as a function of the input current according to

$$V_{IN} = j\omega L_S \left(1 + g_m \frac{1}{j\omega C_{GS}}\right) I_{IN} + \frac{1}{j\omega C_{GS}} I_{IN}, \tag{3.26}$$



(a) MOSFET with inductive source degeneration (b) simplified small signal equivalent circuit

Figure 3.53: Inductive source generation

the input impedance is

$$Z_{IN} = j\omega L_S - j\frac{1}{\omega C_{GS}} + \frac{g_m}{C_{GS}} L_S. \tag{3.27}$$

This impedance has a frequency-independent, non-zero real part originating from the degeneration inductor. In the case of the ideal equivalent circuit of figure 3.53b, this real part can be expressed as a function of the intrinsic cut-off frequency f_c that has been defined in equation (3.2) of subsection 3.2.2.4. Hence,

$$\Re\{Z_{IN}\} = \frac{g_m}{C_{GS}} L_S = 2\pi f_c L_S = \omega_c L_S. \tag{3.28}$$

In the more realistic case of a transistor including all relevant parasitic (or even a cascode stage), the degeneration-inductor's effect on the input impedance can be calculated using the cut-off frequency ω_T of this device instead of ω_c, resulting in

$$\Re\{Z_{IN}\} \approx 2\pi f_T L_S = \omega_T L_S. \tag{3.29}$$

Note that this value has to be complemented by the parasitic gate and source resistances.

In addition to the modification of the input impedance, source degeneration also impacts the transconductance. For the simplified circuit in figure 3.53b, the degenerated small signal transconductance is

$$g_{m,deg} = \frac{I_{OUT}}{V_{IN}} = \frac{g_m}{1 - \omega^2 L_S C_{GS} + j\omega L_S g_m}. \tag{3.30}$$

This expression reduces to the transistor's transconductance g_m both at zero frequency and at zero source inductance. At higher frequencies, the reduction in transconductance with respect to the non-degenerated value can be set by accordingly choosing the inductor L_S.

Note that the real part of the input impedance and the reduction of the transconductance are realized without using resistive elements. Thus, at least if neglecting the loss associated with the degeneration inductor, no degradation with respect to noise performance, voltage headroom and power consumption result from this technique.

Inductive source degeneration can serve different purposes:

1. **Simultaneous noise and power matching.** Classical two-port noise theory gives the actual noise figure of a two-port at a given bias-point as a function of the minimum noise figure NF_{min}, the noise resistance R_n, the optimum source admittance $Y_{S,opt}$ and the actual source admittance $Y_S = G_S + jB_S$ according to [133, 155]

$$NF = NF_{min} + \frac{R_n}{G_S} \left| Y_S - Y_{S,opt} \right|^2 . \tag{3.31}$$

   Thus, the source impedance seen by the transistor input must equal the optimum noise admittance $Y_{S,opt}$ to minimize the NF. However, in general this impedance does not coincide with the impedance that is required for a complex conjugate match that optimizes power transfer: while the imaginary part of the complex conjugate input admittance in CMOS technology usually is fairly close to $B_{S,opt}$, this is not the case for its real part [156].
   Inductive source degeneration provides a means to nevertheless achieve a simultaneous noise and power match [198]: because $Y_{S,opt}$ is not modified when adding an ideal degeneration inductor L_S to the transistor, a two-step matching approach can be employed: first, the optimum noise conductance $G_{S,opt}$, which is proportional to transistor width [155, 198], is set to the desired source conductance G_S by sizing the transistor accordingly. Second, the value of the degeneration inductor L_S is chosen according to (3.29) to yield a real part of the input impedance that equals the real part of the source impedance. Hence, sizing achieves the noise match, while degeneration realizes the power match.
   Once this equivalence of the real parts is achieved, the matching of the imaginary parts can be realized for example by adding a series inductor of appropriate size to the input.
   T. Yao *et al.* give a detailed algorithm that applies this technique to the design of 60 GHz LNAs [156]. An application to other building blocks, e.g. the down-conversion mixer as in this thesis, is also feasible.

2. **Feedback linearization.** Adding a degeneration inductor is a means to add frequency-dependent negative feedback to an amplifier circuit. This desensitizes the amplifier, and thus reduces the impact of the open-loop nonlinearity on the closed-loop circuit, while at the same time reducing the amplifier's gain [133].

3. **Stabilization.** As inductive source degeneration increases the real part of a MOSFET's input impedance and reduces gain in a certain frequency range, it can also be used for device stabilization. However, because the influence of the degeneration inductor is increasing with frequency, its effect is usually not sufficient to stabilize a device at low frequencies, where stability issues are more likely to occur. An alternative solution, however at the expense of noise performance, power dissipation and voltage headroom, is stabilization employing resistive source degeneration.

In most of the designs presented in this thesis, inductive degeneration is employed to achieve one or more of the above-mentioned goals. Note that the analytical calculations need to be complemented by more accurate simulations to take into account the parasitic elements that have a major impact at 60 GHz.

3.7 LAYOUT TECHNIQUES

This section illustrates layout issues that arise - and associated techniques that are beneficial - when designing mm-wave circuits in a nanoscale CMOS technology.

3.7.1 *Dummy Fill*

The expression *dummy fill* refers to the process of inserting additional metal (so-called *dummies* or *tiles*) to the final layout of a circuit to respect design rules that require a certain metal density in each layout layer. These rules, specifying minimum and maximum densities (mostly centered around 50%) for both metal and active layers in nanoscale CMOS technologies, originate from extremely tight process control requirements. Critical are in particular STI etch and polish, the definition of the channel length, and inter-level dielectric planarization.
Usually, once the circuit layout is completed, dummy exclusion markers are added to mark regions where additional metal would interfere with the circuit behavior. In 60 GHz circuits, these regions are especially the vicinity of spiral inductors and transmission lines. An automatic dummy insertion process then adds small pieces of additional metal at places where this is allowed, up to the point where all density rules are satisfied.

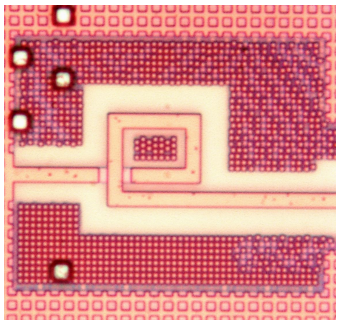


Figure 3.54: Microphotograph of inductor surrounded by dense dummy metal

However, especially if several passive mm-wave devices are located close together, dummy insertion has to be allowed in close proximity to these devices. Otherwise, density rules are not respected. An example of an inductor closely surrounded by dummy metal is shown in figure 3.54. These dummies have an influence on the device's behavior by adding additional parasitic capacitance (approximate simulations show a decrease of effective inductance up to several percent for a minimum dummy distance below 5 µm from the inductor).
While the density rules usually cannot be considerably relaxed by the foundry, the arbitrary insertion of dummies by an automated process can be minimized by creating an initial layout that already respects the density rules over large parts of the circuit. As in this case the presence of metal is known during design, it can be taken into account in simulations.
This thesis still relied on automatic dummy insertion in the vicinity of spiral inductors, while large open spaces in the layout are filled with a structure containing about 50% of metal in each layer. This structure is shown in the next subsection.

3.7.2 *Ground- and Supply Distribution Network*

The design of the ground plane and the supply distribution network in circuits implemented in a nanoscale CMOS technology is highly influenced by the stringent metal density requirements. The structures described in the following are inspired by the a presentation of S. Voinigescu *et al.* in [199].

In the circuits designed as part of this thesis, a ground plane covers almost the entire substrate. The only exceptions are areas where active devices are located or the inside of the ground ring that surrounds spiral inductors. The ground plane shields the signals from the low resistivity substrate, and serves as a return path for the supply currents. Because a continuous ground plane would violate the density rules, the structure shown in figure 3.55 is employed.

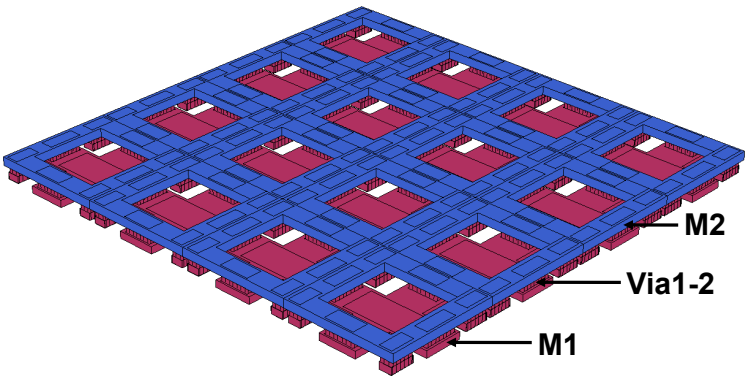


Figure 3.55: Ground plane consisting of shunted metal layers M1 and M2

It consists of small squares with a side length of 3 µm, that are joined to each other to constitute a large surface. The metal layers M1 and M2 used to build this ground plane are connected to each other and the substrate by a large number of vias and substrate contacts, thus maximizing conductivity. As the metal density is about 50 %, the density rules are well respected in layers M1 and M2. Dummy patterns on the active and polysilicon layers are manually added to furthermore comply with the density rules associated to these layers.

In circuit regions where this does not deteriorate circuit performance, the ground plane can be complemented by the higher metal layers, yielding the structure given in figure 3.56. In this structure, the metal layers M4 and M6 are shunted to the ground plane below by a multitude of vias, while the layers M3, M5 and M7 constitute planes of independent potential. While the M7-plane carries the supply current, M3 and M5 can be used to route the bias voltages.

The structure given in figure 3.56 has several benefits:

- It respects all density rules, thus avoiding the arbitrary insertion of dummy metal.
- It provides the routing of ground, supply and bias currents with maximized conductivity.

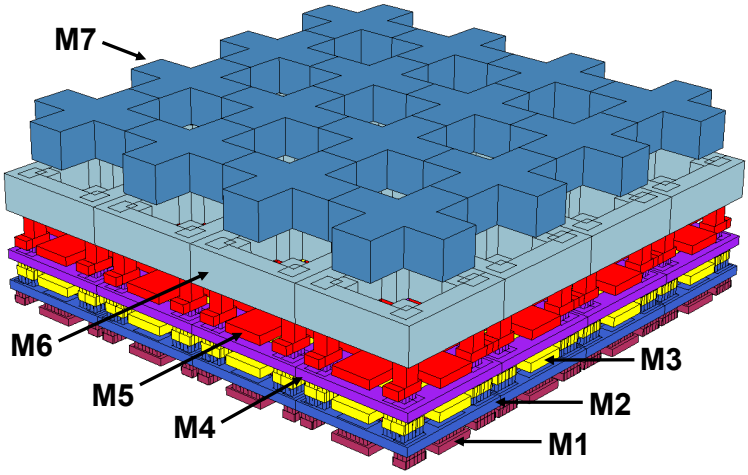


Figure 3.56: Shielding and supply distribution network consisting of all copper metal layers (metal layer 7 for V_{DD}, metal layer 3 and 5 for bias voltages and interconnected metal layers 1,2,4 and 6 for ground).

- It allows to isolate adjacent devices and building blocks by forming grounded metal cages.
- It adds a huge grounded capacitance to the planes consisting of M3, M5 and M7, thus increasing the decoupling of bias and supply voltages from RF signals.

Due to these advantages, the structure of figure 3.56 is used in all circuits of this thesis to fill the unused space between devices and building blocks.

3.7.3 *Signal and Bias Pads*

In order to connect the RF signal and the bias and supply voltages to the CMOS circuit, appropriate pads need to be designed. Their implementation should take into account the fact that testing in the framework of this thesis is done using on-wafer probes, while the use of flip-chip connections is intended for the future SiP integration.

For the RF connection, Ground-Signal-Ground (G-S-G) pads with a pitch of 100 µm between two adjacent contact points are chosen to minimize circuit size, which is often pad-limited. The size of the ground pads should be maximized to realize a large contact area and to optimize the connection to the ground plane. The size of the signal pads should be minimized in order to minimize the pad capacitance, which short-circuits the 60 GHz signal to ground. The lower bound for the pad size is given by the minimum area on which a reliable contact is possible.
The dimensions adopted for the G-S-G pad are given in figure 3.57 together with the pad geometry. The signal pad consists of a shunt connection of M7 and the aluminum layer alucap. The passivation layer CB2 exhibits an opening window over the entire pad surface. Beneath the pad, the M1-M2 ground plane discussed in subsection 3.7.2 covers the substrate. The simulated parasitic pad-to-ground-capacitance is about $C_{pad} = 26\,fF$ (before dummy fill).
The ground pads are realized by a massive connection of all metal layers

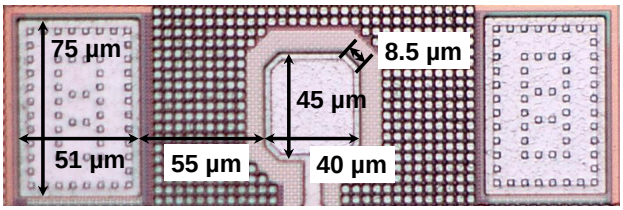


Figure 3.57: Die photo of G-S-G pad with annotated dimensions

from alucap down to the ground plane, to which they are connected over the whole pad surface. The small dots visible on the pad surface originate from the vias connecting the M7 layer to alucap. As for the signal pad, the opening in the CB2 passivation layer covers the whole pad surface. Note that the G-S-G-S-G pads for differential signals are created correspondingly.
The structure of the supply and bias pads is similar to the ground-pads in a G-S-G configuration. However, a square shape with a side length of 75 µm is chosen to maximize contact area: even when employing a pitch of 100 µm, the distance between two pads remains sufficiently large. The supply pads descend down to the layer in which the associated signal is routed. To ensure mechanical stability, the layers below the pads are not used. However, the ground plane continues below pads to ensure substrate shielding.
Note that no ESD protection is integrated in the pads as the realized circuits are intended for research purposes only. In a commercial design, protective measures are however indispensable.

3.8 CONCLUSION

This chapter provides the prerequisites for the successful design of the building blocks of a 60 GHz transceiver front-end.
First, a description of the 65 nm CMOS technology of STMicroelectronics is given. It focuses on the design-kit devices suitable for 60 GHz design and the metal back-end, which is used to implement full-custom passive devices.
Next, the design of full-custom active (varactors) and passive (inductors, transformers, transmission lines) devices is addressed. A special focus lies on the accurate simulation and measurement of 60 GHz spiral inductors, which are extensively used for circuit design in this thesis. The results of the work on inductor simulation and measurement de-embedding is published in [200] and [195].
In the remaining part of this chapter, various design and layout techniques, which prove useful when designing mm-wave circuits in a nanoscale CMOS technology, are addressed.
Based on the devices and techniques described in this chapter, the chapters 4 and 5 describe the design of 60 GHz circuit components and a 60 GHz receiver front-end.

4 FRONT-END KEY BUILDING BLOCKS IN 65 NM CMOS

4.1 INTRODUCTION

This chapter discusses the implementation of the key building blocks for the 60 GHz transceiver front-end introduced in section 2.5 of chapter 2. Due to the low-power low-cost application the transceiver has to serve, these building blocks need to exhibit low power consumption, high efficiency and small chip size. In addition to that, their bandwidth has to cover at least one of the 60 GHz channels of 1.88 GHz presented in chapter 1.
The implementation of the building blocks is based on the 65 nm CMOS technology of STMicroelectronics. Both the design kit devices and the full-custom active and passive components presented in the previous chapter are utilized for the design.
In the following, a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a down-conversion mixer and an up-conversion mixer are presented in sections 4.2 to 4.5. For each building block, a brief literature review is given. Then, the component's design is outlined and the measurement results are presented. Finally, a table compares the achieved results to the state of the art.

4.2 THE LOW NOISE AMPLIFIER

This section deals with the design of the first essential building block of a 60 GHz receiver front-end, the Low Noise Amplifier (LNA). Besides the requirements of very low power consumption and small chip area, which dominate the design of all circuits in this thesis, *both* Noise Figure (NF) *and* gain of the LNA decisively influence the receiver's performance. This can bee seen from the Friis equation [146], which is discussed for the complete receiver front-end in section 2.5.2 of chapter 2. A simplified version, where NF_{LNA} is the noise figure of the LNA, NF_2 the total noise figure of all subsequent circuit elements, and G_{LNA} the gain of the LNA, reads

$$NF_{tot} = NF_{LNA} + \frac{NF_2 - 1}{G_{LNA}}. \tag{4.1}$$

It shows that in order to achieve a low receiver noise figure NF_{tot}, a high LNA gain is essential, because it allows to screen the usually much higher noise figures of the subsequent stages.
Another important characteristic of the LNA is its reverse isolation. This is especially important if a direct conversion architecture is used, since the LO leakage via the mixer to the receive-antenna has to be minimized (cf. section 2.4.4). Furthermore, a good reverse isolation ensures unconditional stability of the amplifier.

The LNA was one of the first 60 GHz building blocks that has been realized in CMOS technology (cf. the 2005 milestone paper by C.H. Doan, S. Emami *et al.* [61]). Since then, a multitude of 60 GHz CMOS LNAs have been published, all of them using either Common Source (CS) stages, cascode stages, or a mix of them. While the majority uses Transmission Lines (TLs) for matching [61, 80, 163, 201–212], T. Yao *et al.* showed in their 2007 article the benefit of using spiral inductors and proposed an algorithmic design procedure, which was also followed during the design of the LNA presented in the following. Other inductor-based LNAs found in literature confirm the interest of using spiral inductors to design the matching networks [175, 213]. Transformer-based LNAs have also been demonstrated in the 60 GHz band [214, 215]. Their benefit is the very large achievable bandwidth.

Like all other building blocks shown in this thesis, the LNA is implemeted using full-custom spiral inductors (cf. section 3.4 for more details on their design and properties). As reverse isolation and stability are essential for the transceiver performance, a cascode topology is employed.
The following subsections give details on the LNA design, show the obtained measurement results and compare the achieved performance to the publications mentioned above. A second, slightly modified version of the LNA is briefly introduced in subsection 4.2.4.

4.2.1 *Design of the LNA*

The low noise amplifier employs two single-ended cascode stages as illustrated in figure 4.1. The algorithm of [156] is followed throughout design.

The first stage is optimized for very low noise. Therefore, the transistors are biased around minimum NF current density at 0.15mA/µm (cf. section 3.6.1.1). The widths of the transistors M1 and M3 are chosen to be $22 \times 1\mu m$ in order to yield a real part of the optimum noise impedance R_{SOPT} that equals $50\,\Omega$ to facilitate matching. All transistors used in the design have a minimum drawn gate length of 60 nm.
The inductor L_{m1} forms an artificial transmission line together with the parasitics of M1 and M3, and thus increases the f_T of the cascode [156]. The value of L_{m1} is 87 pH. A degeneration inductor is added at the source of M1 to allow a simultaneous noise and power match of the LNA input. Using L_{deg} =97 pH, the real part of the input impedance yields around $50\,\Omega$, without changing R_{SOPT}. The benefits of inductive source degeneration and the associated theoretical background in given in subsection 3.6.3 of chapter 3.
The input of M1 has to be matched to the $50\,\Omega$ source impedance in parallel with the 26 fF pad capacitance. Because the imaginary part of the optimum noise impedance X_{SOPT} is roughly equal to the negative imaginary part of the input of M1, a simultaneous noise and conjugate match is achieved. The matching network consisting of C_{in} =55 fF, a $50\,\Omega$ transmission line of length 25 µm, and L_{in} = 139 pH is designed using the Smith chart for a match around 60 GHz.
The second stage is optimized for high gain and linearity. Therefore, the transistors are biased at the maximum f_T current density around 0.3 mA/µm. The transistors M2 and M4 have a width of $26 \times 1\mu m$ and thus are slightly larger than M1 and M3 for improved linearity of this second stage. The middle inductor for the second stage was chosen to be L_{m2} = 73 pH.
The input and output of the second stage are power matched to the preceding stage and the load impedance ($50\,\Omega$ in parallel to the pad capacitance). The values for the interstage matching network are L_{L1} = 125 pH and C_C = 210 fF, the values for the output matching network are L_{L2} =139 pH and C_{out} =38 fF.

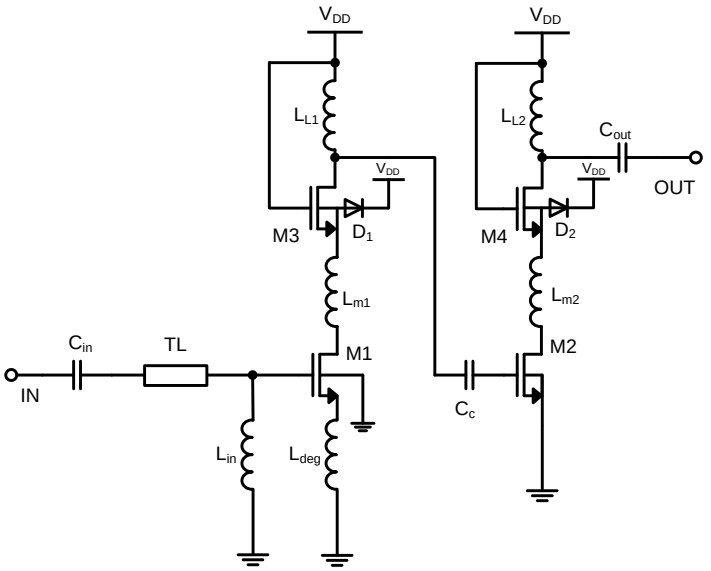


Figure 4.1: Simplified schematic of the designed two-stage cascode LNA (parasitic diodes D_1 and D_2 due to deep n-wells surrounding M3 and M4)

4.2.1.1 *Transistors*

Like all 60 GHz building blocks of this thesis, the LNA uses LVT GP NMOS transistors to maximize performance at a given power consumption. One consequence of their use is the lower breakdown voltage of 1 V. A remedy used during LNA design is to embed the cascode transistors into a deep n-well as illustrated in section 3.2.2.5: In doing so, they are isolated from the grounded substrate and drain and gate voltages in excess of 1 V become feasible. The parasitic diodes that originate from the additional p-n junctions are added to the schematic in figure 4.1.
While the presented circuit was designed for a V_{DD} of 1.5 V, a lower supply voltage of 1 V can be employed to reduce power consumption and harmonize the supply voltage to the one employed by the other building blocks for front-end integration.

4.2.1.2 *Fabricated Circuit*

Following the circuit design outlined above, the layout of the circuit is done. Besides the accurately modeled inductors and the small piece of transmission line at the input of the circuit, interconnect lengths are short enough to be neglected.
The presented circuit was fabricated in the 65 nm CMOS technology of STMicroelectronics described in section 3.2. Figure 4.2 shows a photo of the fabricated circuit. Four bias pads and 2 G-S-G pads for the 60 GHz in- and output surround the LNA core and limit the size of the LNA to 0.16 mm^2.

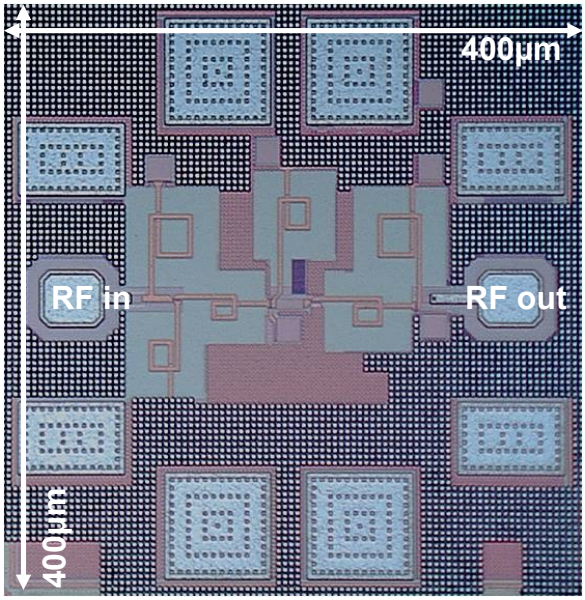
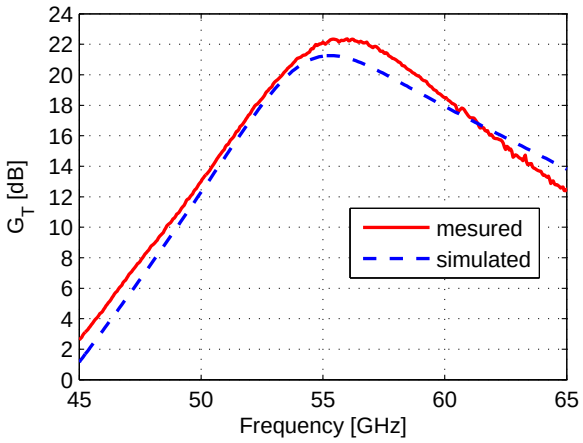


Figure 4.2: Photo of the fabricated LNA, circuit dimensions 400 µm x 400 µm including pads.

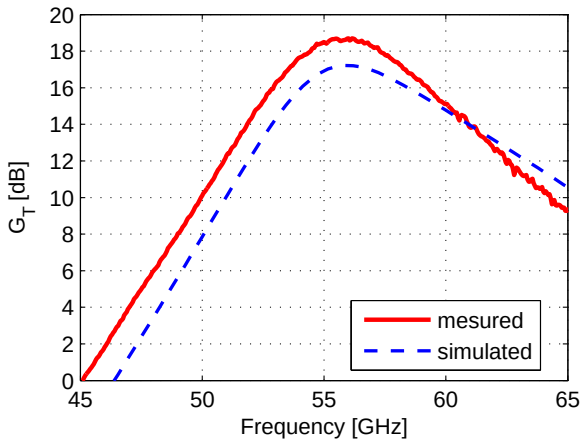
4.2.2 *Results*

Measurements up to 65 GHz are performed using an Anritsu ME7808A Vector Network Analyzer (VNA). A SOLT calibration moves the reference planes to the probe tips. No de-embedding of the pads is required

as their capacitance is taken into account by the circuit's matching network.
The measurement of the circuit performance is done at two different bias points: The first *high gain* bias point at V_{DD}=1.5 V requires a supply current of 11.2 mA and thus yields a power consumption of 16.8 mW. The second *low power* bias point employs V_{DD}=1.0 V, drawing 8.5 mA supply current and thus exhibiting a power consumption of 8.5 mW.
The transducer power gain G_T at these bias points is shown in figure 4.3a and 4.3b, respectively. Peak gain values of 22.4 dB and 18.7 dB, both at 56 GHz, are achieved, showing good agreement with simulation results.
The input and output matching of the LNA at the *high gain* bias point is illustrated in figure 4.4 (for the low power bias point the curves are very similar). A Return Loss (RL) inferior to -20 dB is measured around 56 GHz. Furthermore, on the basis of the S-parameter measurements, unconditional stability of the LNA is verified.
In order to quantify the linearity of the LNA, its output power (P_{out}) is measured versus the input power (P_{in}), thus obtaining the 1 dB compression point (P_{-1dB}). In figure 4.5 this curve is plotted together with the uncalibrated gain at the *high gain* bias point. An output-referred



(a) supply voltage of 1.5 V



(b) supply voltage of 1.0 V

Figure 4.3: Small signal transducer power gain G_T of the LNA, measurement results versus Cadence SPECTRE simulation

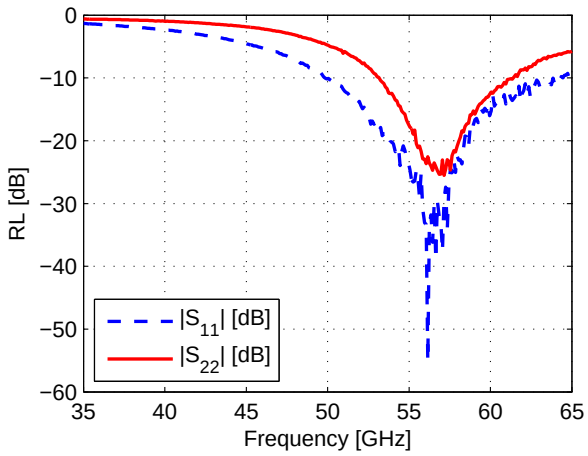


Figure 4.4: Return Loss (RL) measured at the input and output of the LNA biased at V_{DD}=1.5 V.

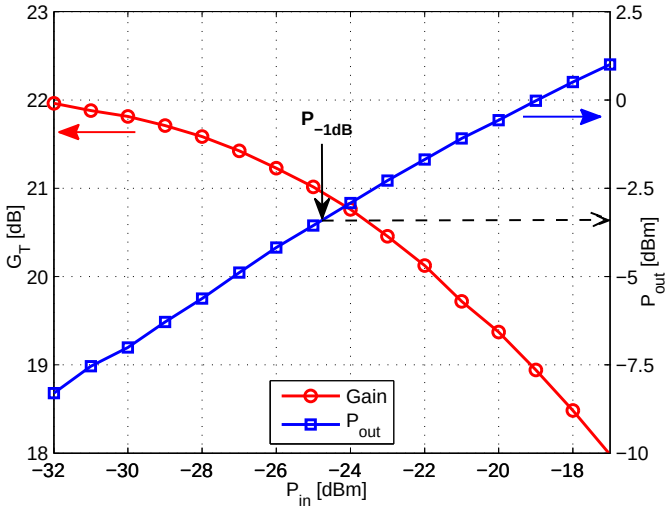
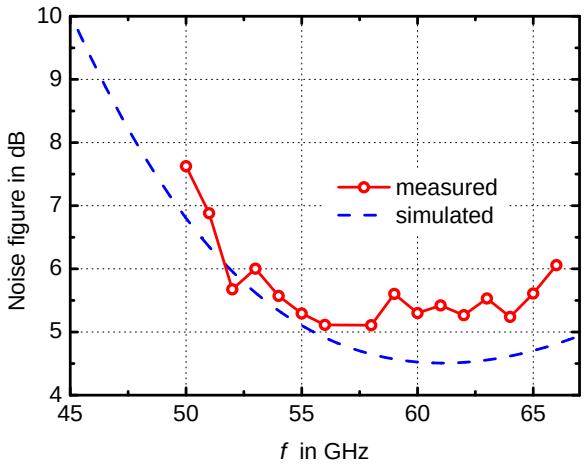


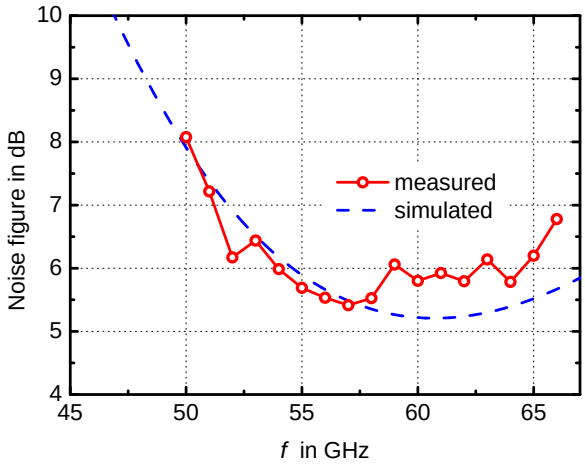
Figure 4.5: Plot of measured transducer power gain G_T and output power P_{out} versus input power P_{in} to obtain the 1 dB compression point.

OP_{-1dB} of -3.4 dBm is measured, which is sufficient according to the system considerations of section 2.5.2. For the *low power* bias point, OP_{-1dB} equals -6.5 dBm (curve not shown).
The presented results stem from one single die. Measurements of several other dies of the same wafer confirm the obtained results very closely.

The NF of the LNA has been measured using a 60 GHz noise figure measurement system employing the Rohde & Schwarz FSU 67 GHz spectrum analyzer and the associated FS-K30 noise figure measurement software to control both calibration and measurement. A Noisewave NW50G75-W noise source, with an Excess Noise Ratio (ENR) above 15.5 dB, calibrated from 50 to 75 GHz in 1 GHz steps is employed. Furthermore, isolators and a LNA with about 30 dB gain in the measurement bandwidth are completing the system. The measurement is based on the Y-factor method. The noise contribution of the spectrum analyzer and the access cables is removed by calibration and de-embedding, allowing a very high precision of the measurements (about $\pm$0.1 dB).



(a) supply voltage of 1.5 V



(b) supply voltage of 1.0 V

Figure 4.6: Measured versus simulated noise figure for supply voltages of 1V and 1.5V.

Figure 4.6 plots the measured and simulated NF for both operating points of the amplifier. Measured minimum values of 5.1 dB (at 1.5 V) and 5.4 dB (at 1.0 V) have been obtained, while the noise performance remains close to these minima all over the band of interest. The measurements are very close to the NF predicted by simulation, which confirms the good accuracy of the BSIM4 models even with respect to noise parameters at 60 GHz. The slightly higher measured NF can be attributed to, among others, the contact resistance of the on-wafer probes and the non-ideality of the contact pads.

4.2.3 *Comparison to the State of the Art*

Table 4.1 on page 116 presents a performance overview comparing 60 GHz CMOS LNAs found in literature with the proposed amplifier. General observations are that the noise figure decreases with scaling of technology, and that circuits using lumped elements exhibit smaller size and better over-all performance. The LNA developed in this thesis yields the lowest power consumption of, and the best performance compromise for all LNAs employing a cascode topology, showing the

Table 4.1: Performance comparison to LNAs found in literature

Ref.	Techn. [nm]	Freq. [GHz]	max. G_T [dB]	OP_{-1dB} [dBm]	min. NF [dB]	V_{DD} [V]	P_{DC} [mW]	Area [mm^2]	Topol.	Match.
C.H. Doan, 2005 [61]	130	60	12	+2	8.8	1.5	54	1.3	cas-code	TL
C.M. Lo, 2006 [201]	130	56	24.7	+1.8	7.1	2.4	79.2	0.48	cas-code	TL
B. Heydari, 2007 [163]	90	60	12.2	+4	6[5]	1.0	10.4	0.48	CS	TL
T. Yao, 2007 [156]	90	58	14.6	-0.5	5.5	1.5	24	0.14	cas-code	lmpd.
M. Varonen, 2007 [202]	65	60	11.5	1.5	5.6	1.2	72	0.61	CS	TL
H.Y. Yang 2008 [203]	130	53	14	-6	6.1	1.2	10.6	0.53	CS	TL
S. Pinel, 2008 [80]	90	60	16	+1	6	1.8	29	N.A.	cas-code	TL
S. Pellerano, 2008 [204]	90	64	15.5 13.5	+3.8 N.A.	5.2 N.A.	1.65 1.26	85.8 47.9	0.52	cas-code	TL
E. Cohen, 2008 [175]	90	58	15	-4	4.4	1.3	3.9	0.14	CS	lmpd.
A. Siligaris, 2008 [205]	65[1]	64	12	-5	8	2.2	36	1.0	cas-code	TL
C. Weyers, 2008 [214]	65	60	19.3	+2.7	6.1	1.2	34.8	0.21	cas-code	xfmr
A. Natarajan, 2008 [213]	65	57	16.7	+1.6	5.9	1.5	30.8	1.05	cas-code	lmpd.
C. Pavageau, 2008 [206]	45[2]	60	13.4	N.A.	5.6	1.8	95	0.36	cas-code	TL
I. Haroun, 2009 [207]	90	54	11.5	N.A.	4.1	1.5	15.1	0.2	cas-code	TL
Y.S. Lin, 2009 [208]	65	59	17.1	N.A.	8.2	1	21.4	0.475	cas-code	TL
B.R. Huang, 2009 [209]	130	58	20.4	+0.4	7.2[3]	2.4	65	0.72	cas-code	TL
W.H. Lin, 2009 [210]	90	60	13	-7	6.3	0.7	4.9	0.35	CS	TL
K. Kang, 2010 [211]	90	57	18.6	+2.8	5.7	1.2	29	0.7	CS	TL
E. Janssen, 2010 [215]	65	60	10	-4.6	3.8[4]	1.2	35	0.94	CS	xfmr
C.C. Chen, 2010 [212]	130	58	11.1	-3.1	5.4	1.5	29.1	1.09	cas-code	TL
proposed LNA [176]	**65**	**56**	**22.4** **18.7**	**-3.4** **-6.5**	**5.1** **5.4**	**1.5** **1.0**	**16.8** **8.5**	**0.16**	**cas-code**	**lmpd.**

[1] SOI, [2] physical gate length, [3] without the ESD protection, [4] measured at $37 + j10\Omega$, [5] simulated

interest of using a 65 nm CMOS technology and lumped inductors for LNA design. The work presented by E. Cohen *et al.* [175] demonstrates the interest of using small transistor widths and a simpler common source (CS) topology, if the high reverse isolation of a cascode topology is not necessary.

4.2.4 *LNA Redesign*

To integrate the LNA into the receiver front-end, a redesign has been done. The first objective was to remove the need for two external bias voltages and achieve optimum biasing without manual adjustments. This is achieved using current mirrors for biasing as discussed in section 3.6.1. The new circuit consumes 11 mA from a 1 V voltage supply.
The second objective is to increase the frequency of operation to get the maximum gain at 60 GHz. This is done by slightly adjusting the input, output and interstage matching networks of the amplifier.
As illustrated in figure 4.7, the new LNA achieves a center frequency of around 58.3 GHz and a gain of 16.8 dB at a supply voltage of 1 V. Its 3 dB bandwidth reaches from 54.3 GHz to 61.6 GHz. Figure 4.8 shows the return loss of the LNA. The minimum for both in- and output match lies around 58 GHz. A good match well below −10 dB is achieved throughout its 3 dB bandwidth.
The fact that the LNA's center frequency, while increased with respect to the initial design, is still below 60 GHz can be explained by the increased insertion of dummy metal (cf. section 3.7.1) during the second fabrication run. This seems to add sufficient parasitic capacitance to the spiral inductors to decrease the amplifier's center frequency by 2.8 %.
Figure 4.9 plots the measured noise figure of the redesigned LNA at $V_{DD} = 1.0\,V$. The minimum value of 6.4 dB lies above the one of the initial LNA design. This can be explained by the fact that, due to the use of current mirror biasing, the redesigned LNA is biased slightly above the minimum NF current density.

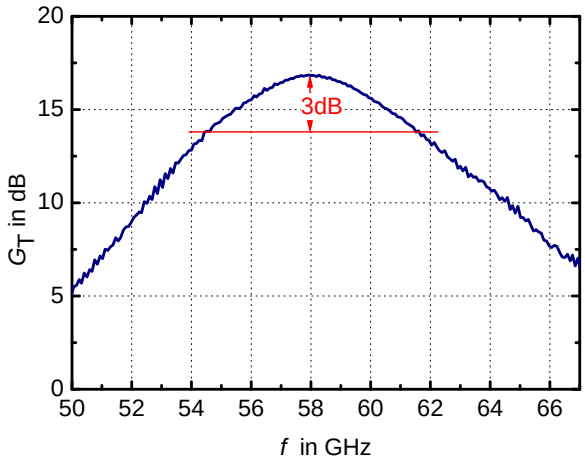


Figure 4.7: Measured transducer power gain of the redesigned LNA at V_{DD}=1V

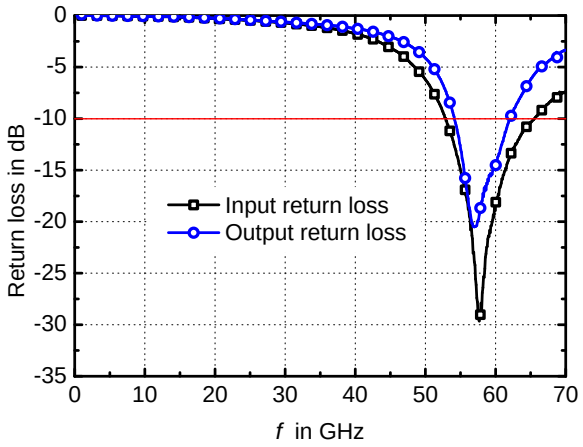


Figure 4.8: Measured return loss of the redesigned LNA biased at $V_{DD} = 1\,V$

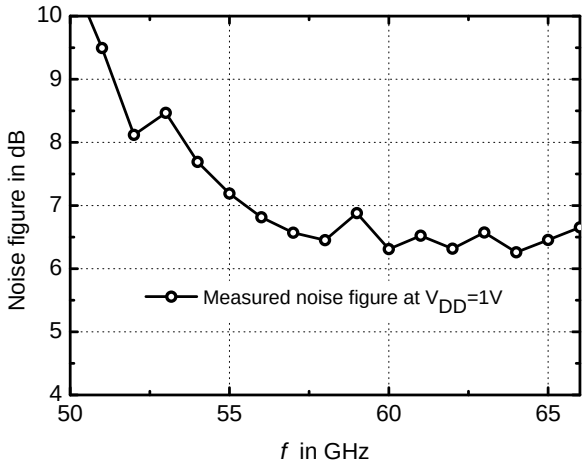


Figure 4.9: Measured noise figure of the redesigned LNA biased at $V_{DD} = 1\,V$

4.2.5 *Conclusion on the LNA*

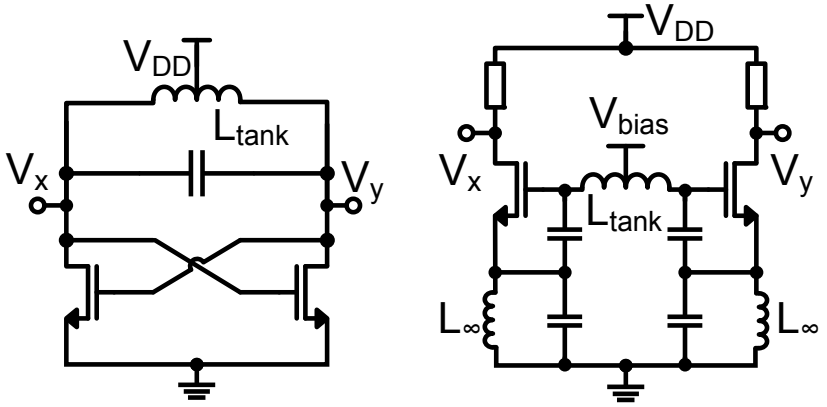
The high-gain low-power LNA presented in this section exhibits state-of-the-art performance, yielding a very good compromise for the input stage of a low-cost low-power 60 GHz receiver. Key points in circuit design are the use of inductors, the embedding of the cascode transistor in a deep n-well to allow higher supply voltages, and the use of the 65 nm CMOS technology for low power-consumption and low noise. The LNA has been published in [176].
The initial LNA has been modified in order to facilitate biasing and slightly increase its operating frequency. It is this redesigned version that is used in the receiver front-end presented in chapter 5.
To minimize coupling effects, a differential version of this LNA should be implemented if power consumption is less of an issue, and the preceding (antenna or phase shifters) and subsequent elements (down-mixer) allow this.

4.3 THE VOLTAGE CONTROLLED OSCILLATOR

As discussed in chapters 1 and 2, the transceiver front-end developed in the framework of this thesis has to meet severe power consumption requirements. However, when it comes to the design of oscillators, reducing power consumption is not enough: output power is equally important, because mixer performance increases with local oscillator power. Furthermore, the output of an integrated VCO supplies several circuit blocks (e.g. I and Q mixer and phase locked loop). Hence, when sacrificing VCO output power to reduce power dissipation, additional, power-hungry circuit blocks become necessary: the overall power consumption is not reduced.
Thus, in order to minimize transceiver power consumption, the VCO's *efficiency* has to improve. At the same time, this increase of efficiency should neither be done at the expense of Frequency Tuning Range (FTR) nor phase noise performance.
CMOS VCOs operating around 60 GHz regularly exhibit quite low output power (see table 4.2 at the end of this section). Even the most powerful designs like [216] with P_{out}=-4 dBm and [217] with P_{out}=-6.6 dBm stay well behind their SiGe counterparts. At the same time, efficiency is usually poor for these realizations with high output power. In the following, a VCO design is detailed which optimizes efficiency. Due to the use of a differential common-source Colpitts architecture [218], which was not yet used for CMOS oscillators operating in the 60 GHz band, a record efficiency of up to 4.9% and a record ouput power of up to -0.9 dBm is achieved.

4.3.1 *CMOS VCOs in the 60 GHz band*

Since the year 2001 [219], a multitude of CMOS VCOs operating in and around the unlicensed 60 GHz band have been published. While first implementations make use of 250 nm CMOS [216, 219], more recent designs use technologies down to the 65 nm node. Also SOI CMOS technologies have been employed [217, 220].
A large majority of the 60 GHz CMOS VCOs uses the differential cross-coupled architecture illustrated in figure 4.10a. To allow frequency



(a) Cross-coupled oscillator (b) Common-drain Colpitts oscillator

Figure 4.10: Commonly used architectures for 60 GHz VCOs

tuning, a part of the tank capacitance is made of one of the different kinds of MOS-based varactors presented in section 3.3: references [171, 219–222] use analogly tuned AMOS varactors, [223, 224] use IMOS varactors and [81, 216, 217, 225–229] use varactors based on unmodified MOS transistors. More exotic designs employ switched AMOS varactors [173, 230, 231] or exploit either the intrinsic variable MOSFET capacitance [232] or the Miller effect [233] for tuning.
Besides the cross-coupled topology, two other architectures also have been implemented: K.W. Tang *et al.* employ the differential common-drain Colpitts topology [234] illustrated in figure 4.10b. It was used before at lower frequencies [235] and is more common in SiGe realizations. L.M. Franca-Neto *et al.* use optimum pumping for their oscillator [236], which however is not voltage controlled. The conclusion on VCO design (subsection 4.3.4 of this section) contains a comparison of the afore mentioned oscillators in table 4.2 and gives more details on their performance.
The VCO proposed in the following makes use of an alternative architecture, based on a differential common-source Colpitts VCO [218]. It is is to the best of the author's knowledge not yet employed in the 60 GHz band. Circuit design is detailed in the next subsection.

4.3.2 *Oscillator Circuit Design*

In the following the design of a high-efficiency VCO is described. First, the adopted differential Colpitts architecture is introduced together with its benefits. Then, the dimensioning of the resonator's elements is discussed. Further subsections give more details on the output buffers and the way the tank inductor and the varactors are chosen.

4.3.2.1 *The adopted architecture*

The simplified schematic of the proposed VCO is given in Fig. 4.11. The chosen architecture can either be considered as the extension of a cross-coupled oscillator by capacitive voltage dividers. Alternatively, and more consistent with earlier implementations at lower frequencies (e.g. [218]), it can be seen as a differential Colpitts oscillator (whose decisive feature is the feedback using capacitive voltage dividers as shown in

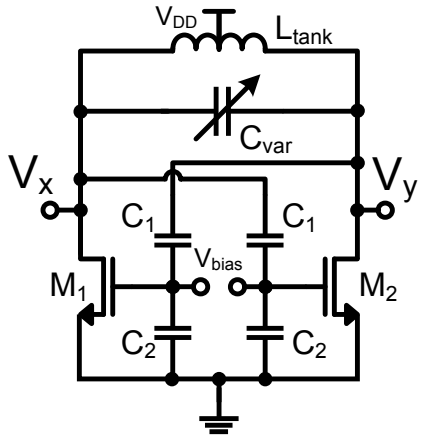
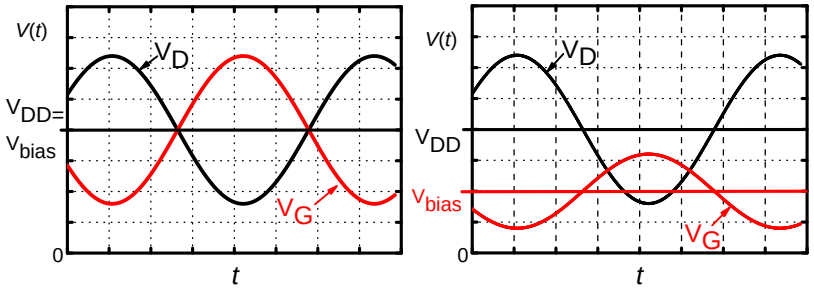


Figure 4.11: Schematic illustrating the principle of the common-source Colpitts VCO

the original patent[1]). The transistors are used in a common source configuration, which, in contrast to the common drain configuration shown in Fig. 4.10b, inverts the signal. Hence, the output signal is fed back from the other half of the differential circuit, where the drain voltage is available at inverted polarity due to odd-mode operation.



(a) Cross-coupled oscillator (b) Proposed Colpitts oscillator

Figure 4.12: Illustration of oscillators' gate and drain voltage

The key differences between the proposed Colpitts VCO and a cross-coupled VCO are illustrated in Fig. 4.12: 4.12a shows that the cross-coupled VCO's gate voltage is just an inverted version of its drain voltage, implying that gate bias voltage and supply voltage are identical. In the case of a large voltage swing, the gate voltage deviates considerably from its initial (already non-ideal) bias point. As a consequence, the transistor is providing less transconductance than at the bias point, eventually even entering the triode region. This limits the drain voltage swing at which a cross-coupled VCO can provide sufficient negative resistance to further increase the oscillation amplitude.
In the case of the proposed Colpitts VCO, the capacitive connection between gate and drain allows to independently choose the gate bias voltage as illustrated in Fig. 4.12b. Hence, the drain current density of the transistors can be chosen arbitrarily, and one of the optimum bias points discussed in section 3.6.1 can be selected. Because efficiency is the main issue here, a current density of around $0.3\,\mathrm{mA/\mu m}$, which maximizes the transistor's linearity [156], is set. Alternatively, to minimize the noise contribution of the transistors, the minimum noise current density of around $0.15\,\mathrm{mA/\mu m}$ may be selected. Note that in both cases a coefficient of the equation describing phase noise (equation (4.9), discussed in subsection 4.3.2.2) is optimized: in the former case it is the signal power P_{sig} due to the maximization of the tank voltage swing, in the latter case it is the noise factor F.
The gate voltage swing observed in Fig. 4.12b is $C_1/(C_1+C_2)$ times the drain voltage swing (in the illustration $C_1/(C_1+C_2) \approx 0.5$). Thus, the transistor's gate voltage stays close to the initial bias point. But, compared to the cross-coupled case, a Colpitts VCO requires wider transistors: this is because the capacitive voltage division also reduces the negative resistance that is added to the tank per micron of transistor width (cf. next subsection for the exact expression). However, as the drain current density of the transistors is much lower than in the cross coupled case, power consumption does not increase. Yet, the higher linearity provided by these larger transistors can be exploited to achieve

[1] E.H. Colpitts: Oscillation Generator, US patent 1,624,537, filed 02/1918, granted 04/1927

a higher output power, and thus increase efficiency.
In comparison to the common-drain Colpitts VCO of Fig. 4.10b, the proposed common-source VCO has the advantage of a potentially higher tank voltage swing and thus linearity. This is due to the fact that it connects the tank to the transistor's drain rather than to its gate and source. The disadvantage of the proposed solution with respect to the common drain VCO is that the oscillator's output and the tank share the same terminals: the attached load has thus an influence on the tank impedance. To minimize this influence and further increase output power, buffer amplifiers are employed (cf. subsection 4.3.2.5).

4.3.2.2 *Dimensioning of transistors and resonator elements*

Once the architecture and bias point of the VCO are fixed (differential common-source Colpitts, maximum linearity current density of 0.3 mA/µm, supply voltage $V_{DD} = 1\,V$ due to the use of GP transistors), the component values (L_{tank}, C_{var}, C_1, C_2) and transistor widths (W_1=W_2) have to be found. Their influence can be illustrated by the small-signal equivalent circuit given in figure 4.13.

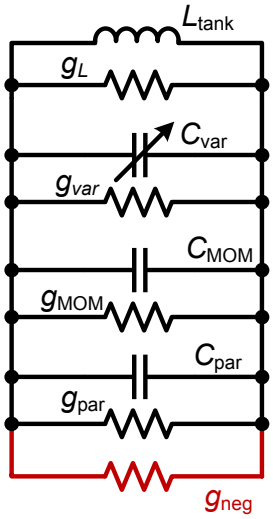


Figure 4.13: Steady-state parallel oscillator model

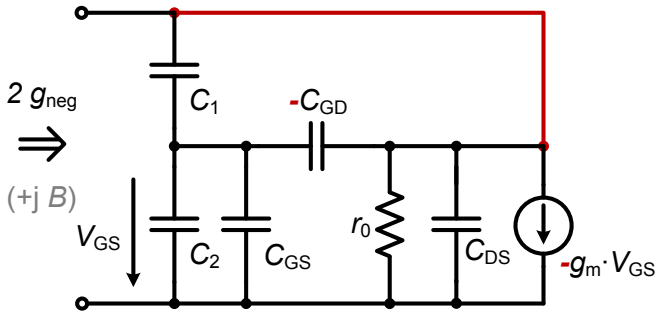
It contains the tank's capacitive and inductive energy storage elements. Here, L_{tank} represents the tank inductor and C_{var} the varactor. C_{MOM} is the equivalent capacitance of the capacitive voltage divider constituted of MOM capacitors C_1 and C_2. The remaining parasitic capacitance (originating from inductor, transistors and buffer amplifiers) is incorporated in C_{par}.
The loss associated to each of these elements is represented by parallel admittances: for the tank inductor, the parallel admittance at a frequency f can be approximated by

$$g_L \approx \frac{1}{2\pi f L_{tank} Q_L}, \tag{4.2}$$

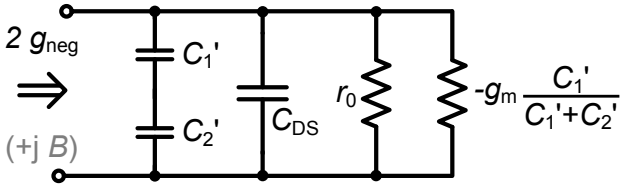
where Q_L is the inductor's quality factor. In the case of the loss associated with capacitors, the equivalent admittance at frequency f is given by

$$g_{capa} \approx \frac{2\pi f C}{Q_{capa}}, \tag{4.3}$$

where Q_{capa} is the respective capacitor's quality factor.
The negative small-signal admittance g_{neg} originates from the transistors in the capacitively cross-coupled feed-back configuration. To calculate its value from the elements of the transistor's equivalent circuit and the capacitances C_1 and C_2, odd mode operation is assumed. Then, the equivalent half-circuit is the one given in figure 4.14a (gate, source and drain resistances of the MOSFETs are neglected). To allow feedback from the output of this half circuit back to its input (and not to the input of the transistor at the opposite side), the signs of C_{GD} and the transconductance have to be inverted. The real part of the input admittance of this circuit is $2 \times g_{neg}$, because the half-circuit appears two times in series in the tank's equivalent circuit.



(a) Half circuit with odd-mode modifications indicated red



(b) Half-circuit after simplifications

Figure 4.14: Equivalent half-circuit to calculate the negative admittance g_{neg}

If assigning $C_1' = C_1 - C_{GD}$ as well as $C_2' = C_2 + C_{GS}$, and converting the controlled current source to an admittance (which is possible because the control voltage is a fraction of the voltage over the current source's terminals), the equivalent half circuit simplifies to the one shown in figure 4.14b. It shows that the negative admittance added to the full parallel tank is given by

$$g_{neg} = -g_m \frac{C_1'}{2\left(C_1' + C_2'\right)} + \frac{1}{2r_0}. \tag{4.4}$$

As g_m is proportional to the transistor width, the negative admittance can be adjusted either by sizing the transistor, or (as indicated in (4.4)) by choosing the voltage division ratio $C_1' / \left(C_1' + C_2'\right)$. Both transistor size and capacitance ratio influence output swing (and thus phase noise), power consumption and the fraction of parasitics added to the tank by the transistor.
Note also the imaginary part of the half-circuit's input impedance: the influence of the parasitic capacitances C_{GS} and C_{GD} is limited, because, being part of C_1' and C_1', they are connected in series. In the equivalent circuit of the tank (figure 4.13), the capacitances shown in figure 4.14 are incorporated in C_{MOM} and C_{par}. Based on this equivalent circuit,

whose elements are discussed above, the different characteristics of the oscillator are derived in the following.

FREQUENCY OF OSCILLATION f_0 The most fundamental property of the tank impedance at oscillation frequency is that its imaginary part vanishes. This fact is exploited to determine the VCO's center frequency f_0: it is given by

$$f_0 = \frac{1}{2\pi\sqrt{L_{tank}\left(C_{var,o} + C_{MOM} + C_{par}\right)}} = \frac{1}{2\pi\sqrt{L_{tank}C_{tot}}}, \tag{4.5}$$

if the varactor's capacitance is tuned to its midpoint value $C_{var,o}$. Equation (4.5) illustrates that for a given oscillation frequency the product of the total tank capacitance C_{tot} and the tank inductance L is constant, implying that if one factor increases (decreases), the other has to decrease (increase).
In a VCO, the oscillation frequency changes because C_{var} varies. The absolute frequency tuning range is given by [78]

$$\Delta f = \frac{1}{2\pi\sqrt{L_{tank}\left(C_{var,min} + C_{MOM} + C_{par}\right)}} - \frac{1}{2\pi\sqrt{L_{tank}\left(C_{var,max} + C_{MOM} + C_{par}\right)}}, \tag{4.6}$$

where $C_{var,min}$ and $C_{var,max}$ are the minimum and maximum values achievable by the varactors as discussed in section 3.3. The normalization of the absolute tuning range Δf to the center frequency f_0 according to

$$\frac{\Delta f}{f_0} = \sqrt{\frac{\left(C_{var,o} + C_{MOM} + C_{par}\right)}{\left(C_{var,min} + C_{MOM} + C_{par}\right)}} - \sqrt{\frac{\left(C_{var,o} + C_{MOM} + C_{par}\right)}{\left(C_{var,max} + C_{MOM} + C_{par}\right)}}, \tag{4.7}$$

shows that the relative Frequency Tuning Range (FTR) of the VCO only depends on the relationship between the different capacitances and the minimum and maximum of the varactor's capacitance. For first order considerations, the choice of the inductance can thus be done independently of the tuning range that should be achieved.

START-UP CONDITION AND POWER CONSUMPTION In order to allow the start-up of the oscillation, the loss associated with the reactive tank elements needs to be compensated by the negative admittance g_{neg}. The start-up condition hence reads

$$-g_{neg} > g_{var} + g_{MOM} + g_{par} + g_L. \tag{4.8}$$

A sufficient margin (in this thesis a factor of around two) has to be respected to ensure that this condition is always fulfilled. As long as (4.8) is true, the oscillation amplitude grows. However, as g_{neg} is a function of the tank amplitude V_{tank}, its effective large signal value decreases with increasing V_{tank}. If $|g_{neg}|$ is equal to the total tank admittance, the oscillation reaches the steady state.
As mentioned before, large g_{neg} values are realized by wide transistors and thus result in high power consumption. Thus, for low-power designs, the right hand side of (4.8) must be minimized. Equations (4.2)

and (4.3) show that this can be achieved by maximizing L_{tank} (and thus minimizing C_{tot}), because g_L is inversely proportional to the inductance value and g_{capa} is proportional to capacitance (if Q is considered to be independent of the capacitance/inductance value).

PHASE NOISE A multitude of theories to explain the physical processes of phase noise are available. Prominent examples are the works of D.B. Leeson [237], A. Hajimiri and T.H. Lee [133, 238], J.J. Rael and A.A. Abidi [239] or A. Demir *et al.* [240] (see [241] for an excellent overview). Most of them are subject of controversial discussions. While to the author of this thesis the latter one seems the most mathematically rigorous, and the advantage of a Colpitts architecture to minimize phase noise is well explained by the theory of A. Hajimiri *et al.*, the classical Leeson formula is used in the following to obtain fundamental design insights. This formula reads [133]

$$L(\Delta\omega) = 10\log_{10}\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{corner}}{|\Delta\omega|}\right)\right\}, \quad (4.9)$$

where the phase noise $L(\Delta\omega)$ is given in dBc/Hz[1] at a distance $\Delta\omega$ from the carrier at angular frequency ω_0. Q is the tank's quality factor, P_{sig} the power of the oscillating signal, k the Boltzmann constant, T the temperature, F the noise factor and ω_{corner} the corner frequency which separates the $1/f^3$ from the $1/f^2$ region in the phase noise spectrum. The latter two parameters have to be considered empirical in Leeson's phase noise model. In general, they can be minimized by minimizing the transistor's thermal and flicker noise contribution. In the following, the focus is on the less controversial parameters Q and P_{sig} that need to be maximized to minimize phase noise.

QUALITY FACTOR The quality factor of the VCO's tank can be derived from the general definition (see [165] and section 3.2.3) given by

$$Q = \frac{2\pi f E_{max}}{P_{diss}}, \quad (4.10)$$

where E_{max} is the total stored energy and P_{diss} is the dissipated power. $E_{max} = \frac{1}{2}C_{tot}V_{tank}^2$ at resonance, when the total energy is momentarily stored in the capacitors. The dissipated power is the product of the squared tank RMS voltage and the sum of all admittances. This yields a Q factor at angular resonance frequency ω_0 of

$$Q_{tank,o} = \frac{\omega_0\frac{1}{2}C_{tot}V_{tank}^2}{\left(\sqrt{2}V_{tank}\right)^2\left(\frac{1}{\omega_0 L_{tank}Q_L}+\frac{\omega_0 C_{var}}{Q_{var}}+\frac{\omega_0 C_{MOM}}{Q_{MOM}}+\frac{\omega_0 C_{par}}{Q_{par}}\right)}. \quad (4.11)$$

Due to the fact that $L = 1/(\omega_0^2 C_{tot})$ at resonance, (4.11) can be simplified to yield

$$\begin{aligned} Q_{tank,o} &= \frac{1}{\left(\frac{1}{Q_L}+\frac{C_{var}}{Q_{var}C_{tot}}+\frac{C_{MOM}}{Q_{MOM}C_{tot}}+\frac{C_{par}}{Q_{par}C_{tot}}\right)} \\ &= \frac{1}{\left(\frac{1}{Q_L}+\frac{1}{Q_{C,tot}}\right)}, \end{aligned} \quad (4.12)$$

[1] Note that the "per Hz" refers to a division by frequency *in the argument* of the logarithm

with

$$\frac{1}{Q_{C,tot}} = \frac{C_{var}}{Q_{var}C_{tot}} + \frac{C_{MOM}}{Q_{MOM}C_{tot}} + \frac{C_{par}}{Q_{par}C_{tot}}. \tag{4.13}$$

This allows two important observations with respect to the optimization of the tank's Q-factor:

- First, the inductive Q_L and the capacitive $Q_{C,tot}$ have the same impact on the tank Q regardless the employed values for L_{tank} and C_{tot}.
- Second, the capacitive Q factor is composed of the Q-factors of the individual capacitances, weighted by their proportion of the total capacitance. Furthermore, due to the fact that reciprocal values are employed to combine the Q-factors, worse Q factors have a bigger impact.

In summary, to optimize the tank's Q factor, the individual elements have to be optimized with respect to their Q factors and high loss capacitors should make up only a small portion of the resonator.

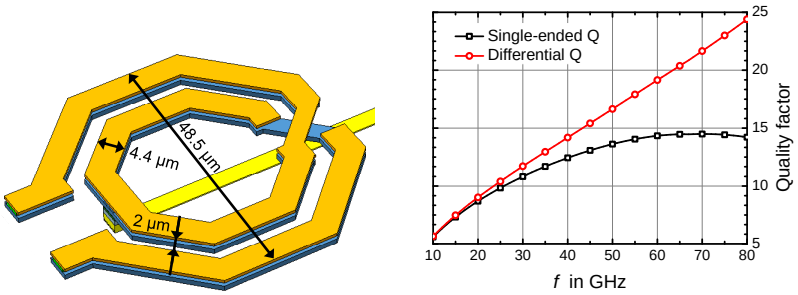
MAXIMIZATION OF SIGNAL POWER The oscillator's signal power P_{sig} is proportional to the reactive energy E_{tank} stored in the resonator. Because E_{tank} can be expressed either as a function of the resonating current or the tank voltage, it is important to note that in the present Colpitts oscillator, tank energy is limited by the tank voltage swing: either V_{GS} or V_{GD} of the core transistors is limited before this is the case for the drain current I_D (this corresponds to the fact of operating in the voltage-limited regime discussed in [242]).
Thus, E_{tank} has to be given here as a function of the tank voltage according to

$$E_{tank} = \frac{1}{2}C_{tot}V_{tank}^2 = \frac{1}{2\omega_0^2 L_{tank}}V_{tank}^2. \tag{4.14}$$

This equation shows that to maximize the signal energy at a given permitted tank voltage swing, L_{tank} must be minimized implying that C_{tot} is maximized. Or, to put it differently, a resonator operating at a given frequency f_0 is capable of stocking a higher amount of energy per tank voltage if it is constituted by a small inductance and a large capacitance. Note that this design rule is the opposite of the one for low power oscillators (where the inductance has to be maximized). Thus, in practice, a compromise has to be realized.

4.3.2.3 *The tank inductor*

As the tank inductor is connected with both ends to the resonator, its differential performance is more important than its single ended behavior. This has consequences on the optimization of the spiral dimensions aiming to obtain a high Q factor at the specified resonance frequency 60 GHz: slightly larger metal widths as in the case of single ended excitation, as well as shunting of the two topmost thick metal layers is advantageous in this case.
The layout of L_{tank} is given in Fig. 4.15a. In contrast to the other full-custom inductors used in this thesis (cf. section 3.4) it is of octagonal shape: this geometry exhibits slightly increased Q with respect to a



(a) Geometry of the tank inductor

(b) Q-factor of the tank inductor

Figure 4.15: Characteristics of the VCO's 155 pH tank inductor

rectangular geometry and permits the injection of the supply current at its symmetry plane. However, as it is quite cumbersome to implement, its application is limited to the VCO, where even slight increases in Q are beneficial for phase noise performance.
The value of L_{tank} is chosen to be 155 pH. This realizes a compromise between low power consumption, necessitating large inductors, and low phase noise, necessitating small inductors. Figure 4.15b shows the simulated effective Q-factors (defined as $|\mathrm{Im}\{Y_{nm}\}/\mathrm{Re}\{Y_{nm}\}|$) of the tank inductor. A very high value of 19.1 for the differential Q has been achieved at 60 GHz, while the single-ended Q has a value of 14.5 at that frequency.

4.3.2.4 *The accumulation MOS varactors*

Four full-custom Accumulation-mode MOS (AMOS) varactors, which are presented in section 3.3 of chapter 3 are used to change the VCO's oscillation frequency. They are differentially tuned as illustrated in figure 4.17 to reduce phase noise according to [243]. As one terminal of each varactor is connected to the supply voltage of 1 V, tuning is done for voltages at the other terminal that vary around this value. The parasitic diode to the grounded substrate thus does not interfere with varactor operation.
Each of the AMOS varactors has a capacitance ranging from 8.4 fF to 12.7 fF, which yields an equivalent varactor capacitance C_{var} where these values represent $C_{var,min}$ and $C_{var,max}$. According to equations (4.5) and (4.6), these values allow a tuning range of around 3 GHz around 60 GHz, if taking into account that L_{tank} equals 155 pH. Thus, about 35 fF is left for the remaining capacitors.

4.3.2.5 *The common-drain output buffers*

To minimize the loading of the VCO core and to allow the driving of a differential 100 Ω output, buffer amplifiers are employed. A common-drain topology is chosen for this purpose [217]: it exhibits a high input impedance which avoids loading of the VCO core. Furthermore, as it does not suffer from the Miller effect due to the fact that its voltage gain is less then unity, good reverse isolation can be achieved. Note that cascode-based buffers exhibit similar advantages and additionally provide voltage gain. Their use can thus be beneficial if voltage headroom is not an issue.

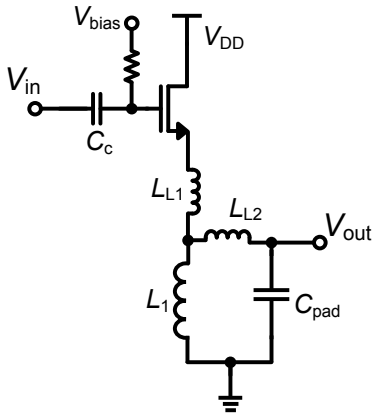


Figure 4.16: VCO source follower output buffer

Figure 4.16 shows the schematic of the buffer amplifier added to each one of the differential outputs of the VCO. Its input is decoupled from the VCO supply voltage by the capacitor C_c of value 32.9 fF which also further reduces loading of the VCO core. The transistor is a 65 nm GP device with 14x1 µm channel width to allow low power consumption. It is biased at maximum f_T current density to achieve good linearity and to allow the use of a common bias voltage with the VCO core.
The buffer outputs are matched to the 50 Ω load which appears in parallel with the parasitic pad capacitance C_{pad} of around 25 fF. An inductance value of L_1=197 pH is chosen. The matching also takes into account the parasitic interconnect inductances $L_{L1} \approx 14.6$ pH and $L_{L2} \approx 11.0$ pH.

4.3.2.6 *The finalized VCO design*

Figure 4.17 shows the schematic of the realized VCO. It combines the chosen differential Colpitts architecture with the common-drain buffers and the differentially tuned varactors. In order to maximize voltage headroom, provide common-come rejection and minimize phase noise, a tail inductor L_{tail} is employed. Its size of 85 pH is chosen to resonate

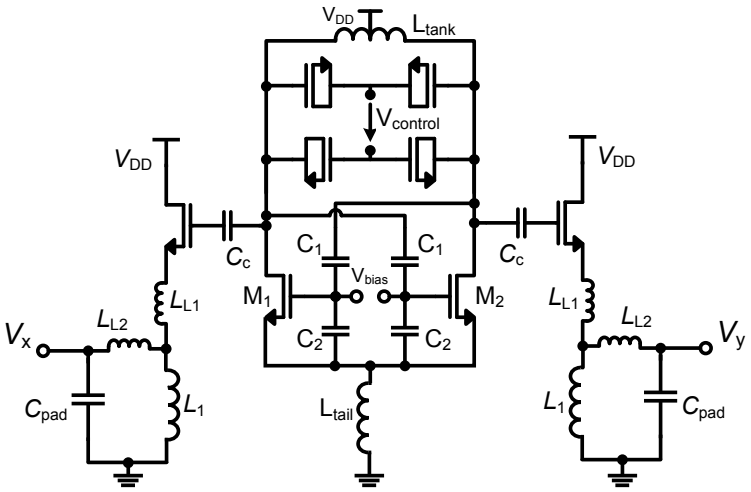


Figure 4.17: Proposed differential common-source Colpitts VCO (without bias circuitry), achieving high efficiency at 60 GHz

with the transistor's parasitic source-bulk capacitances in order to filter the second harmonic $2 \times \omega_0$ of the oscillation frequency [244].
The capacitive voltage divider and the transistor width is determined to accommodate the choice of the tank inductor and the varactors as outlined above. Initial hand calculations and subsequent optimization by SPECTRE simulations yield $C_1 = 38\,\text{fF}$, $C_2 = 22.7\,\text{fF}$ and a width of $14 \times 1\mu\text{m}$ for the 65 nm GP transistors.

4.3.3 *Measurement Results*

The fabricated VCO is shown in Fig. 4.18. Its size of 0.21 mm^2 is essentially limited by the numerous pads for signal, bias and control voltages as well as the buffer inductors.

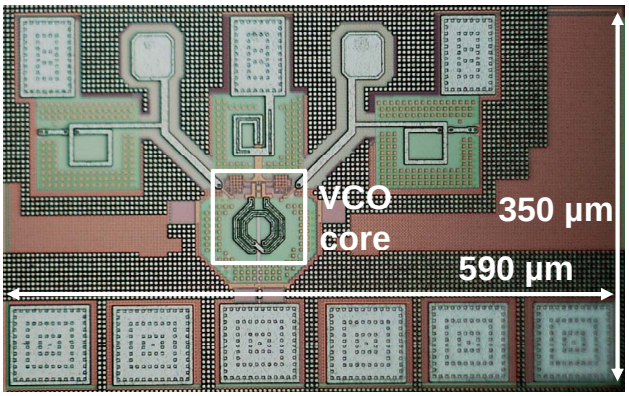


Figure 4.18: Die photo of the fabricated 60 GHz VCO (size pad-limited)

4.3.3.1 *Measurement setup*

The VCO was characterized on-wafer, using a R&S FSU 67 GHz spectrum analyzer for frequency, power and phase noise measurements. The output return loss is characterized using an Anritsu VNA. The bias, supply and tuning voltages were connected using an eye-pass probe with six tips separated by 100 µm pitch. Each of the tips is equipped with a decoupling capacitor connected to ground. The VCO is tuned by a differential voltage V_{control}, applied by two voltage sources with $V_{DD} \pm V_{\text{control}}/2$.
The spectrum analyzer was connected to one of the VCO's outputs, while the other output was terminated by a 50 Ω precision load. Corrections for cable loss and single-ended measurement (in total around 9 dB to 11 dB, depending on the cables used) are applied.
The phase noise measurements were done inside a Faraday cage using batteries to generate the required voltages. Because the phase noise was characterized on the *free-running* VCO (no PLL stabilized the VCO frequency), the purity of the voltage sources employed for measurements is essential to avoid an variation of the oscillation frequency induced by varying supply voltages.

4.3.3.2 *Startup of oscillation*

For a supply voltage of 1 V, the VCO starts oscillating at $I_D \approx 5\,\text{mA}$. This current is equally split between oscillator core and buffers, because they are biased at the same current density and consist of transistors

of identical size. At the maximum linearity bias point, the complete circuit draws 16.5 mA from a 1 V supply, which is the maximum voltage allowed to ensure reliability. All measurements presented in this section are done using this bias point. Figure 4.19 plots the oscillator's output spectrum at this bias point if the control voltage is zero.
(Further measurements using $V_{DD} = 1.2\,V$ have been done, showing a increased power consumption of about 24 mW. Consequently, the output power increases by about 2 dB. However, as this is not a reliable bias point, it is not employed in the following).

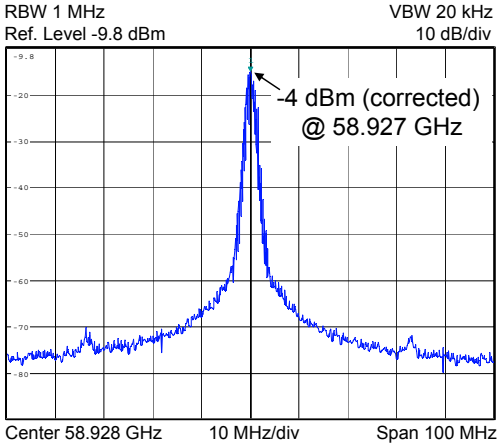


Figure 4.19: Measured oscillator output spectrum at 58.92 GHz ($V_{control}$=0 V)

4.3.3.3 *Frequency Tuning*

Figure 4.20 shows the oscillator's frequency tuning curve. The oscillation frequency f_0 reaches from 57.58 GHz to 60.80 GHz, which corresponds to a relative Frequency Tuning Range (FTR) of 5.4%. A sensitivity of around 1 V/ GHz is achieved. All measured circuits exhibit the same FTR within less then 0.1 GHz.
As mentioned before, the FTR can be increased in a future redesign, if necessary, by either minimizing the varactor's parasitic capacitance (cf. section 3.3) or increasing the fraction of the tank capacitance which is represented by the varactors.

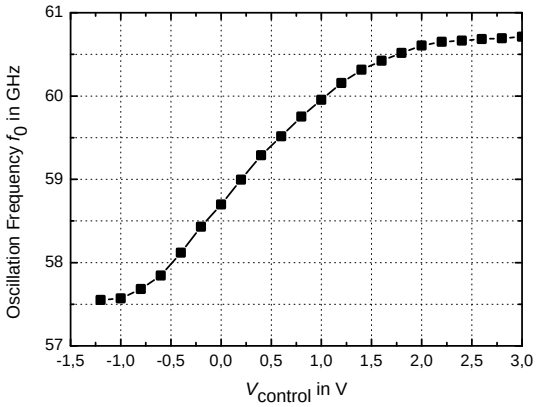


Figure 4.20: Measured tuning curve of the VCO

4.3.3.4 *Oscillator Output Power*

The major virtue of the proposed VCO is its high output power, especially if the circuit's low power consumption is kept in mind. As illustrated in figure 4.21, $P_{out,diff}$ is increasing with increasing frequency. Variations are due to the fact that the quality factor of the varactor is not constant over frequency. The maximum measured output power value is -0.9 dBm at 60.52 GHz, which corresponds to a maximum efficiency of 4.93%.

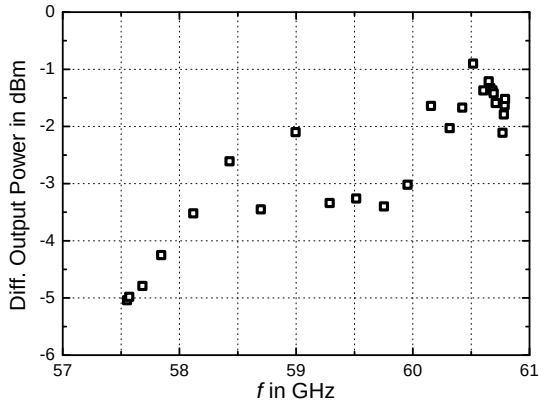


Figure 4.21: Measured differential output power

4.3.3.5 *Output matching*

Figure 4.22 shows the return loss measured at one of the outputs of the VCO. The reference plane for the calibration with respect to which these measurements are taken is the probe tip that contacts the G-S-G pads of the circuit's output. A very broadband match, attested by a measured return loss below -11 dB from 26 GHz to 65 GHz (upper limit imposed by measurements), is obtained.

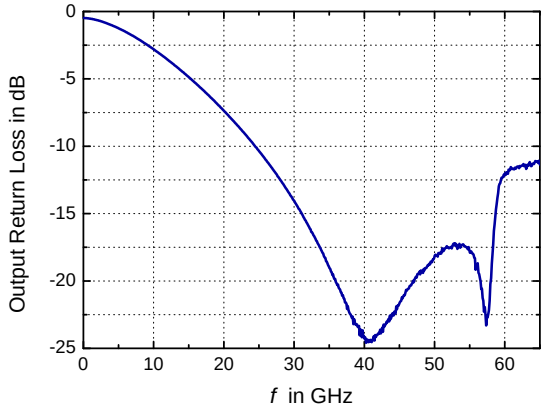
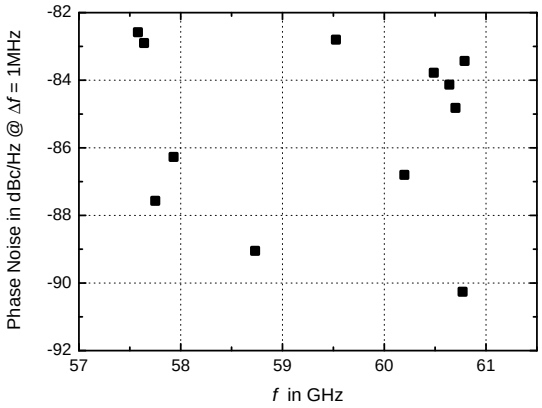


Figure 4.22: Output Return loss measured at one of the VCO outputs

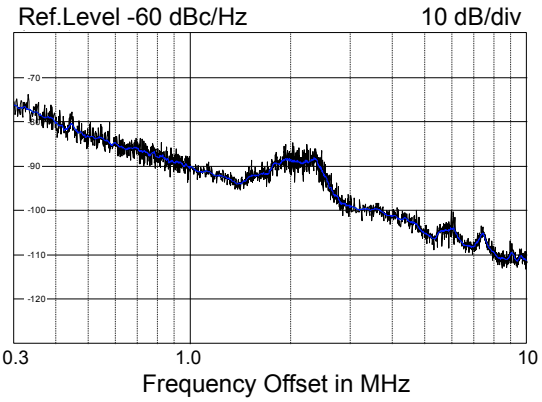
4.3.3.6 *Phase noise behavior*

While phase noise is not the key feature of the developed oscillator, it is important to achieve a sufficient spectral purity of the oscillator's output signal. Figure 4.23a shows the measured phase noise of the

VCO over its band of operation at 1 MHz offset from the carrier. The obtained performance varies from -82.5 dBc/Hz to -90.3 dBc/Hz.
Fig. 4.23b shows the phase noise at 60.77 GHz, where a maximum of -90.3 dBc/Hz at 1 MHz offset is achieved. The phase noise at 10 MHz offset lies around -112 dBc/Hz at this frequency. Around 2 MHz, a local peak can be observed, which is likely to originate from interference on one of the supply voltages.



(a) Phase Noise measured at different oscillation frequencies



(b) Phase noise at f_0=60.77 GHz from 300 kHz to 10 MHz offset from the carrier

Figure 4.23: Measured Phase Noise Characteristic of the VCO

4.3.4 *Conclusion on the VCO*

Table 4.2 on page 134 shows the performance of the implemented VCO in comparison to nanoscale CMOS VCOs that operate around 60 GHz found in literature. The best performance achieved in each column is highlighted.
As mentioned above, a large majority of the designs (which are exclusively differential) employ cross-coupled architectures. However, the best phase-noise performance of -100.3 dBc/Hz at 1 MHz offset is achieved by the common drain Colpitts VCO presented by K.W. Tang *et al.*, even though this oscillator works at a slightly higher frequency (77 GHz) than the others. The largest frequency tuning range of 17.8% is obtained by the VCO of C. Cao *et al.* due to the use of optimized AMOS varactors. The lowest power consumption, which is achieved by two designs, amounts to 2 mW. However, the corresponding publications

do not specify the output power of these VCOs: one may thus suspect that this performance is achieved at the expense of a quite low signal at the output.
To assess the ability of the VCO to convert DC power to mm-wave power, which is more meaningful than absolute power consumption or output power, the efficiency $P_{out,diff}/P_{DC}$ is also given in table 4.2. The VCO proposed in this thesis exhibits with -0.9 dBm not only the highest output power, but also consumes only 16.5 mW of DC power, thus achieving a record efficiency of 4.93%. This achievement is attributed to the differential common-source Colpitts architecture, which in this thesis was used for the first time to design a 60 GHz CMOS VCO.
Additionally, a Figure of Merit (FoM) is employed to compare the oscillator's performances. It is defined by

$$\mathrm{FoM} = -10\log_{10}\left[\left(\frac{f_0}{\Delta f}\frac{\mathrm{FTR}}{10\%}\right)^2 \frac{P_{RF}}{P_{DC}}\frac{1}{L[\Delta f]}\right], \tag{4.15}$$

where $L[\Delta f]$ is the phase noise at a Δf offset from the f_0 carrier and FTR is the tuning range given in %. In addition to the parameters taken into account by the conventional $\mathrm{FoM_T}$, the efficiency is also included in the above definition. This FoM allows to quite fairly compare the different implementations (at least if realized in a similar technology), because no kind of optimization is favored. The best design tradeoff, attested by a FoM of -175.7 dB, is achieved by the design of J.L. Gonzalez *et al.* which exibits a high efficiency while at the same time maintaining good tuning range and phase noise performance. The VCO presented in this thesis has a quite high FoM of -167.3 dB and thus realizes a state-of-the-art compromise if the focus is on high efficiency, as in the case of low power applications. The proposed VCO is published in [245].

Table 4.2: Performance comparison to CMOS VCOs found in literature

Reference	Techn. CMOS	Topol.	f_0 [GHz]	Ph. Noise[1] [dBc/Hz]	FTR [%]	P_{DC} [mW]	$P_{out,diff}$ [dBm]	$\frac{P_{out,diff}}{P_{DC}}$ [%]	FoM [dB]
H. Wang, 2001 [219]	250 nm	cc	50	-100	2.2	17	-9.5	0.66	-159
M. Tiebout, 2002 [225]	120 nm	cc	51	-90	2.75	10	-13	0.5	-149.9
F. Ellinger, 2004 [217]	90 nm SOI	cc	56	-92	14.7	21	-6.6	1.0	-170.3
Franca-Neto, 2004 [236]	90 nm	optimum pumping	64	-110 @ 10 MHz	N.A.	20	N.A.	N.A.	N.A.
R.-C. Liu, 2004 [216]	250 nm	cc	63	-85	3.97	119	-4	0.34	-148.2
T.-N. Luo, 2005 [226]	180 nm	cc	49	-96	1.47	4	-25.5	0.07	-141.6
K.W. Tang, 2006 [234]	90 nm	Colpitts[2]	77	**-100.3 @ 1 MHz**	8.1	38	-13.8	0.11	-166.6
D. Huang, 2006 [227]	90 nm	cc	60	-100.2	0.2	**2**	N.A.	N.A.	N.A.
C. Cao, 2006 [171]	130 nm	cc	56.5	-89	**17.8**	10	-10	1.02	-169.1
D.D. Kim, 2007 [220]	65 nm SOI	cc	70.2	-106.1 @ 10 MHz	9.55	10	-35	0.003	-137.4
S. Bozzola, 2008 [223]	65 nm	cc	54	-118 @ 10 MHz	11.5	7	N.A.	N.A.	N.A.
J. Borremans, 2008 [246]	130 nm	cc	62	-90	10	4	-15	0.811	-164.9
Z. Liu, 2008 [228]	130 nm	cc	64	-90.7	7.19	N.A.	-10	N.A.	N.A.
H.-K. Chen, 2008 [232]	130 nm	cc	68.8	-98.4	4.5	4	-11.3	1.72	-170.6
R. Genesi, 2008 [230]	90 nm	cc	53	-116.5 @ 10 MHz	3.77	**2**	N.A.	N.A.	N.A.
S. Sarkar, 2008 [81]	90 nm	cc	52	-95	6	20	N.A.	N.A.	N.A.
P. You, 2009 [247]	130 nm	cc	56	-95	3.9	14	-10	0.69	-160.2
C.W. Tsou, 2009 [229]	130 nm	cc	55.3	-93	7	8	-20	0.13	-155.7
H.-H. Hsieh, 2009 [224]	180 nm	cc	63	-89	1.06	55	-15	0.06	-133.1
M. Lont, 2009 [233]	65 nm	cc	63.3	-85	10.5	80	-13	0.06	-149.4
L. Li, 2009 [221] (see also [222])	90 nm	cc	64	-95	8.75	3	-11	2.51	**-174.0**
J.L. Gonzalez, 2009 [173, 231]	65 nm	cc	56	-99.4	17	25	-9.3	0.47	-175.7
VCO proposed in this thesis	65 nm	Colpitts[3]	59	-90.3	5.4	16.5	**-0.9**	**4.93**	-167.3

cc: cross-coupled, [1]at 1 MHz offset if not mentioned otherwise, [2]common-drain version, [3]common-source version

4.4 THE DOWN-CONVERSION MIXER

In a 60 GHz direct conversion receiver, the transposition of the signal from the 60 GHz band to the baseband is done in one single step. Thus, the down-conversion mixer is of special importance. Its design is described in this section.
In the case of a mixer, the power consumption, which has to be minimized for all circuits designed in this thesis, consists of two parts: the dissipated DC power P_{DC} and the local oscillator power P_{LO}. As the latter is more expensive in the sense that it takes much more DC power to create the same amount of LO power due to the low efficiency of mm-wave CMOS oscillators and power amplifiers, the foremost goal of low power mixer design is to minimize P_{LO}.
As in the case of the LNA, the Friis equation [146] also governs the design of down-conversion mixers. While the gain of the LNA hides the noise figure of the remaining system to a large part, a huge noise figure of the subsequent stages cannot be tolerated. Thus, not only the mixer's noise figure has to be optimized, but it should also provide some gain. If, however, the down-converter exhibits conversion loss, the noise figure of the baseband stages attains importance according to the Friis equation. Hence, while suitable for upconverters, the use of mixers exhibiting conversion loss should be avoided at the receiver side (at least in the case where the NFs of active and passive mixers are comparable).
Linearity is also an issue in mixer design: As illustrated in section 2.5.1, the receiver blocks closer to the output must be more linear, as the received signal has already been amplified by the preceding stages.
The requirement of high LO-to-BB isolation is less problematic under the given circumstances: because the LO frequency range is far from BB, a strong attenuation of the LO signal is easy to ensure as both the mixer output stage and the BB amplifiers act as low pass filters.

A multitude of different architectures can be employed for 60 GHz mixers in CMOS technology. The realizations found in literature accomplish different compromises between the various requirements given above:

- The early implementation by S. Emami *et al.* in 2005 uses a quadrature balanced single gate architecture [248], which exhibits -2 dB conversion loss.
- The simple unbalanced dual-gate implementations in [249] and [250] neither provide good isolation nor conversion gain.
- The various passive implementations in [188, 251–254] either require considerable LO power, or exhibit high conversion loss. As the latter drawback is less of a problem for transmitter circuits, passive architectures are better suited for the up-converter side, where a high output linearity is mandatory.
- Several other architectures are implemented in [255–258], mostly also limited due to low conversion gain values.
- The down-converters with properties most suitable for the receiver front-end in this thesis are the different flavors of the Gilbert cell [259]. 60 GHz CMOS implementations using double balanced

[260–262], half [67, 263] or sub-harmonic [264] Gilbert cells can be found in literature. All of these realizations exhibit at least moderate conversion gain, while some of them are also optimized with respect to power consumption. Due to the balanced nature of this architecture, high isolation is feasible, if the layout is symmetric and well balanced differential signals are applied.

The down-conversion mixer designed in this thesis employs a single balanced, half Gilbert cell. This architecture is selected due to its potential to realize an excellent compromise between the various requirements discussed above. A double balanced Gilbert cell is not necessary, because the LNA provides a single-ended output and good isolation can be achieved by low-pass filtering.
To facilitate the characterization of the circuit, a passive LO balun and a differential BB output buffer to drive a $2 \times 50\,\Omega$ output are integrated with the standalone version of the mixer.

The following sections illustrate the design of the mixer circuit (including buffer) and give its measured performance. The comparison to published down-mixers given in section 4.4.5 shows that it exhibits the lowest LO power requirement (-5 dBm) and circuit size (0.25 mm^2) of all mixers found in literature and at the same time provides a maximum of 9.1 dB of conversion gain and a RF bandwidth reaching from 54 GHz to at least 65 GHz. It thus realizes a better compromise that any other downmixer found in literature for the requirements given in this thesis.

4.4.1 *Circuit Overview*

Figure 4.24 gives the block diagram of the designed mixer. The RF input port is single-ended, because the preceding circuit block in the receiver is the single-ended low noise amplifier presented in section 4.2. The differential IF output of the mixer (which actually corresponds to the baseband output, as the intermediate frequency is zero in a direct conversion architecture) is connected to a buffer amplifier based on a differential pair. The design of this BB buffer is detailed in subsection 4.4.3. The buffer is optimized to drive a differential 100 Ω load (or alternatively two grounded 50 Ω terminations). The total circuit's power consumption is dominated by this buffer, which dissipates around 14 mW. In an integrated receiver circuit, this kind of power-wasting

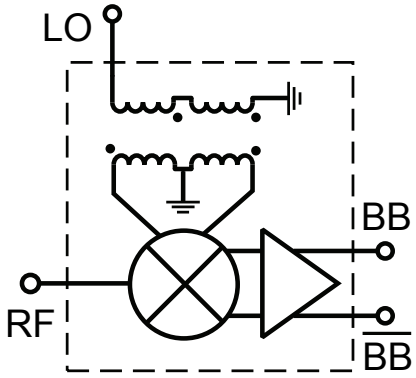
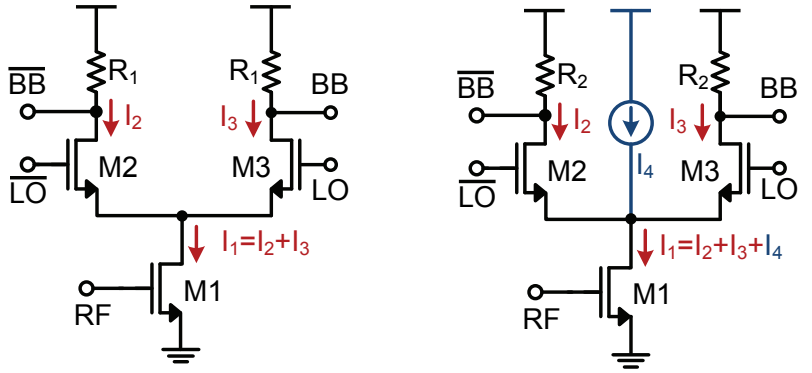


Figure 4.24: Block diagram of the downconversion mixer with integrated LO balun and baseband buffer

buffer is not necessary, because higher load impedances can be employed.
The differential LO port of the mixer core is connected to a passive on-chip balun. The balun is composed of two symmetric spiral transformers connected as indicated in figure 4.24. Its layout can be identified in figure 4.29, where the balun is connected to the LO input pad by an inductor that resonates the pad capacitance. The employed balun topology allows a much better amplitude and phase balance compared to a single transformer with center tap. For further details on the balun refer to section 3.4.5.2 of chapter 3.

4.4.2 *Design of the Mixer Core*

The proposed mixer core is based on the very common single-balanced multiplier-based mixer given in figure 4.25a. This circuit is often referred to as "half Gilbert cell". It first converts the RF input voltage to a current by the transconductance transistor M1. The multiplication then takes place in the current domain [133]: The switching pair, which consists of the LO-driven transistors M2 and M3, switches the current from one side of the circuit to the other one. At the output, the BB signal is available is differential form.



(a) Conventional half Gilbert cell

(b) Current bleeding with ideal current source

Figure 4.25: Half Gilbert cell with and without current bleeding

However, the conventional version of this mixer has several drawbacks: because the transistors M2 and M3 have to carry the entire bias current of M1 (which has to be large to ensure high gain and linearity), they inject a large amount of noise to the output and switch only slowly, thus wasting part of the RF current as common mode component [67, 265]. In addition to that, and since voltage headroom is limited, the load resistors R_1 in figure 4.25a need to be quite small to limit the voltage drop among them. This results in low conversion gain.
A remedy to the issues listed above is the use of the current bleeding technique [265], which is also known under the name of charge injection [266]. Its principle is illustrated in figure 4.25b: due to the insertion of a current source in parallel with the switching pair, the part I_4 of the bias current of the transconductance by-passes the upper transistors and the load resistors. Thus, independent transistor biasing is possible. This allows for a high transconductance of M1, fast switching of and less noise injection by transistors M2 and M3, and high conversion

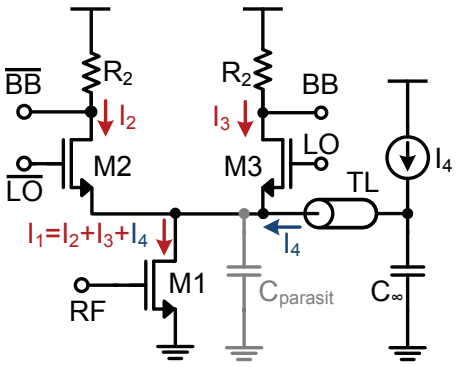


Figure 4.26: Current bleeding as proposed by B. Razavi [67]

gain due to larger load resistors R_2. While only a fraction of the total bias current of M1 is passing the switching pair, the entire RF current generated by the transconductor is switched by M2 and M3, as the DC current source is of high impedance for these small-signal currents.
A second benefit of this technique, which is very welcome in low power designs, is that the LO power necessary to drive the switching pair can be reduced due to the small widths of the transistors M2 and M3.

A remaining issue in the circuits of figure 4.25, especially if working close to the transistor's cutoff frequency, is the total parasitic capacitance $C_{parasit}$ present at the common terminal of the three transistors. This capacitance would even increase, if a real current-source was employed for charge injection at this point. It short-circuits a part of the RF current generated by the transconductor to ground, thus reducing the current that is commuted by the switching pair.
B. Razavi proposes in [67] to use a transmission line inductor to resonate $C_{parasit}$ at the mixer's operating frequency as illustrated in figure 4.26. This creates a high impedance that absorbs $C_{parasit}$ and hides the source of the bleeding current. The capacitance C_∞ provides a RF short-circuit to ground. In addition to the benefits of current bleeding, this special type of current injection further increases conversion gain.

Based on the considerations above, the circuit in figure 4.27 is proposed as down-conversion mixer in this thesis. Rather than using a current source for current bleeding, the current $I_B = 1.4\,mA$ which by-passes the switching pair is set by the resistor $R_B = 367\,\Omega$. It passes by the spiral inductor $L_B = 121\,pH$, which at the same time resonates the parasitic capacitance present at the drain of M1 at 60 GHz. The capacitance $C_B = 200\,fF$ is taken into account to accurately determine the resonance frequency.
The transistor M1 is biased at the minimum noise current density of 0.15 mA/µm. Its width is 14x1 µm. M1 is degenerated by the inductor $L_D = 73\,pH$. This improves linearity and allows a simultaneous noise and power match at the input. Inductors $L_2 = 15\,pH$, $L_3 = 121\,pH$ and $L_4 = 200\,pH$ realize this input match (taking into account also the pad capacitance) over a wide bandwidth. (For more details on inductive source degeneration refer to section 3.6.3 of chapter 3.)
Transistors M2 and M3, which are 35x1 µm wide, are biased at very low current densities to allow fast switching. The inductor $L_1 = 156\,pH$ is used to match the gates of the switching pair to the balun's impedance.

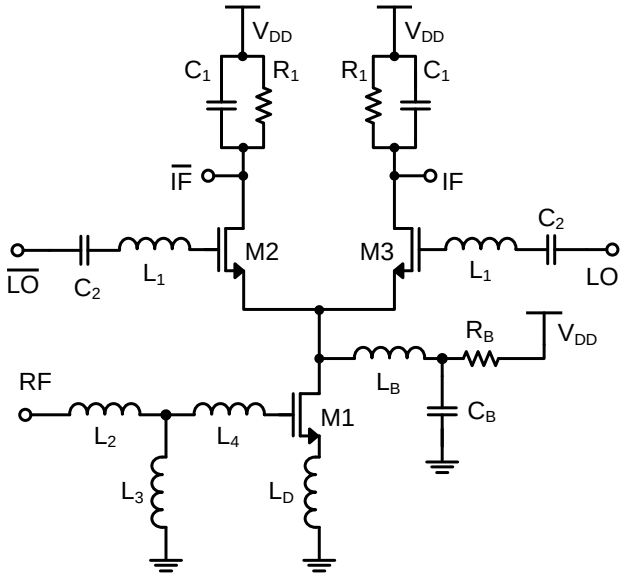


Figure 4.27: Simplyfied schematic of the mixer core without biasing details

The capacitor $C_2 = 200\,\text{fF}$ is inserted to cut the DC path and permit the application of a bias voltage at the gates of M2 and M3.
The resistive loads $R_1 = 395\,\Omega$ are short-circuited by $C_1 = 338\,\text{fF}$ for RF and LO frequencies, which considerably improves conversion gain G_C, linearity and isolation.

4.4.3 *Design of the Baseband Buffer*

In order to allow the mixer output to drive a $2 \times 50\,\Omega$ load, a differential BB buffer is employed. Figure 4.28 shows the schematic of this buffer. The chosen circuit is based on a conventional differential pair [154]. To allow DC-coupling between mixer core and amplifier input, the biasing is done using a simple current mirror. The transistors M1, which is of gate width $W_1 = 18 \times 10\mu\text{m}$, and its scaled version M1′ are of gate

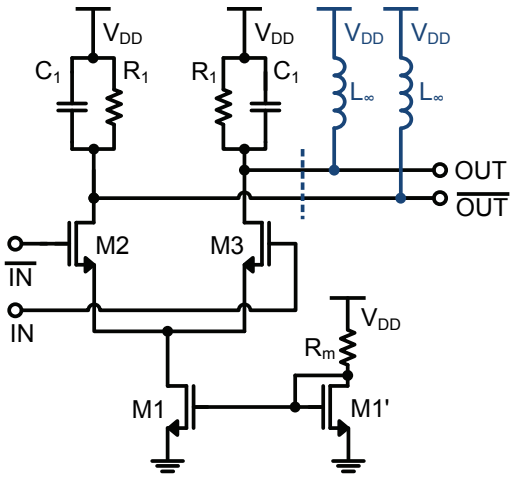


Figure 4.28: Differential pair serving as baseband buffer for the down-converter output

lengths $L = 180\,nm$ to increase the transistor's output resistance r_0. The tail current of $14\,mA$ is set by $R_m = 545\,\Omega$.
The upper transistors M2 and M3 are of $35 \times 1\,\mu m$ gate width and biased for maximum f_{max} at a current density of $0.2\,mA/\mu m$. Like in the other parts of this thesis, LVT GP devices are employed.
The baseband load impedance consists of two parts:

- On-chip, the resistors $R_1 = 94\,\Omega$ realize, together with the output impedance of the transistors M2 and M3, a $50\,\Omega$ impedance in the baseband frequency range. The parallel capacitances $C_1 = 78\,fF$ are negligible at BB frequencies, but increase the rejection of the LO and RF signal.
- Off-chip, the inductors L_∞ can be added by bias-Ts. They allow to inject the bias current without voltage drop, thus permitting a DC voltage of $V_{DD} = 1\,V$ at the drains of M2 and M3. Due to their large values they do not change the load impedance at signal frequencies.

4.4.3.1 *Fabricated Circuit*

Fig. 4.29 shows a photo of the circuit fabricated in STMicroelectronics 65 nm CMOS technology. A very small, pad limited die size of only 0.49mm x 0.52mm = $0.255mm^2$ is obtained, which is further reduced when integrating the mixer into the receiver.
The layout symmetry that is necessary to obtain good RF-to-BB isolation can be observed at the mixer core. Furthermore, the transmission lines that connect the core to the BB output are of exactly the same length (even though perfect symmetry is not feasible, because the balanced output needs to be routed to one side of the chip). As LO and RF signals are single-ended, no symmetry is observed at the associated signal paths.

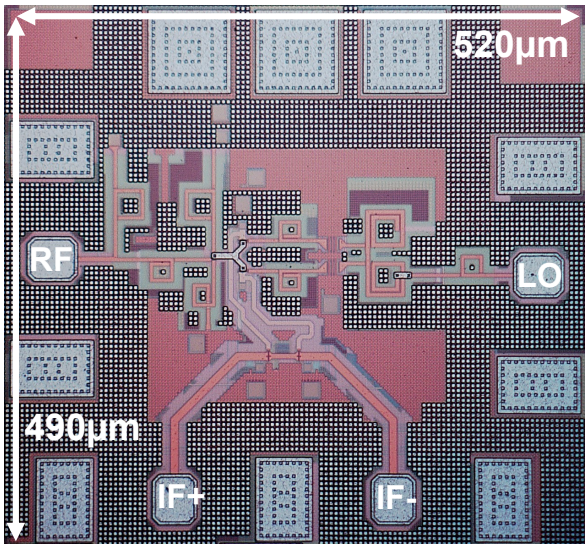


Figure 4.29: Die photo of the fabricated down-mixer

4.4.4 *Results*

The mixer circuit of figure 4.29 is measured on-wafer up to 65 GHz. The return loss is determined using an Anritsu ME7808A VNA. The LO signal is generated by an Agilent E8257D source that provides up to 14 dBm output power at 60 GHz.
Power conversion gain and power sweep measurements are done using the VNA as RF signal source and connecting a Rohde & Schwarz FSU 67 GHz spectrum analyzer to one of the BB ports, while terminating the other one. All loss originating from cables and probes is subtracted from the obtained results, and 3 dB are added to the BB output power to account for the differential signal.
While measuring, the mixer is biased at the current densities fixed during design. The bias of the switching pair depends on the LO power and is set to 0.7 V for the LO power sweep. For the other measurements, P_{LO} equals -1 dBm and the switching pair is biased at 0.56 V. The circuit including buffers is drawing 16.8 mA from a 1 V supply, from which only 2.8 mA are attributed to the mixer core.

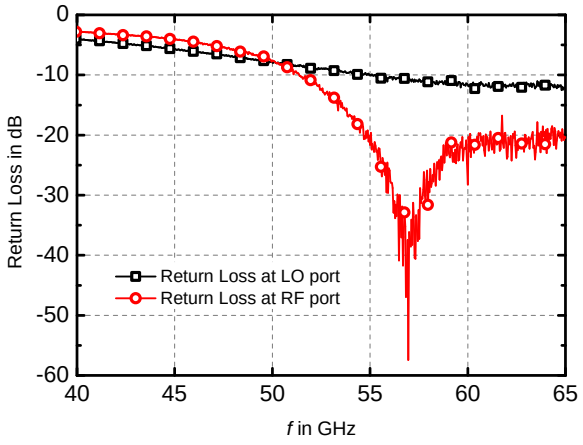


Figure 4.30: Measured return loss at LO and RF port

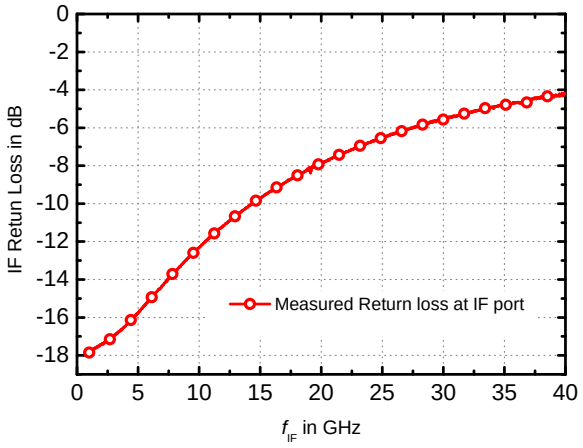


Figure 4.31: Return loss measured at one of the baseband outputs

4.4.4.1 *Return loss*

Figure 4.30 illustrates the measured Return Loss (RL) at the RF and LO ports. An excellent broadband match is ensured, contributing to a very flat, wideband response of the mixer: The LO return loss stays below -10 dB from 55 GHz to at least 65 GHz, while the RF RL stays below -20 dB within the same band.
Figure 4.31 shows the measured BB return loss. It stays below -15 dB from DC up to 5 GHz.

4.4.4.2 *Conversion gain*

The LO power is swept for $f_{LO} = 60$ GHz and $f_{RF} = 61$ GHz to find the value that achieves maximum conversion gain G_C. According to figure 4.32, this is the case at the low LO power value of -5 dBm.
Figure 4.33 plots the conversion gain G_C in the Lower Sideband (LSB) and Upper Sideband (USB). A very flat, wideband response can be observed for IF frequencies of 1 GHz and 2 GHz, while both sidebands are very symmetric. The conversion gain is around 6 dB at 1 GHz from

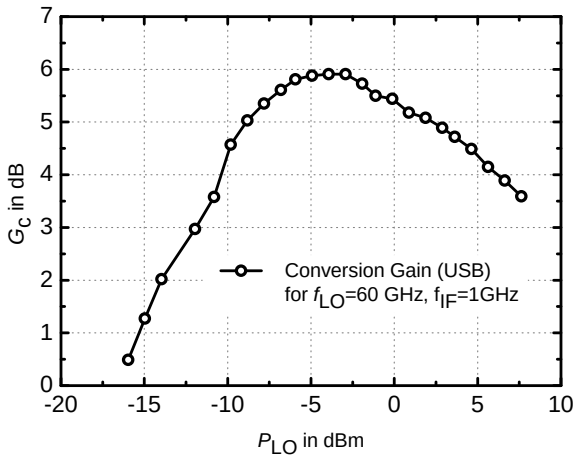


Figure 4.32: Measured conversion gain versus LO power at $f_{LO} = 60$ GHz and $f_{IF} = 1$ GHz from the upper sideband

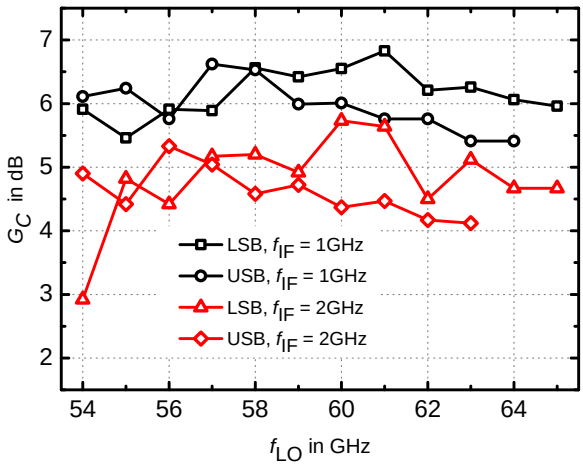


Figure 4.33: Conversion gain G_C versus LO frequency for two different intermediate frequencies, both in upper (USB) and lower sideband (LSB).

the carrier over the whole band. The measurement frequency range was bounded to below 65 GHz due to the used measurement equipment. Figure 4.34 shows the conversion gain for five fixed LO frequencies while sweeping the RF over both sidebands. The peak in G_C is achieved close to the carrier, while the 3 dB BB bandwidth is around 2 GHz (i.e. 4 GHz of band around the LO frequency).

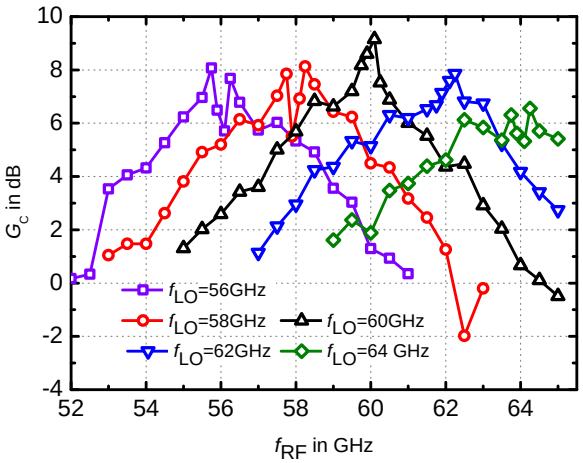


Figure 4.34: Conversion gain G_C versus f_{RF} for different LO frequencies. The IF is varying from 100 MHz to 5 GHz.

4.4.4.3 *Linearity*

Figure 4.35 plots BB output power and conversion gain versus input power to illustrate the linearity of the circuit. An output referred 1 dB compression point OP_{-1dB} of -5 dBm is obtained for $P_{LO} = -1$dBm.

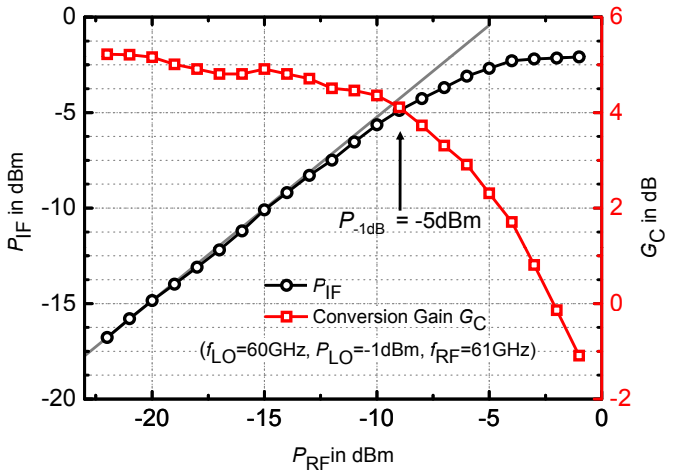


Figure 4.35: P_{IF} and G_C versus P_{RF} to illustrate nonlinearity and 1 dB compression point

4.4.4.4 *Other characteristics*

Isolation is less important for this mixer, due to the distance from baseband to LO/RF which allows inexpensive low pass filtering on-chip. LO-to-BB isolation is observed to be around 30 dB, while RF-to-BB

isolation is around 28 dB. The latter value is expected to increase if an integrated differential oscillator with even better phase balance provides the LO signal. Furthermore, a double-balanced architecture should be employed if these isolation values are not sufficient.
The simulation of the noise figure using SPECTRE RF shows a Double Sideband (DSB) value of around 9 dB, which gives a theoretical single sideband value that lies at 12 dB. Measurement results are expected to be very close due to the use of BSIM4 models and the fact that all parasitics are taken into account during simulation.

4.4.5 *Comparison to the State of the Art*

Table 4.3 compares the presented work to 60 GHz CMOS mixers found in literature. The proposed mixer has the smallest chip size, one of the highest gain values and a very wide BB and RF bandwidth. The fact that its DC power consumption is relatively high originates from the BB buffer that drives two 50 Ω loads. This buffer alone consumes 14 mW. On the other hand, the proposed mixer requires the lowest LO of all mixers given in table 4.3. This allows its use in very low power front-ends, because both the oscillator and the LO buffer can be dimensioned for lower output power than in the case of mixers that require larger LO signals.
Concerning noise figure, the proposed mixer realizes a good (simulated) value. However, a meaningful comparison to the state of the art is not possible, because most publications do not give any NF. The few given simulated NFs still need to be confirmed by measurements.

4.4.6 *Conclusion on the Downconverter*

The proposed single-balanced down-mixer is the perfect choice for the low-cost low-power direct conversion receiver targeted in this thesis due to its conversion gain of up to 9.1 dB, its moderate DSB noise figure of 9 dB and its high OP_{-1dB} of -5 dBm. Its ultra-wide bandwidth respects the channel requirement of all worldwide standards for the unlicensed 60 GHz band. The very small (pad-limited) size of only 0.49×0.52 mm^2 and the low LO power requirement of -5 dBm are record values with respect to the state of the art and allow to build a low-power low-cost receiver front-end.
Key points during mixer design were the use of spiral inductors for matching, the inductor-based current-bleeding technique to achieve high gain and low LO power, and the simultaneously noise and power-matched input.
The presented down-conversion mixer is published in [268].

Table 4.3: Comparison of published 60 GHz down-conversion mixers in CMOS

Ref.	Topol.	Techn. [nm]	IF [GHz]	RF [GHz]	G_c [dB]	NF (DSB) [dB]	P_{LO} [dBm]	OP_{-1dB} [dBm]	P_{diss} [mW]	Area [mm²]
S. Emami, 2005 [248]	single gate	130	2	55-61	-2	8.5[1]	0	-5.5	2.4	2.7
B. Razavi, 2006 [67]	half Gilbert cell	130	N.A.	60	12[1,2]	15[1]	N.A.	N.A.	0.9	N.A.
Motlagh, 2006 [251]	resistive	90	2-9	56-64	-11.6	N.A.	4	-7.5	0	4
I.C.H. Lai, 2006 [249]	dual gate	90	4	60	-1.2	N.A.	0.5	-1.7	29.4	0.49
J.H. Tsai, 2007 [260]	Gilbert cell	90	0.01	25-75	3 ± 2	N.A.	6	-4	93	0.3
Zhang, 2007 [261]	Gilbert cell	130	1	55-63	3	N.A.	0	-12	N.A.	0.81
Kantanen, 2008 [252]	resistive	90	0.4	60	9.8	N.A.	5	-2	14	0.77
J.H. Tsai, 2008 [264]	Subh. Gilbert cell	90	0.1	30-300	1.5 $\pm$1.5	N.A.	10	-10.4	58	0.35
Shahroury, 2008 [255]	current mode	130	2	57-63	1	7[1]	0	+2	3.6	1.46
C.H. Lien, 2008 [256]	gate pumped	130	4.5	58-65	0.5	8.5[1]	3	-5.5	7.5	0.56
D.H. Kim, 2009 [263]	half Gilbert cell	130	5	60	4.9	N.A.	N.A.	-15	8.2	N .A.
P. Sakian, 2009 [262]	Gilbert cell	65	0 - 1.3	60	4	9	N.A.	N.A.	6	N.A.
C.Y. Wang, 2009 [257]	bulk driven	130	0.5	51-65	1	16.5[1]	3	-18	3	0.45
R.E. Amaya, 2009 [267]	single gate	130	2.4	60	0.3	10.8	0.5	2.3	14.4	1.4
H.C. Kuo, 2009 [250]	dual gate	130	5	60	-2.7	18.5	0	-10.7	16.8	0.9
H.Y. Yang, 2009 [253]	distrib. drain	130	0-2	0.8-77.5	-5.5	N.A.	10	-8.5	0	0.39
C.H. Lien, 2010 [258]	gate pumped	130	0-3	53-67	0	N.A.	5	-10	14	0.53
D.Y. Jung, 2010 [188]	resistive	130	5.8	56-63	-6.3	N.A.	0	-11.8	0	0.49
M. Ercoli, 2010 [188]	passive	65	0	50-70[1]	-6.9[1]	8.4[1]	-5[1]	N.A.	15[1]	N.A.
proposed mixer	**half Gilbert cell**	**65**	**0-2**	**54 - 65**	**9.1**	**9***	**-5**	**-5**	**16.8**	**0.25**

[1] simulated, [2] voltage conversion gain

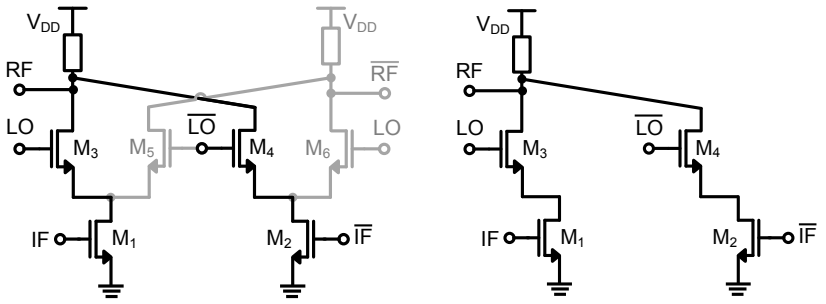
4.5 THE UP-CONVERSION MIXER

When research on 60 GHz CMOS circuits started, it focused on demonstrating receiver front-ends. Thus, down-conversion mixers were in the center of interest: as illustrated in section 4.4, a variety of different CMOS down-converters for the 60 GHz band can be found in literature. Meanwhile, fully integrated 60 GHz CMOS transceivers are designed, fostering the research on up-conversion mixers, where noise figure and conversion gain are less and linearity more of an issue. The first 60 GHz CMOS up-mixers were published in 2007. The double-balanced Gilbert cell [259] is the most popular topology, providing excellent isolation and requiring low LO power. It is employed in [48, 269–272]. Passive resistive mixers have also been implemented [273, 274]. They show very high linearity and consume no DC power, while requiring a high-power LO drive and exhibiting considerable conversion loss.
A particular technique that has been used for up-conversion to the 60 GHz band in [275, 276] is subharmonic mixing: it is explained in detail in section 2.4.8 of chapter 2.

The direct up-conversion mixer implemented in 65 nm CMOS in the framework of this thesis utilizes a balanced dual-gate [277–279] topology. While having been demonstrated for simple unbalanced *down-converters* at 60 GHz (e.g. [249, 250]), to the knowledge of the author this architecture has never been used in CMOS up-conversion mixers for the 60 GHz band.

4.5.1 *Preliminary Considerations*

The requirements on the up-conversion mixer are low-power consumption (and thus, to obtain a low overall transceiver power consumption, also low required LO power), good linearity and low conversion loss. Its IF bandwidth has to exceed the channel bandwidth defined by the 60 GHz standards (i.e. from DC to around 1 GHz, because the IF bandwidth is doubled due to direct up-conversion). The RF bandwidth should cover the whole unlicensed band from 57 GHz to 66 GHz. Furthermore, LO and RF rejection is an important issue.



(a) Gilbert Cell [259] (b) Double-balanced dual-gate mixer

Figure 4.36: Comparison of Gilbert cell (differential output) to dual gate mixer (single-ended output)

A very common solution to meet these requirements is a fully balanced up-converter topology like the Gilbert cell [259], which is given in figure 4.36a. It requires differential IF and LO signals to generate a differential

RF output, at which both input signals are canceled, achieving good isolation. This topology uses at least six transistors and requires a crossing of two signal lines to allow the combination of all signal-parts at the outputs.
However, the block diagram of the planned transmitter front-end (figure 2.19 in section 2.5.1, page 44) shows that the output of the up-conversion mixer only needs to be single-ended, because the subsequent circuit parts are implemented that way. Thus, either a balun needs to be used to convert the differential output of the Gilbert cell to a single-ended one, or, as illustrated in figure 4.36, the Gilbert cell can be simplified by removing two transistors and the signal cross-over (drawn in grey). This measure simplifies the circuit, maintains the canceling of the IF and LO signals at the (now single-ended) output, and avoids the use of a balun (that would introduce loss and imbalance). The result is the double-balanced dual-gate mixer [277] given in figure 4.36b.
However, the working principle of the mixer changes fundamentally: in the Gilbert cell, the amplitude of the current passing through the transconductance transistors M1 and M2, is, in the ideal case, not influenced by the LO signal. Transistors M1 and M2 work in saturation all the time. By the LO-driven switching stages, their drain current is switched from one output arm to the other. This commutation produces the up-conversion. It relies on the nonlinearity of the switching quad, whose transistors switch from cut-off to saturation [279].
In the dual-gate mixer, the drain current of the transconductance stages is necessarily influenced by the switching stage: as illustrated in figure 4.36b, each of the transconductance transistors M1 and M2 is connected to only one upper transistor, either M3 or M4. If the upper transistor is not passing the current which the transconductance transistor tries to impose, this current has to be reduced. This reduction is done by forcing the lower transistor to enter triode region. Thus, rather than commutating the IF current, the LO signal modulates it via the drain potential of the lower transistor. The transistors M_1 and M_2 are switching back and forth from saturation to triode region [278].

In the following, the design of a balanced dual-gate mixer according to figure 4.36b is described. In addition to the fact that it exactly meets the front-end requirement of providing a single-ended output from differential IF and LO signals, A. Verma *et al.* [278] showed that it can provide higher linearity than a comparable Gilbert cell.

4.5.2 *Mixer Design*

4.5.2.1 *Overview of the mixer circuit*

As mentioned in the previous section, the up-conversion mixer exhibits differential inputs and a single ended output. While these interfaces are adjusted for the integration of the mixer in the transmitter front-end, they are not suited for characterization of the standalone mixer. In addition to that, the output port needs to drive a $50\,\Omega$ load, and the inputs should also be matched to $50\,\Omega$. Thus, the mixer core (whose design is described in subsection 4.5.2.2) must be surrounded by buffers and single-ended to differential converters as illustrated in figure 4.37.

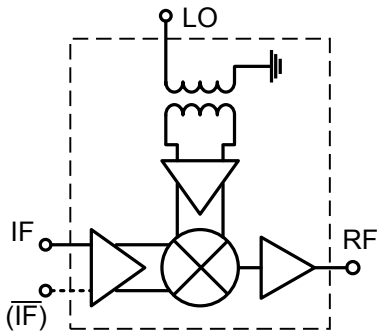


Figure 4.37: Mixer breakout comprising IF, LO and RF buffers and an LO transformer balun.

At the LO port, a single-ended to differential conversion is necessary, because synthesizers for the 60 GHz band usually provide only asymmetric signals. To this end, a single-coil transformer balun is integrated at the LO input port. An additional differential LO buffer amplifier to compensate the loss of the balun and to further balance the differential signal is added. Its design is described in subsection 4.5.2.4.
At the IF input, the possibility of using either single-ended or differential signals is desired. As the IF input of the mixer requires a well balanced differential signal, even if the externally applied signal is asymmetric, a differential IF buffer amplifier with high common-mode rejection is added. If a single-ended signal is applied at the IF input, the IF buffer acts as active balun. It is described in subsection 4.5.2.3.
A RF buffer amplifier is also added to the output of the mixer to drive a 50 Ω load. It is detailed in section 4.5.2.5.

4.5.2.2 *The dual-gate double-balanced mixer core*

In the classical version of a (single-ended) dual-gate mixer, only one *dual-gate* device is necessary [277]. It consists of a MOS transistor with two distinct gate terminals, allowing the design of simple one-device mixers with separate IF, RF and LO ports. The dual-gate device can be represented by two transistors in cascode. The advantage of using a single dual-gate device in an integrated mixer circuit is the minimization of interconnect parasitics. However, the channel width W of this transistor is chosen as a compromise between the requirements for the upper and lower transistor width.
To avoid this compromise, a cascode using two transistors of different channel width is utilized here to constitute the dual-gate device [278]. Like in the cascode LNA presented in section 4.2, an inductor L_M is inserted between the two transistors [156]: together with the parasitic source-bulk and drain-bulk capacitances it forms an artificial transmission line that absorbs these parasitic capacitors.
Figure 4.38 illustrates the schematic of the proposed balanced dual-gate up-mixer using these kind of cascodes. The lower transistors M_1 and M_2 are with 32×1.6 µm twice as wide as the upper transistors M_3 and M_4, which are of 26×1µm width. The larger lower transistors achieve a high transconductance and thus increase conversion gain, while the more narrow upper transistors exhibit less parasitics and thus allow a faster variation of their source potential. Simulations show that for these transistor sizes, a middle inductor of $L_M = 87$ pH is well suited.
As mentioned during the preliminary considerations, the working prin-

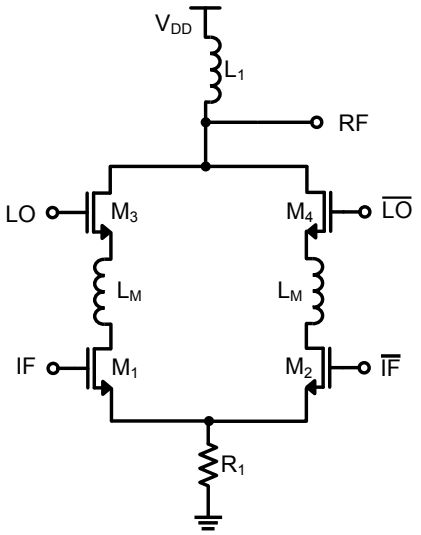


Figure 4.38: Schematic of the dual-gate mixer core (without biasing)

ciple of the dual-gate mixer fundamentally differs from the Gilbert cell [278, 279]: in order to allow the upper transistors to modulate the drain current of the lower transistors, a variation of the drain potential of M_1 and M_2 has to have maximum influence on their drain current. Hence, they have to be biased in or at the edge to triode region. This is achieved by setting the gate bias voltage of M_3 and M_4 to a low potential. Here, $V_{G,3/4}$ is fixed to 750 mV by means of a resistive voltage divider. This pushes also the drain potential of M_1 and M_2 further down, thus making them approach triode region. At the same time, the upper transistors have sufficient voltage headroom to ensure operation in saturation region.

The current density in the two arms of the mixer is chosen to be much lower than in the other designs of this thesis: rather than optimizing the high frequency behavior, this decreases channel length modulation and thus maximizes the gain per drain current for M_1 and M_2. Hence, the mixer core draws only about 1.2 mA from a 1 V supply voltage. Alternatively, biasing at higher current densities (but still at the edge to triode region for the lower transistors) is an option if power consumption is less of an issue.

To allow for very low IF frequencies at the gates of the transistors M_1 and M_2, their gate bias voltage is not capacitively decoupled from the signal. Thus, the DC voltage at the output of the IF buffer stage has to serve as bias voltage for the mixer core. To maximize voltage swing, the bias voltage must be about half the supply voltage, which is hard to achieve when using very wide LVT transistors. Thus, HVT transistors are employed for M_1 and M_2. Due to their higher threshold voltage, a gate bias voltage of around 400 mV becomes feasible. This voltage is present at the output of the IF buffer due to the fact that its load resistor and output current are chosen accordingly.

The gate bias voltage of the lower transistors further increases due to the tail resistor R_1. It is added at the sources of transistors M_1 and M_2 to increase the common mode rejection of the differential input signals. The load inductor $L_1 = 43$ pH, which is added at the drains of the upper transistors, is part of the network that matches the output of the

mixer core to the input of the RF buffer. Its low inductance value shows that the interface from mixer to RF amplifier is of low impedance.

4.5.2.3 *The IF buffer with active balun*

The IF buffer stage is shown in Fig. 4.39. It is based on a two stage differential amplifier with improved common mode rejection.

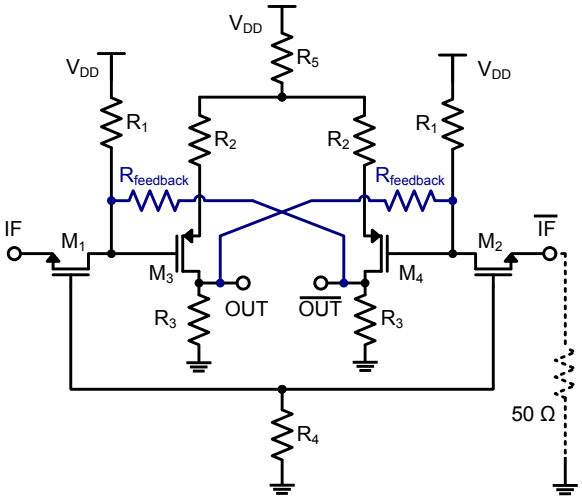


Figure 4.39: Simplified schematic of the IF buffer / active balun

The input stage is realized as a common-gate amplifier consisting of the transistors M_1 and M_2 and the load resistors R1. R_4 is part of the gate bias network (the lower terminal of R_4 is at AC-ground only) and increases common mode rejection. A common-gate amplifier is employed because it allows to easily realize a broadband impedance match to $50\,\Omega$ by sizing the transistors accordingly. The input impedance of the common gate amplifier can be approximated by [154]

$$R_{IN} \approx \frac{1}{g_m} + \frac{R_1}{1 + g_m r_0}, \tag{4.16}$$

if bulk and source contact are connected. While the second part of this equation is often neglected, in 65 nm CMOS it can become quite large due to the low intrinsic gain $g_m r_0$. In the present case, R_1 is chosen to be $170\,\Omega$ and the transistor width is $35 \times 1\mu m$ to achieve $50\,\Omega$ at each one of the two inputs. This resistance is about equally split between the two parts of equation (4.16). The pad capacitance in parallel to the $50\,\Omega$ load, as well as the interconnect parasitics which need to be taken into account for matching at 60 GHz, can be neglected at the IF.
The second amplifier stage is made of the p-channel MOS transistors M_3 and M_4 used in a common-source configuration. The transistors are $60\,\mu m$ wide. The load resistors R_3 have a value of $900\,\Omega$, while the resistors $R_2 = 170\,\Omega$ are used for source degeneration to linearize the amplifier and $R_5 = 260\,\Omega$ improves common mode rejection. P-channel transistors are employed to realize a lower output common-mode voltage, which is used to bias the mixer input.
Throughout the entire IF amplifier stage no coupling capacitor is used. This allows a response down to DC, however implies that the output of one stage has to bias the subsequent stage. This is also true for the interface between IF buffer and mixer core. Hence, the values of the

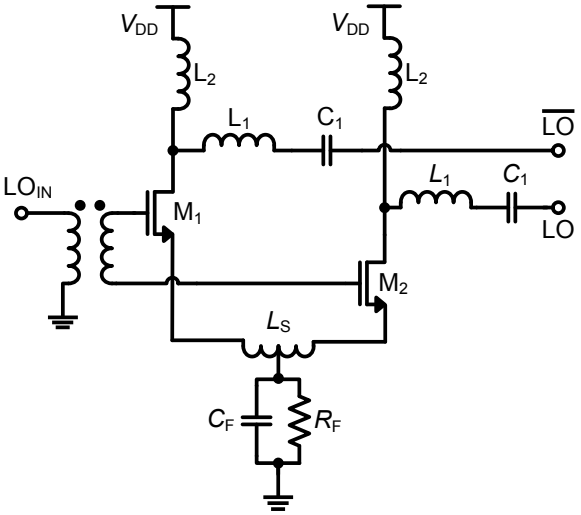


Figure 4.40: Differential LO buffer amplifier with transformer balun at the input

employed resistors have to satisfy both bias and AC-behavior requirements.
In order to improve common mode rejection up to a point where the buffer can be used as a active broadband balun (with the second input matched to $50\,\Omega$ as indicated in figure 4.39), cross-feedback is introduced from the output of the second stage of one arm to the input of the second stage of the other arm by the resistors $R_{feedback} = 550\,\Omega$. Because the second stage inverts the signal, this measure helps to balance the outputs of the IF buffer.

Due to the use of large input transistors and small load resistors R_1, which are necessary to obtain a broadband input match to $50\,\Omega$, the IF buffer has a simulated power dissipation of around 6.7 mW. It achieves a voltage gain of about 4 from a single input to the differential output. Due to the use of resistive loads that are necessary to obtain a very broadband behavior, the limitation of the output voltage to 1 V also sets a fundamental limit to the buffer's linearity: the simulated input-referred -1 dB compression point is thus -11.3 dBm.

4.5.2.4 *The LO buffer with passive balun*

The upper transistors of the mixer core need to be driven by a differential LO signal with high power and very good phase and amplitude balance. The first step to generate such a signal from an externally applied single-ended LO signal is the use of a single-ended to differential converter. It is realized by the single-coil transformer balun introduced in section 3.4.5.1 of chapter 3.
However, the signal at the output of this balun should not be directly applied to the mixer input, because it suffers from considerable amplitude and phase imbalance (see section 3.4.5.1 of chapter 3). Thus, the differential LO buffer amplifier shown in figure 4.40 is added. Besides balancing the signal, it also improves the matching to the input of the mixer core transistors.
The LO buffer transistors M_1 and M_2 are $26 \times 1\mu m$ wide and biased at the peak f_{max} current density of 0.15 mA/µm. Hence, the buffer consumes about 8 mW from a 1 V supply voltage. The inductor $L_S = 183\,pH$

provides source degeneration (cf. section 3.6.3) to linearize the amplifier at the expense of power gain. The tail current filter consisting of $C_F = 180\,fF$ and $R_F = 10\,\Omega$ exhibits a cut-off frequency above 60 GHz, thus providing common mode rejection for the fundamental signal while passing its first harmonic. This improves amplitude and phase balance.
The output matching network consists of $L_1 = 174\,pH$, $L_2 = 75\,pH$ and $C_1 = 248\,fF$. The capacitance is added to decouple the buffer from the mixer core's LO input, allowing to impose a bias voltage different from V_{DD}.

In summary, rather than providing gain, the LO buffer improves phase and amplitude balance of the LO signal originating from the balun and compensates its loss. Furthermore, it is optimized for linearity to allow the use of single-ended input power levels up to 10 dBm.

4.5.2.5 *The RF output buffer*

A single-ended common-source RF output buffer is added between mixer core and 50 Ω load. Its schematic is given in figure 4.41. The employed 65 nm transistor is $26 \times 1\mu m$ wide and biased between peak f_{max} and maximum linearity current density. Thus, it consumes around 7 mW from the 1 V supply and achieves an output-referred 1 dB compression point of about -1 dBm. This ensures that the output buffer is not limiting the mixer's linearity.

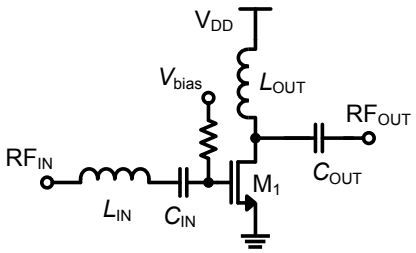


Figure 4.41: Common-source buffer amplifier added to the RF output port of the mixer

The output matching network of the RF buffer consists of $L_{OUT} = 110pH$ and $C_{OUT} = 67fF$. These values are calculated taking into account the pad capacitance of 25 fF that appears in parallel to the 50 Ω load. At the input, the inductor $L_{IN} = 143pH$ results from a connection of about 150 µm length between the RF buffer and the mixer core. The capacitor $C_{IN} = 67fF$ is added to achieve DC-decoupling and complete the input matching.
However, as during design phase the interconnect inductance L_{IN} was not extracted correctly, only imperfect matching is achieved, and the desired center frequency is shifted to higher frequencies. The output return loss obtained by the fabricated circuit is given in subsection 4.5.3.2.

4.5.3 *Measurement Results*

The mixer circuit described above was fabricated using the 65 nm CMOS technology of ST Microelectronics. Its die photo in figure 4.42 shows how the use of spiral inductors allows to achieve very small (actually

pad-limited) circuit size, even if a multitude of matching networks are necessary. Transmission lines are only used at the IF input due to the distance of 200 µm between the differential IF signal pads. At the LO input, the transformer balun, surrounded by dummy metal squares, is clearly visible. Apart from the RF output, which is asymmetric due to its single-ended nature, and the LO input of the transformer, the mixer circuit is laid out in perfect symmetry. Thus, if well balanced LO and IF signals are available, their rejection is expected to be very high at the RF output.
The mixer's large-signal behavior is measured on-wafer using Picoprobes, a Rohde & Schwarz FSU 67 GHz spectrum analyzer, an Agilent E8257D PSG 70 GHz synthesizer which delivers up to 14 dBm output power at 60 GHz and an Anritsu synthesizer to generate the baseband signal. The connections are made using V-type coaxial cables. The total loss in the RF path and the LO path is about the same, it amounts to about 8 dB. The IF loss is 0.5 dB at 1 GHz. The presented results are corrected by the measured loss values if not mentioned otherwise.
The single-ended return loss at the IF, RF and LO port is measured using an Anritsu 65 GHz VNA. In the case of the IF return loss measurements, one of the two inputs is matched by a 50 Ω precision load.

Biased at the current densities mentioned in the previous section, the complete circuit draws 23 mA from a 1 V supply, including IF, RF and LO buffers. The mixer's core power consumption is estimated to be only 1.5 mW.

4.5.3.1 *Conversion gain*

Figure 4.43 shows the power conversion gain G_c measured for different LO power levels at an LO frequency of 62 GHz. The IF frequencies

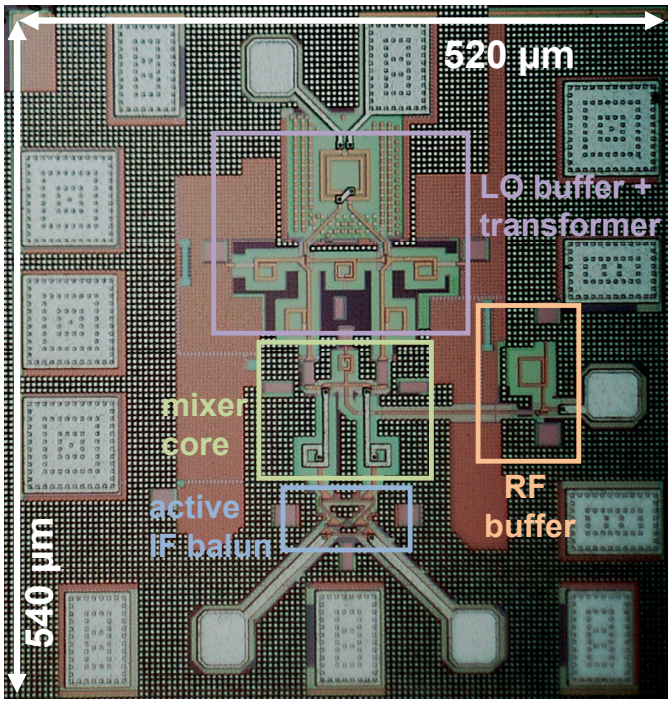


Figure 4.42: Die photograph of mixer circuit, size pad-limited

are 1 GHz and 2 GHz, respectively. Results for both the Lower Sideband (LSB) and the Upper Sideband (USB) are plotted. The maximum measured conversion gain for this LO frequency is G_c= -4.1 dB at f_{IF} = 1 GHz and G_c = -5.0 dB at $f_{IF} = 2$ GHz. It is achieved when the maximum possible LO power of 6 dBm is applied to the single-ended LO port of the mixer chip. Figure 4.43 allows the assumption that higher LO power levels allow a further increase of G_c, and that the mixer actually achieves is maximum G_c for LO power levels around 10 dBm. As this is the power level in front of the lossy transformer balun, lower LO powers should be sufficient if the mixer is directly driven by the output of an integrated differential VCO.
In figure 4.43, an asymmetry between the LSB and the USB can be observed, which is both due to the frequency response of the RF buffer stage and the phase imbalance of the differential inputs.

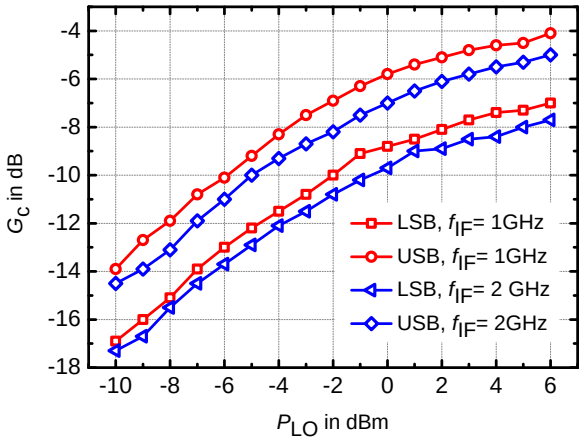


Figure 4.43: Conversion Gain versus LO power for two IF frequencies with $f_{LO} = 62$ GHz and $P_{IF} = -20$ dBm.

The results presented in the following are obtained using the maximum available LO power of 6 dBm. Figure 4.44 shows the conversion gain at different LO frequencies. It can be observed that G_c increases towards higher frequencies and is higher in the USB than in the LSB. This can be confirmed by figure 4.45, which plots G_c versus RF frequency at three different LO frequencies. It shows a rather flat response especially

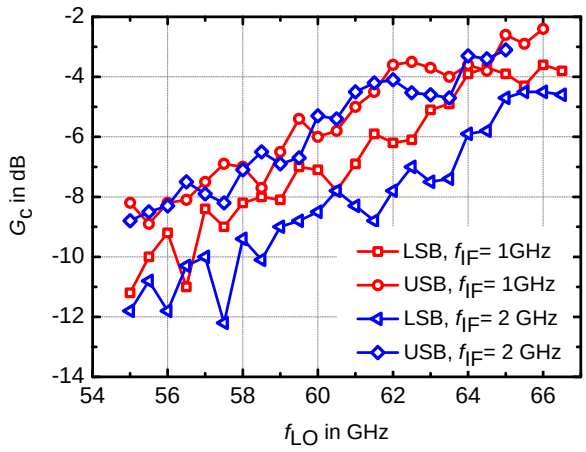


Figure 4.44: Conversion gain versus LO frequency for two different IFs

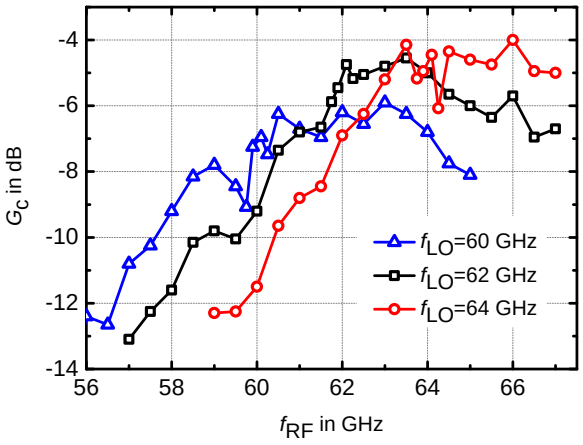


Figure 4.45: Conversion gain versus RF for three LO frequencies

in the USB, and conversion gain increasing towards higher frequencies. An explication for the difference between the sidebands can be given by the phase imbalance of the LO signal due to the balun: Similar to an image reject mixer, one sideband is amplified (here the USB) and the other weakened due to this effect. As the mixer will be driven by a differential on-chip VCO in the transmitter circuit, this effect is expected to disappear in the integrated version.
(Note that measurements above 67 GHz were not possible due to the limitations of the spectrum analyzer.)

4.5.3.2 *Return loss at the mixer ports*

The return loss at all three mixer ports was measured using a calibrated VNA whose reference plane was at the probe tips of the on-wafer probes. Figure 4.46 shows the single-ended IF input return loss with respect to 50 Ω. As expected, due to the use of a common-gate input stage, an extremely broadband input match is achieved. The measured return loss increases towards higher frequencies together with the parasitic's influence.

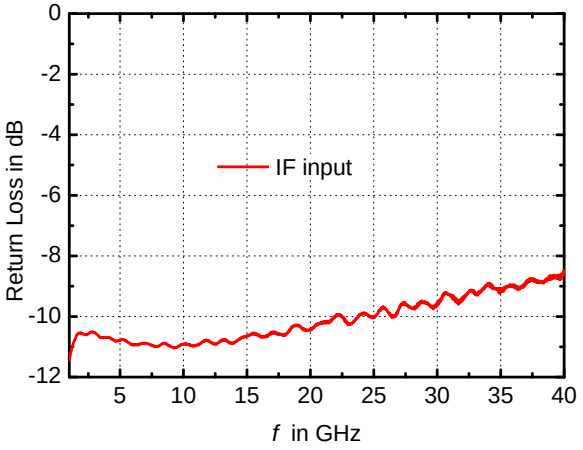


Figure 4.46: Measured input matching at the IF port

Figure 4.47 shows the return loss measured at the RF and LO port. The RF port's minimum return loss is shifted towards higher frequencies

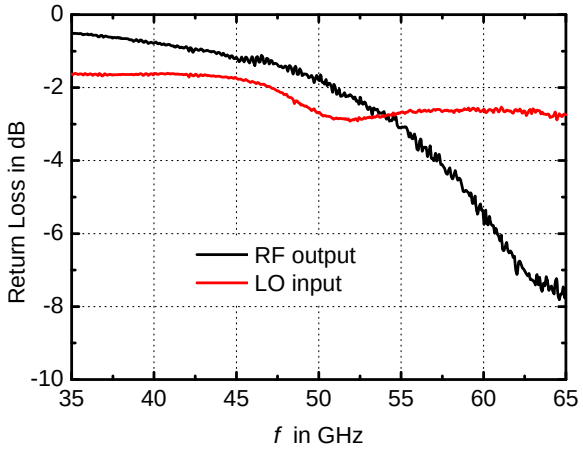


Figure 4.47: Measured LO input and RF output matching

and its value is quite high. As mentioned in subsection 4.5.2.5, the reason for this is that the inductance of the interconnect between mixer core and buffer was not extracted correctly.
The return loss at the LO input port is also quite poor: this is due to the fact that the transformer balun is directly connected to the LO pad without further matching circuitry.

4.5.3.3 *Isolation and linearity*

Figure 4.48 shows an example of the (uncorrected) output spectrum measured using the spectrum analyzer. The carrier and the sidebands are clearly visible. An LO-to-RF isolation of 15.4 dB is obtained is this case, which increases to 22.5 dB if P_{LO}= 6 dBm. This rather low isolation value originates from the amplitude and phase imbalance of the differential IF and LO signals. Especially the single-coil transformer balun at the LO port introduces this imbalance. As in the planned integrated transmitter the LO signal originates directly from the differential VCO presented in section 4.3, a much higher isolation is expected due to the

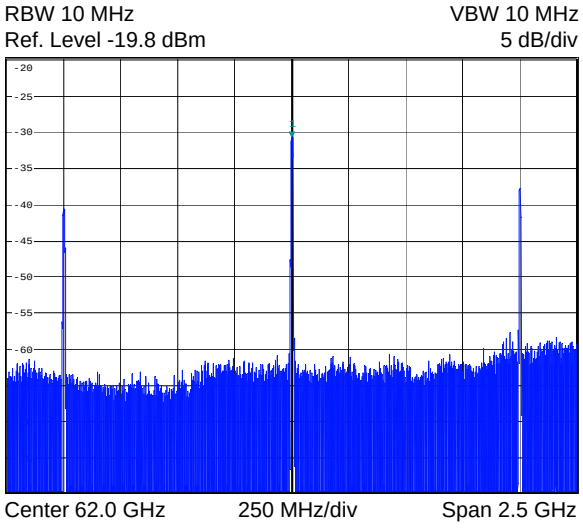


Figure 4.48: Uncorrected output spectrum using $P_{LO,corr}$ = -5 dBm, $P_{IF,corr}$=-20.5 dBm

balanced nature of the mixer.
To characterize the linearity of the mixer, input-referred 1 dB compression (IP_{-1dB}) and third order intermodulation (IIP3) points are measured. Figure 4.48 shows the plot used to find the former of them. It was created by sweeping the power of a 1 GHz signal applied to one of the IF input ports, while the other one was matched to 50 Ω. The LO power used is 6 dBm. For an input power of $IP_{-1dB} \approx -13$dBm the conversion gain and output power lie 1 dB below the linear extrapolation. This value decreases by around 2 dB if an LO power of -5 dBm is utilized.

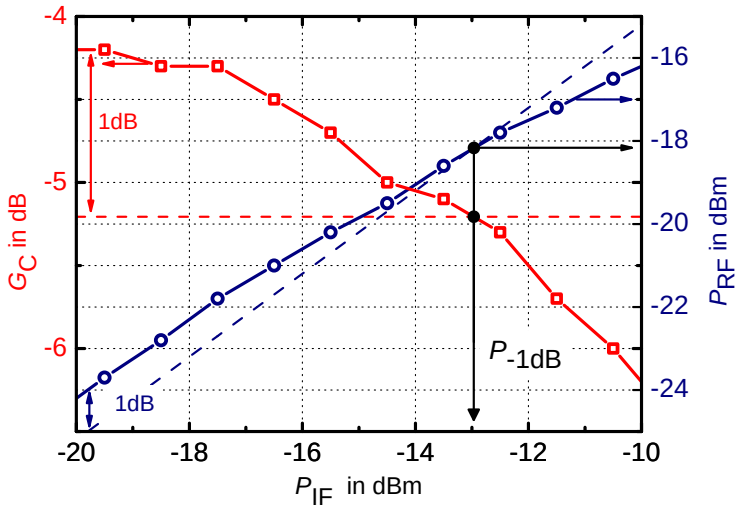


Figure 4.49: 1 dB Compression point measured at P_{LO}=6 dBm, f_{LO}= 62 GHz, f_{IF}=1 GHz

The IIP3 was measured by applying two signals of frequencies $f_{IF,1}$= 995 MHz and $f_{IF,1}$= 1005 MHz to the two IF inputs of the mixer, and sweeping their power from -26 to -22 dBm. The extrapolation of the fundamental and third-order intermodulation product in the upper sideband of the mixer's RF output yields an IIP3 of ≈ -4.2 dBm for P_{LO}= 6 dBm.

4.5.4 *Conclusion on the up-mixer*

This section presented the first double-balanced dual-gate up-conversion mixer for the 60 GHz band implemented in CMOS technology. It is published in [280]. The mixer's IF band ranges from DC to around 3 GHz, while the RF output lies inside the unlicensed 60 GHz band. The maximum power conversion gain measured on the fabricated test circuit for $P_{LO} = 6$ dBm, $f_{LO} = 65$ GHz and $f_{IF} = 1$ GHz is -2.4 dB. Its measured IP_{-1dB} and IIP3 are -13 dBm and -4.8 dBm, respectively. The total power consumption, including IF, RF and LO buffers is 23 mW, while the mixer core is consuming only 1.5 mW of DC power.
Furthermore, a novel IF buffer topology with integrated broadband active balun has been proposed and realized. It allows to test the mixer circuit using either a single-ended or differential IF signal and provides broadband input matching due to the use of a common-gate input stage.

If this mixer shall be used in a transmitter front-end, the redesign of the RF buffer's matching network, taking into account the corrected value of the interconnect inductance, is mandatory. Furthermore, a direct connection to an on-chip differential VCO is expected to improve conversion gain and LO-to-IF isolation and yield a better symmetry between upper and lower sidebands.

Table 4.4 compares the proposed balanced dual-gate mixer to other 60 GHz up-converters found in literature. The best performance in each column is highlighted. It shows that the proposed dual-gate architecture is a good alternative for applications where a Gilbert cell is too complex, and small chip area and low power consumption are desired.
If considering the achieved *output* power levels of the published mixers at the 1 dB compression point, one finds rather low values: in the case of resistive mixers that exhibit quite high IP_{-1dB} values, the high conversion loss limits the achievable output power. The proposed dual-gate mixer is no exception here.
However, for a low-power transmitter front-end, the output power of the mixer is a key parameter that has to be maximized. This is because it influences how much gain has to be added by subsequent power-hungry amplifier stages. Hence, further studies towards the use of a passive mixer with high output power, like the one published in [188] but as up-converter, are required.
The up-conversion mixer presented in this section is published in [280].

Table 4.4: Performance comparison to CMOS up-mixers found in literature

Reference	Techn. CMOS	Topol.	IF [GHz]	RF [GHz]	G_c [dB]	P_{LO} [dBm]	IP_{-1dB} [dBm]	P_{DC} [mW]	Die size [mm^2]
S. Voinigescu, 2007 [269]	90 nm	Gilbert	1 to 5	60	-4	N.A.	N.A.	70	0.6 × 0.6
M. Varonen, 2007 [273]	65 nm	resistive	1 to 5	53 to 62	-13.5	8.7	-5.5	0	0.7 × 0.67
I.C.H. Lai, 2007 [270]	90 nm	Gilbert	11	51	-11	0	1	13.2	0.6 × 1.05
J.-H. Tsai, 2007 [275]	130 nm	sub-harm.	0	35 to 65	-6	7	-13	75.9	0.98 × 0.8
F. Zhang, 2008 [271]	130 nm	Gilbert	1	59 to 65	4	0	-7.5	24	0.3 × 0.7
P.S. Wu, 2008 [276]	130 nm	sub-harm.	2.5 to 5.5	58 to 66	5	5	-10	92.2	0.366
Valdes-Garcia, 2008 [48]	65 nm	Gilbert	10	60	-6.5	5	-11.5	29	0.7 × 1.4
M.C. Chen, 2009 [272]	130 nm	Gilbert	0 to 3.5	58.3 to 62.5	-5.6	N.A.	-14	8.6	0.78 × 0.88
J.H. Chen, 2010 [274]	180 nm	resistive	0 to 5	15 to 50	-14.5	10	4 to 8	0	0.45 × 0.45
proposed mixer [280]	**65 nm**	**dual-gate**	**0 to 3**	**64**	**-2.4**	**6**	**-13.5**	**23**	**0.52 × 0.54**

4.6 CONCLUSION

This chapter presented the design of four key building blocks for the 60 GHz transceiver front-end which is in the focus of this thesis. All of these components have been realized paying special attention on power consumption and circuit size, which are the most important requirements of the targeted applications. At the same time, state-of-the-art performance with respect to the different features that are important for each of these building blocks was demanded. The design of these components is based on the technology and devices presented in the preceding chapter 3. This implies in particular the use of the 65 nm CMOS technology and full-custom spiral inductors, transformers and varactors.

The following components result from this part of the thesis:

- **A high-gain low-power Low Noise Amplifier (LNA), consisting of two cascode stages**. If a supply voltage of 1 V is applied, it dissipates only 8.5 mW, and occupies only 0.4×0.4 mm^2 of chip area, while providing 18.7 dB of gain at 56 GHz. This state-of-the-art performance has been published in [176]. A redesign with slightly higher center frequency is used for the receiver front-end in this thesis.

- **A Voltage Controlled Oscillator (VCO) achieving a record efficiency of 4.9 % while oscillating in a frequency range from 57.58 GHz to 60.80 GHz**. The VCO consumes 16.5 mW including buffers while occupying only 0.35×0.59 mm^2 of chip area. Its minimum phase noise is -90.3 dBc/Hz at 1MHz offset from a 60.77 GHz carrier. The high differential output power of up to -0.9 dBm is achieved by using a differential common-source Colpitts architecture which has not been employed in a 60 GHz CMOS oscillator before. The proposed VCO is published in [245] and serves as the local oscillator in the receiver front-end of this thesis.
  Further increase in tuning range and decrease in phase noise is feasible when optimizing the full-custom varactors employed and reducing the size of the tank inductor in favor of a larger capacitance.

- **A broadband high-gain single-balanced down-conversion mixer with the lowest required LO power (-5 dBm) and smallest die area (0.49×0.52 mm^2) found in literature for a 60 GHz down-converter**. The maximum achieved conversion gain is 9.1 dB, the output-referred 1 dB compression point is -5 dBm and the covered RF bandwidth reaches from 54 GHz to at least 65 GHz. The whole circuit draws 16.8 mA from a 1 V supply, while only 2.8 mW are associated to the mixer core. The achieved performance originates from the use of the current bleeding technique in combination with spiral inductors and the fact that the baseband signal is low-pass filtered in the mixer core. The down-mixer is published in [268] and used without major modifications in the receiver front-end presented in chapter 5.

- **A double balanced dual gate up-mixer with active IF balun**. The proposed mixer is the first CMOS implementation of a dual-

gate up-mixer for the 60 GHz band. At the differential IF input, it includes a novel differential buffer amplifier that can be used as single-ended-to-differential converter due to its high common-mode rejection.
With a maximum power conversion gain of -2.4 dB, an IP_{-1dB} and IIP3 of -13 dBm and -4.8 dBm, respectively, a total power consumption of 23 mW, and a very small die area of 0.52×0.54 mm^2 it exhibits state-of-the-art performance. It is published in [280].
However, its high required LO power and its low output linearity makes it unsuited for the low-power transceiver design targeted in this thesis. Thus, a passive mixer with low LO requirements, i.e. an up-converting version of the mixer presented in [188], has been developed by M. Ercoli for the transmitter front-end (not part of this thesis).

Based on the LNA, the VCO and the up-mixer presented in this chapter, a one branch receiver front-end has been developed. It is presented in the following chapter 5. Due to the fact that the individual building blocks are consequently designed for low power, small circuit size, high performance and integrability, a receiver front-end which is optimized in these regards becomes feasible.

5 INTEGRATION OF A ONE-BRANCH 60 GHZ RECEIVER FRONT-END

5.1 INTRODUCTION

The previous chapter presented the implementation of key building blocks necessary to build the 60 GHz transceiver front-end introduced in section 2.5 of chapter 2. The next important step towards the integration of these blocks to form the complete transceiver is to design a simplified receiver front-end. Most of the 60 GHz CMOS receiver circuits found in literature are of this type: either only a LNA and a down-mixer are integrated, driven by an external LO [62, 63, 67, 69, 71, 74, 89, 125, 126, 129, 281], or the demonstrated front-end also includes a VCO [75, 131, 132, 144]. In [73, 124] a more complete frequency synthesizer including a PLL is used.
This chapter presents such a simplified receiver, being composed of the in-phase branch of the direct conversion receiver front-end. It comprises the LNA, the down-mixer and the VCO presented in the previous chapter.

5.2 CIRCUIT OVERVIEW

The block diagram of the realized 60 GHz receiver front-end is given in figure 5.1. The signal interfaces to the outside consist of a single-ended 50 Ω 60 GHz Radio Frequency (RF) input and a differential $2 \times 50\,\Omega$ Baseband (BB) output. The DC off-chip interfaces are also annotated in figure 5.1: they comprise the supply voltage $V_{DD} = 1\,V$, the control

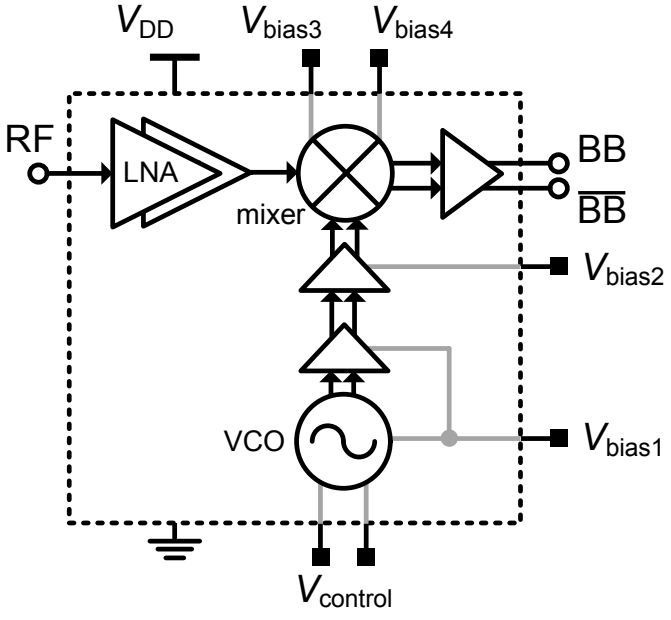


Figure 5.1: Block diagram of the realized receiver front-end with off-chip interfaces

voltage to tune the LO frequency and four bias voltages to adjust the bias currents to the optimum values. The remaining bias currents are derived from the supply voltage by on-chip current mirrors (cf. section 3.6.1.2). The distribution of these supply and bias voltages, and the isolation of adjacent circuit blocks, is done according to the method described in section 3.7.2.
The building blocks that constitute the receiver front-end can be found the different sections of chapter 4:

- The LNA is presented in section 4.2 (the redesigned version is used).
- The VCO with attached source-follower buffers is discussed in section 4.3.
- The down conversion mixer and its differential BB buffer amplifier is illustrated in section 4.4.
- The second differential LO buffer amplifier, whose gain is controlled by the bias voltage, is described in section 4.5 since it also served as part of the standalone up-conversion mixer.

The only difference between these blocks and the ones detailed in chapter 4 is the adaption of the in and output matching networks to preceding or subsequent building blocks, if these interfaces change from external ones to internal ones due to the receiver integration. Namely, this is the case between LNA output and mixer RF input and at the interfaces between the LO buffers and the mixer LO input. Here, the matching networks at the in- and outputs of the standalone circuit blocks are replaced by interstage matching networks. They realize the same impedances as the ones present at these points in the original circuits.

5.3 FABRICATED CIRCUIT

Figure 5.2 shows the die photograph of the fabricated receiver front-end. Its very small size of 0.550 mm^2 is essentially pad-limited: the aligned circuit blocks without pads are only about 200 µm wide. This is the result of using a total of 17 compact spiral inductors for matching. The number of pads can further be reduced because multiple V_{DD} and ground connections are provided (see the respective symbols in figure 5.2). These redundant connections are not essential for the operation of the receiver due to its low supply current (about 43 mA). Furthermore, the bias voltages could be derived from V_{DD} in a redesigned version, allowing to remove four more pads.
The lower part of the circuit, which consists of the differentially implemented parts, is very symmetric to reduce mismatch and improve LO-to-BB isolation.

5.4 MEASUREMENT RESULTS

The receiver front-end was characterized on-wafer using a 67 GHz single-ended 100 µm G-S-G Picoprobe to provide the RF signal and a differential G-S-G-S-G probe of the same type to measure the BB output. The DC voltages were connected using two eyepass six-finger probes.
The measurements were done using either an Anritsu MS4647A 70 GHz

VNA to obtain the return loss. In this case, one of the differential BB outputs was matched to 50 Ω by a precision load. For conversion measurements, an Agilent E8257D 67 GHz synthesizer served as signal source and a LeCroy SDA813Zi 13 GHz real time oscilloscope with spectrum analyzer functionality was connected to the circuit's differential BB output. The loss due to cable and probes is de-embedded and 3 dB is added to the output power in case of single ended measurements.

5.4.1 *Power Consumption*

The receiver front-end is biased at the optimum current densities of the circuit components by applying bias voltages of $V_{bias1} = 460\,mV$,

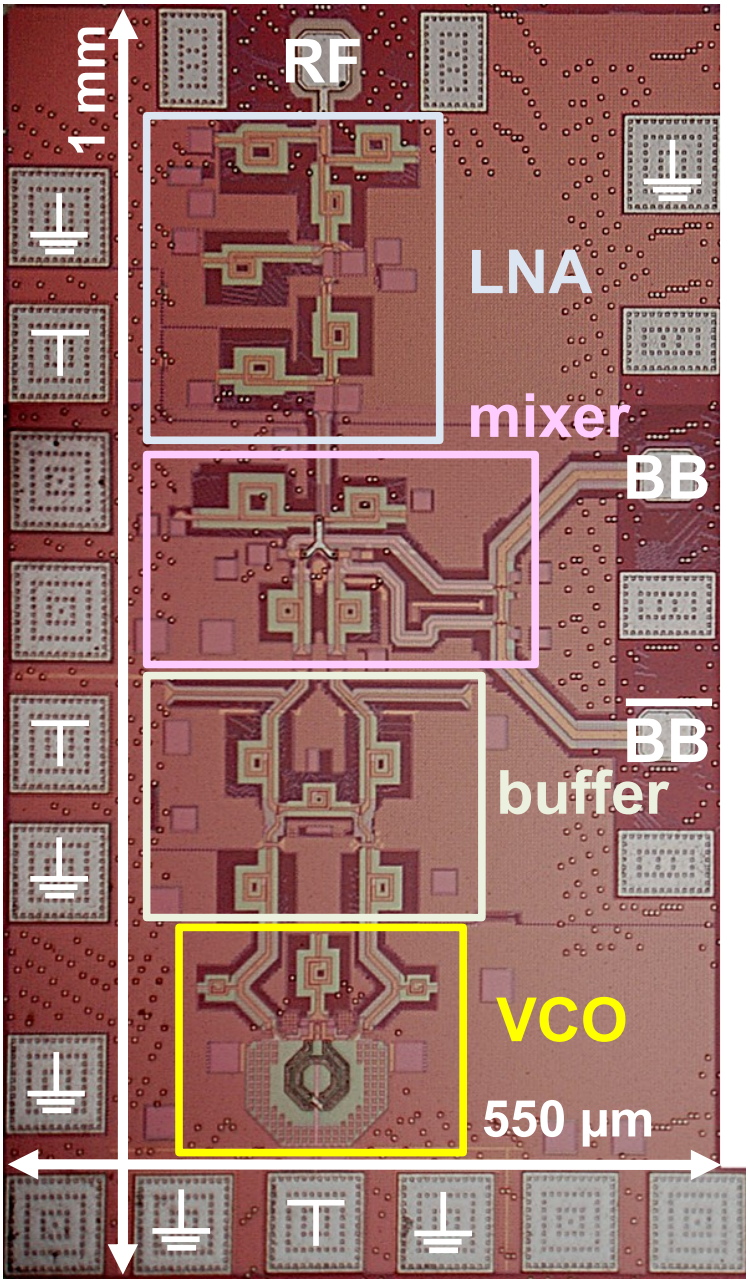


Figure 5.2: Microphotograph of the fabricated CMOS receiver front-end

$V_{bias2} = 390\,mV$, $V_{bias3} = 510\,mV$ and $V_{bias4} = 540\,mV$. It draws about 43 mA from a 1 V supply, thus consuming $P_{DC} = 43\,mW$. This power consumption can be reduced by the amount contributed by the BB buffers (i.e. $\approx 14\,mA$, cf. section 4.4) in an integrated version, because the BB output usually does not have to drive two $50\,\Omega$ loads but a variable gain amplifier with high impedance inputs. Thus, VCO, LO buffers, downmixer and LNA together consume only 29 mW.

5.4.2 *In- and Output Return Loss*

The return loss at the RF input and the baseband output of the receiver front-end were measured at the above mentioned bias point with a control voltage of $V_{control} = 0\,V$, corresponding to a LO frequency of about $f_0 = 57.5\,GHz$. However, the oscillation frequency does not have any influence on the return loss, as both input and output of the receiver are very well isolated from the LO.

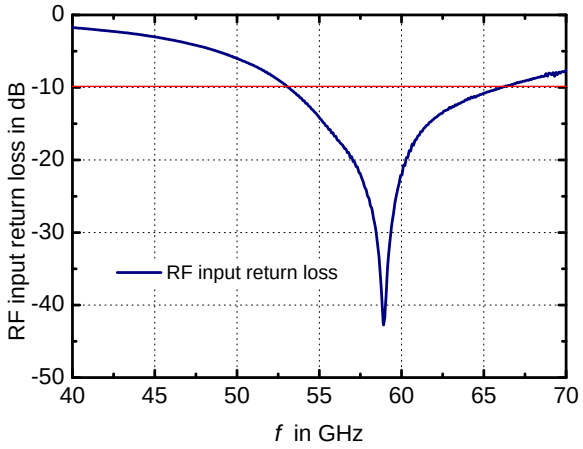


Figure 5.3: Return loss measured at the RF input of the receiver front-end

Figure 5.3 shows the measured excellent, broadband input match which lies below -10 dB from 53.1 GHz up to 66.0 GHz. The minimum return loss of -42.7 dB is achieved at 58.9 GHz.

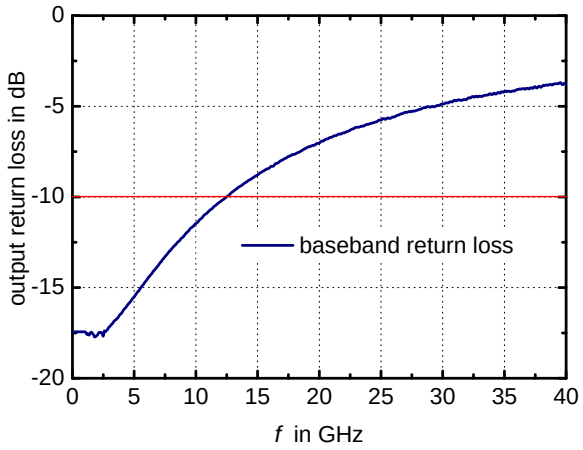


Figure 5.4: Return loss measured at the baseband outputs of the receiver front-end

Figure 5.4 shows the return loss of the baseband output of the receiver front-end. The measured value is about -17.4 dB within the entire required baseband bandwidth of about 1 GHz, and stays below -10 dB up to 12.5 GHz.

5.4.3 *Frequency Tuning Range*

As for the VCO presented in section 4.3, the frequency tuning range of the receiver is about 3 GHz. However, the absolute oscillation frequencies have slightly shifted in the receiver. They lie between 57.0 GHz and 60.0 GHz for a control voltage between 0.15 V and -3 V. This can be explained by the different loads connected to the VCO and the fact that automatic dummy insertion (cf. section 3.7.1) was done differently between the fabrication runs of the standalone VCO and the receiver front-end.

5.4.4 *Conversion Gain*

To measure the receiver's conversion gain, a low-power sinusoidal signal is injected at the RF port of the receiver front-end. In the Lower Sideband (LSB), this signal lies f_{IF} below the carrier frequency, in the Upper Sideband (USB) this signal is f_{IF} above f_{LO}. The ratio between the received power at the differential baseband output and the injected signal power is denoted as power conversion gain G_C in the following. (Note that due to the use of very high impedances at the BB output, receivers in literature often report the voltage conversion gain, which in these cases is considerably higher than the power conversion gain).

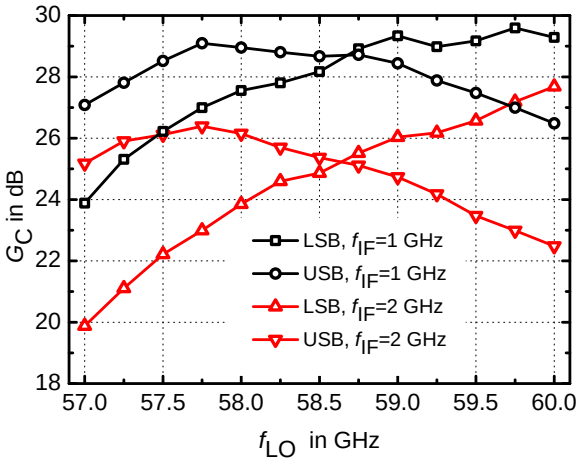


Figure 5.5: Measured power conversion gain versus LO frequency

Figure 5.5 plots the conversion gain in the LSB and USB for baseband frequencies of 1 GHz and 2 GHz. A maximum power conversion gain of 29.5 dB is achieved for a baseband frequency of f_{IF}=1 GHz. In agreement with the input return loss and the characteristic of the redesigned LNA (cf. section 4.2), the LO frequency for which both sidebands have the same conversion gain is about 58.75 GHz. The 3 dB RF bandwidth of the receiver, which is limited by the response of the LNA, reaches from about 56.5 GHz to about 61.5 GHz, thus spanning 5 GHz in the

lower part of the unlicensed 60 GHz band. The LO frequency range considered in figure 5.5 is limited by the oscillator's tuning range.

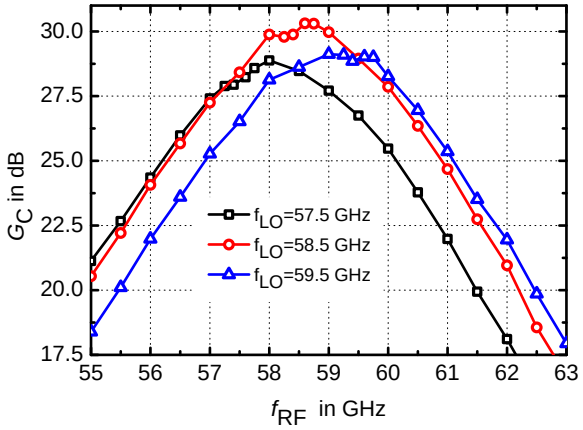


Figure 5.6: Measured power conversion gain versus RF frequency at different LO frequencies

Figure 5.6 plots the conversion gain versus RF input frequency for different LO frequencies. It illustrates that within the bandwidth of 1.88 GHz around the carrier, which is required by the different standards, quite high values between 26 dB and 30 dB are achieved at all possible LO frequencies. For the central LO frequency of f_{LO}=58.5 GHz, the one-sided 3 dB baseband bandwidth is measured to be about 1.5 GHz, corresponding to a channel bandwidth of 3 GHz around the carrier. The receiver's bandwidth is not limited by the baseband circuitry or the mixer, but rather by the characteristics of the LNA, which results in the fact that input signals above and below the center frequency of 58.5 GHz experience less gain.

5.4.5 *Output Waveforms*

To analyze the balance of the differential signal at the baseband output of the receiver, the voltage waveforms were measured for different frequencies and input powers. Figure 5.7 shows this signal at both baseband outputs when the frequency difference is 1 GHz. Even at this high frequency, the phase shift of 180° is well maintained, while variation occur due to the phase variations of the unlocked VCO. For lower baseband frequencies, the voltage waveforms are even better aligned.
To illustrate the impact of the receiver's nonlinearity on the output signal, figure 5.8 shows the spectrum observed at the BB output if the input signal is 11 dB above the 1 dB compression point. While the uncorrected, single-ended BB output signal level is at -6 dBm, the first harmonic (which disappears in the differential case) at 2 GHz is as low as -31.3 dBm and the third harmonic at 3 GHz exhibits a power level of -39.1 dBm. These harmonics lie below the the noise floor if the input power falls below the compression point, yielding a very clean receiver output spectrum.
(The output spectrum in the frequency band around 60 GHz could not be measured due to the unavailability of the appropriate equipment, but from the fact that return loss at this port in this frequency range was

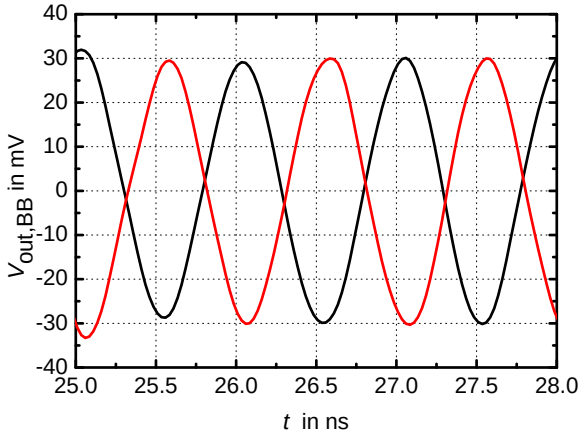


Figure 5.7: (Uncorrected) output voltages at both baseband outputs for f_{LO}=58 GHz, f_{RF}=59 GHz and P_{RF}=-45 dBm

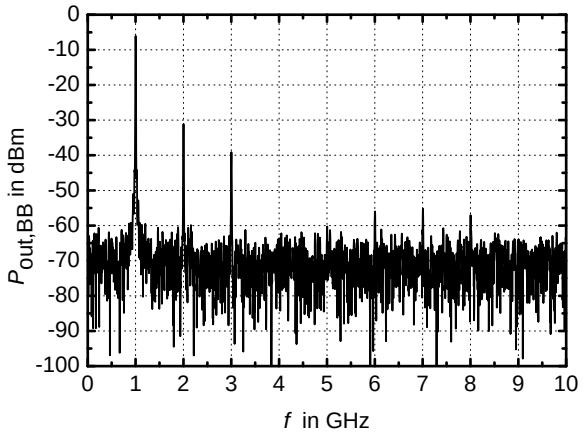


Figure 5.8: (Uncorrected) single-ended output spectrum for f_{LO}=58 GHz, f_{RF}=59 GHz and P_{RF}=-25 dBm

not affected at all by LO frequency and power, a very good LO-to-BB isolation can be surmised).

5.4.6 *Linearity*

The linearity of the receiver front-end is characterized by its 1 dB compression point P_{-1dB}. Figure 5.9 plots power conversion gain and output power versus input power to obtain its value: it shows that the receiver achieves an output-referred compression point OP_{-1dB}=-11 dBm, which corresponds to an input-referred compression point of IP_{-1dB}=-36 dBm. This quite low value at the input of the receiver results from the high conversion gain and the non-linearity of the output stage as discussed in section 2.5. However, as both the received in-band power and the interference power level at the receiver input are expected to be well below this value, this compression point is sufficient for a 60 GHz receiver.

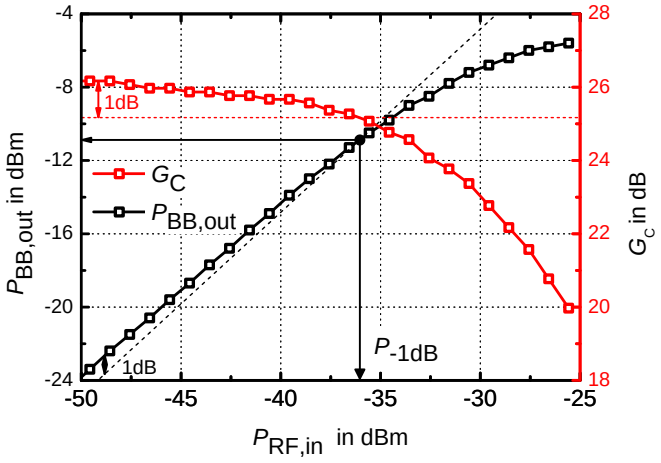


Figure 5.9: Linearity measurement for f_{LO} = 59 GHz and f_{RF} = 60 GHz

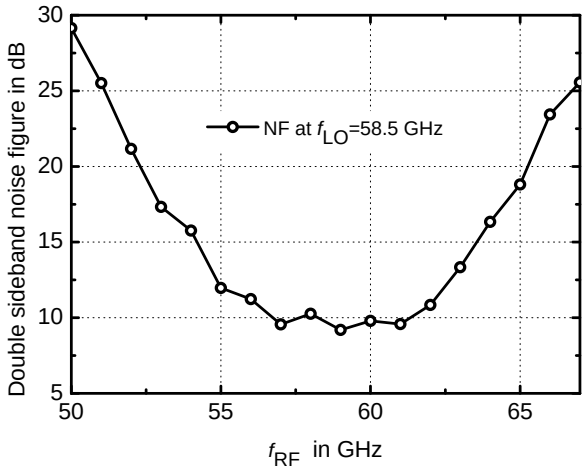


Figure 5.10: Measured double sideband noise figure at f_{LO}=58.5 GHz (influence of spectrum analyzer not removed)

5.4.7 *Noise Figure*

The NF of the receiver has been measured using a 60 GHz noise figure measurement system employing the Rohde & Schwarz FSU 67 GHz spectrum analyzer and the associated FS-K30 noise figure measurement software. A Noisewave NW50G75-W noise source, with an ENR above 15.5 dB, calibrated from 50 to 75 GHz in 1 GHz steps is employed to generate the noise in the RF frequency band of the receiver front-end. The measurement is based on the Y-factor method.
While the influence of the access cables between the noise source and the receiver front-end is de-embedded after measurement, a calibration to remove the noise contribution of the spectrum analyzer has not been done. The reason for this is that to characterize the baseband noise of the analyzer, a direct connection to the noise source output is not sufficient: a frequency conversion from the output of the noise source (in the 60 GHz band) to the input of the spectrum analyzer (baseband) is necessary, as a down-mixer doing this transposition during DUT characterization is part of the receiver. Thus, the measurements include a systematic error due to the noise of the spectrum analyzer, making

the obtained noise figure higher than the actual one of the front-end. Figure 5.10 shows the obtained results from these measurements for an LO frequency of 58.5 GHz. The double-sideband noise figure stays close to 10 dB within the entire communication band, with a minimum value of 9.2 dB. This leads to an estimation of the actual receiver noise figure of below 9 dB, when the noise contribution of the spectrum analyzer is not taken into account.

5.5 CONCLUSION ON THE RECEIVER FRONT-END

This section presented one branch of a 60 GHz direct conversion receiver front-end, implemented in 65 nm CMOS technology, as a first step towards the integration of a complete 60 GHz transceiver. Table 5.1 compares the receiver front-end realized in the framework of this thesis to the state of the art. It contains published front-ends of different levels of complexity. The third column shows which components, besides LNA and mixer(s), are included in each circuit. This is necessary to allow a fair comparison, as the circuit presented in this thesis includes a VCO to internally generate the LO signal. Among the implementations given in table 5.1, only the ones highlighted in gray exhibit a complexity comparable (or superior) to the proposed receiver front-end. Thus, when quantitatively comparing the characteristics for whom this complexity is decisive (i.e. power consumption and circuit size), only these references are taken into account. The front-ends achieving the best performance for each category are highlighted in blue.
The comparison shows that the first strength of the proposed implementation is its very low power consumption of only 43 mW. This value is lower than that of other receiver front-ends of comparable complexity. The second strength is the very small size of the presented implementation, which originates from the use of spiral inductors and the realization in 65 nm technology. Furthermore, the achieved conversion gain of 30 dB compares very favorable to the state of the art.
The measured receiver noise figure is comparable to the values found in literature. Furthermore, as these measurements still include some noise from the spectrum analyzer used for the measurements (cf. section 5.4.7), the actual value is potentially better than the one given in table 5.1.
Regarding the realized bandwidth, the table shows that most of the receiver front-ends only cover parts of the unlicensed 60 GHz band. The proposed realization is no exception. With 5 GHz it exhibits a typical performance in this regard.
The weak point with respect to the state of the art of the presented front-end is its linearity, quantified by an input-referred compression point of only -36 dBm. This low value can be explained by the front-end's low supply voltage of 1.0 V and its high conversion gain, which results in a saturation of the output stages. However, for the application of the front-end this is not critical, as the input power received by the antenna is not expected to ever attain this compression point. Direct coupling from the transmitter output to the receiver input is also not expected to be a problem here, as transmit power remains below a value that would damage the receiver front-end, and receive and transmit paths are not employed simultaneously and separated by a switch with high isolation.

Due to the demonstrated performance, the receiver front-end proposed in this thesis is perfectly suited for communication using the lowest channel of the unlicensed 60 GHz band, whose center frequency is 58.32 GHz (cf. section 1.2.2). The presented work constitutes a low-power, small-size (and thus low cost) implementation as required by the applications described in section 1.1.

Table 5.1: CMOS receiver front-ends found in literature, highlighted rows include LO

Reference	Tech. [nm]	Consists of LNA, mixer(s) &	RF [GHz]	IF [GHz]	NF (DSB) [dB]	G_C [dB]	IP_{-1dB} [dBm]	P_{DC} [mW]	Area [mm^2]
B. Razavi, 2006 [67]	130	-	57.5-64.5	0	12.5	28[1]	-22.5	9	0.12[2]
D. Alldred, 2006 [69]	90	IF & LO buffer	51.5-56.5	3.8-5.5	6	21.5	-21.0	60	0.29
S. Emami, 2007 [62]	130	IF amp., VCO, doubler	57-63	2.0	10.4	11.8	-15.8	76.8	3.8
Sanduleanu, 2007 [144]	90	VCO	59-61	0	9.5	23	N.A.	54	0.86
A. Tomkins, 2008 [70]	65	LO buffer	58-63	0	5.6	14.7	-22.0	151	0.5
B. Afshar, 2008 [63]	90	VGA	58.5-62.5	0-2.2	6.1	18[3]	-26.0	24	1.55
C.S. Wang, 2008 [74]	130	BB & LO buff.	60-65	20	10	30	-27	44	0.77
Tanomura, 2008 [89]	90	BB buff.	60-64	0	8.3	N.A.	N.A.	206	1.9
T. Mitomo, 2008 [124]	90	BB buff.,PLL, antenna	61.3-63.4	0.1	8.4	22.5	N.A.	144	2.64
K.H. Chen, 2008 [73]	90	PLL	61.4-63	1	5.6[4]	25.2	-16	132	1.0
J. Borremans, 2009 [126]	45	digital control	56-67	0-1	6	26	-21.5	21	0.02[2]
Kärkkäinen, 2009 [129]	65	IF buff.	51.5	0.5-2.0	9.2	14.5	-24.4	174	0.9
J. Lee, 2009 [75]	90	IF buff., VCO, OOK demod.	60	10	7.0	25	-26	103	0.68
S. Bozzola, 2009 [131]	65	BB & LO buff., VCO	62-67	20	9	28[1]	-26	80	0.5[2]
C.C. Chen, 2010 [125]	130	BB buff.	50.8-60.6	0.1	9	18	-20.8	50.2	1.2[2]
F. Vecchi, 2010 [132]	65	BB & LO buff., VCO	55-68	20	5.6	35.5	-39	75	2.5
proposed front-end	**65**	**BB & LO buff., VCO**	**56.5-61.5**	**0-1.5**	**9.2[5]**	**30**	**-36**	**43**	**0.55**

[1] voltage gain, [2] only active part, [3] without VGA, [4] NF of LNA, [5] including noise of analyzer

6 CONCLUSION ON TRANSCEIVER FRONT-END DESIGN

The previous five chapters presented the design of a 60 GHz transceiver in a 65 nm CMOS technology. After an introduction to the different aspects of communication in the 60 GHz band and a system overview in chapter 1, chapter 2 discussed the state-of-the-art of 60 GHz radio front-ends in CMOS technology and reviewed suitable front-end architectures. Based on these considerations, a direct conversion architecture with single ended RF path and differential LO and baseband paths is adopted both for the receiver and the transmitter.
Chapters 3, 4 and 5 deal with the RFIC implementation of parts of this front-end. Based on the description of the 65 nm CMOS technology and the discussion of available and full-custom devices in chapter 3, chapter 4 presents the implementation of the front-end building blocks. Chapter 5 shows the first step towards the on-chip integration of the transceiver front-end, which is the realization of one branch of the I/Q receiver.

Several parts of this work gave rise to the publication of novel techniques and circuits:

- The guidelines to very accurately simulate mm-wave inductors, described in section 3.4.3, are published in [200].
- The improved de-embedding technique for the measurement of mm-wave passive devices, discussed in section 3.5, is published in [195].
- The components described in chapter 4, i.e. the LNA, the VCO and the mixers, are realized by circuits that advance the state-of-the-art of 60 GHz RFICs. The demonstrated improvement can be attributed both to the use of lumped element matching in combination with the 65 nm CMOS technology, and the employed circuit design techniques. The associated publications can be found in [176, 245, 268, 280]. The distinguishing features of these building blocks are summarized in detail at the end of chapter 4.
- The receiver front-end presented in chapter 5 exhibits a circuit size and power consumption below the one found in literature for comparable radio front-ends. The publication of this circuit is in progress.

Future work includes the integration of the complete transmitter and receiver front-end, featuring an in-phase and a quadrature path, as described in chapter 2. To this end, two essential building blocks not described in this thesis, i.e. the PLL and the power amplifier, have been realized by project partners. Furthermore, as mentioned in chapter 4, the up-conversion mixer realized as part of this thesis shall be replaced by a passive mixer with improved output linearity and relaxed LO power requirements in the final transceiver. A first (down-converting) version of this mixer is published in [188].

The assembly of all components to form the complete transceiver front-end is intended to be done by adjusting the matching networks to achieve inter-stage matching, as in the case of the receiver front-end presented in chapter 5. Wilkinson power combiners and dividers shall be used to implement the branching points at the LNA output and the PA input. The generation of a quadrature LO signal from the VCO output is going to be done using a quadrature hybrid.

Part II

BEHAVIORAL MODELING OF MILLIMETER-WAVE CIRCUITS

7 INTRODUCTION TO BEHAVIORAL MODELING

7.1 SYSTEMS ON CHIP AND SYSTEMS IN PACKAGE

In order to simplify the assembly and reduce the cost when realizing a radio interface, the concepts of System on Chip (SoC) and System in Package (SiP) have been introduced [41]. They replace a classical assembly that consists either in mounting the individual circuit blocks on a Printed Circuit Board (PCB) as in the case of most modern consumer electronic devices or in putting together connectorized components as in the case of many commercial communication systems.
In a SoC, all circuits of the radio interface are integrated on a single chip. This requires a technology suitable for the implementation of all functionalities, ranging from Medium Access Control (MAC) to the antenna.
In the case of a SiP, this requirement is relaxed: the building blocks are implemented in different technologies, chosen according to the individual circuit's needs. These blocks are then combined to form a heterogeneous system which can be housed in a common package. An appropriate packaging technology needs to be employed to provide the interconnects between individual components and place them inside the package.

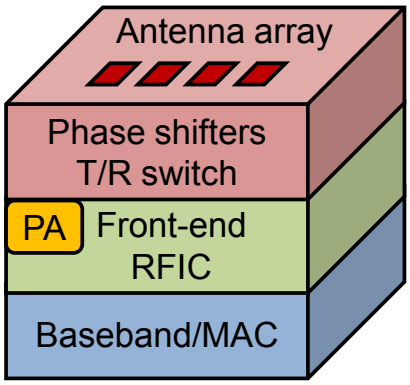


Figure 7.1: Example of a mm-wave radio interface integrated as System in Package (SiP)

Figure 7.1 illustrates the in-package integration of a mm-wave radio interface. The heterogeneous nature is underlined by the different colors and levels: while the mm-wave front-end can for instance be integrated in 65 nm CMOS as shown in part I of this thesis, the phase shifters and the Transmit/Receive (T/R) switch may use Radio Frequency (RF) Micro Electro Mechanical System (MEMS) technology. The Power Amplifier (PA) can be realized in Silicon Germanium (SiGe) or Gallium Arsenide (GaAs) technologies to provide higher output power.
A special feature of SiPs for communication at short wavelengths is the possibility of also integrating the antenna into the package. In addition to lower cost, simplified assembly and size, the advantage is the avoid-

ance of long, lossy and sensitive mm-wave external interconnects in favor of short in-package vias.

7.2 MODELING OF SOC/SIP BEHAVIOR

To successfully assemble a complex SoC or SiP, the behavior of the combined building blocks has to be simulated, and their interaction has to be taken into account. This presents several challenges. To illustrate the arising issues, figure 7.2 shows how a typical mm-wave SiP is subdivided into a digital, a mixed-signal, an analog and a mm-wave domain. Typical blocks present in the different parts of the circuit are noted together with their desired and undesired interaction. (More details on the exact architecture of the mm-wave front-end developed as part of this thesis are given in part I).
To design the individual circuits of the SiP, simulators that work on different abstraction levels are employed: in the digital domain, high-level behavioral VHDL models are used, because they can be directly used to synthesize the circuit.
In the analog and mixed-signal domains, circuit designers use device level models that are much more complex: the circuit simulators PSPICE or SPECTRE use netlists that include thousands of extracted parasitics and sophisticated models of sub-micron transistors that take hundreds of parameters. For the RF front-end and the antenna, in addition to that, electromagnetic simulations become necessary.

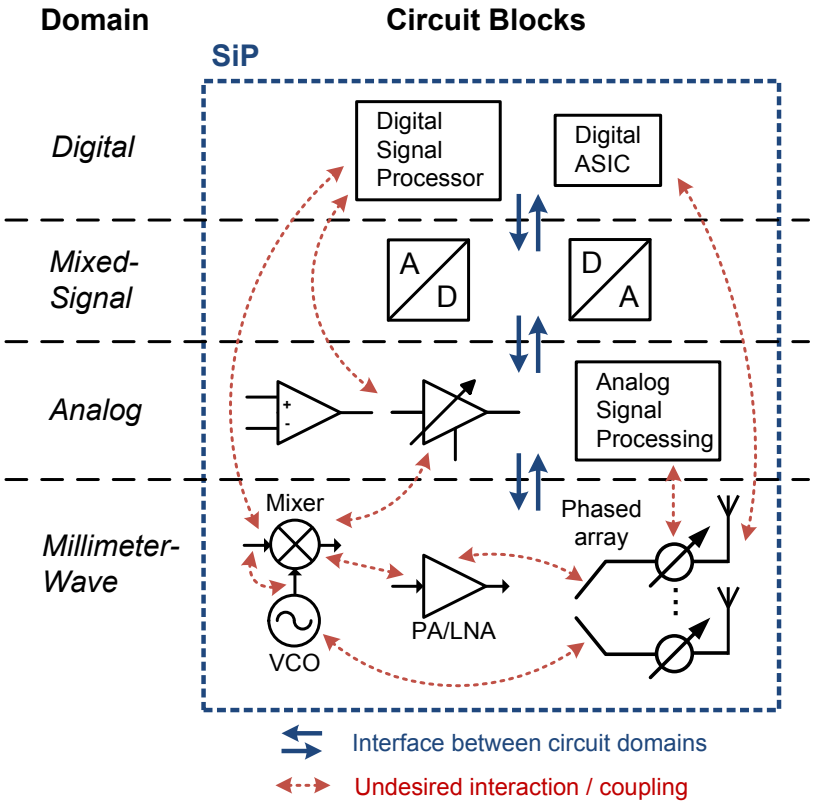


Figure 7.2: Illustration of the different domains of a mm-wave System in Package (SiP) showing typical building blocks and highlighting the issue of parasitic coupling.

These very sophisticated models, which usually are used for the design of all but the digital circuit blocks, cannot be employed when it comes to simulating the whole SoC or SiP due to two major issues:

1. Because of the high complexity of these models, the computation time and resource requirements become prohibitively high.

2. Due to the heterogeneous nature of the different blocks, a variety of different, often proprietary software tools (like ADS, SPECTRE, etc.) are used for device level simulation. Hence, they cannot be simply put together to form one single model for system simulation.

A solution that solves both problems simultaneously is the creation of behavioral black-box models of all SiP components using a unified modeling language. These models do not need to reproduce the internal details of the components (which nevertheless are essential during circuit design), so that a large reduction in complexity and thus computation time is possible. In addition to that, the resulting models can be passed to customers together with Intellectual Property (IP) components without compromising any circuit details.
While the methodology to create the behavioral models depends on the respective building block, and thus will not be identical for all of them, a common modeling language has to be chosen. This choice is influenced by the fact that for the digital circuits, which are automatically synthesized on the basis of VHDL code, behavioral VHDL models are already available. Their re-use is desirable. Thus, the analog and mixed-signal extension to VHDL, named VHDL-AMS and introduced in section 7.3, is the ideal candidate for the implementation of the black box models. Hence, this language is used for the implementation of the models developed in the framework of this thesis. Note that this decision in favor of VHDL-AMS does not constrain the application of the behavioral models presented in the following: if desired, they can by implemented in other modeling languages as well.

7.3 VHDL-AMS

VHDL-AMS, which is the acronym for VHSIC Hardware Description Language - Analog and Mixed-Signal, is an extension to VHDL, introduced in 1999 by the IEEE Standard 1076.1-1999 [282] in order to add analog and mixed-signal capabilities to a language that was up to then limited to the description of digital circuits. A brief overview of the these extensions is given in appendix A. A more detailed introduction to VHSIC Hardware Description Language - Analog and Mixed-Signal (VHDL-AMS) is published in [283] by E. Christen and K. Bakalar, two major contributors to the IEEE standard. An exhaustive designer's guide can be found in [284].
Note that in contrast to VHDL, which is widely employed as a basis for digital circuit synthesis, VHDL-AMS is today only used for circuit modeling. Analog and mixed-signal synthesis based on this language is still in its infancy [285]. The models presented in the following are in no way suitable for automatic circuit generation.

7.4 THE DEVELOPED BEHAVIORAL MODELS

In the context of this thesis, considerable research work has been done concerning the behavioral modeling of mm-wave oscillators. All results of this work are published in [286–290] and the novel modeling approach developed is presented in chapter 8. It is directly applicable to the creation of a behavioral model for the Voltage Controlled Oscillator (VCO) designed in part I of this thesis.
Additional work on the modeling of capacitive RF MEMS shunt switches and phase shifters in VHDL-AMS by the author of this thesis can be found in [291, 292] and in appendix C.

8

A NOVEL TECHNIQUE TO CREATE BEHAVIORAL MODELS OF MILLIMETER-WAVE OSCILLATORS

This chapter describes a novel technique to model the transient, steady state and phase noise behavior of mm-wave oscillators developed in the framework of this thesis. The model is implemented using the hardware description language VHDL-AMS, however, other implementations are feasible. It can be applied to a large variety of both single-ended and differential voltage-controlled oscillators independently of their architecture. The model is derived from output data obtained by a more complex circuit-level model, as for example the one used for the design of the VCO in part I of this thesis.

8.1 INTRODUCTION

There exist a multitude of different approaches to model nonlinear microwave circuits at system level, introduced e.g. in [293], [294] or [295]. Depending on the approach, either time or frequency domain descriptions are possible. However, the input and output data streams of a communication system are not periodic, and thus usually described in the time domain. Furthermore, the VHDL model of the digital part is a time domain model. To allow a convenient interface between the digital circuits and the remainder of the system, a time domain model is thus required also for the front-end blocks, including the oscillator. For this reason frequency domain models are not further taken into consideration here.

The behavioral time-domain models of oscillators can be divided into two principal categories: Either, the output voltage is expressed by a known, usually sinusoidal function that is evaluated at each time step (e.g. [296], [297]). However, in this case neither the transients and dynamics of the oscillator nor its nonlinear characteristic are correctly reproduced. Thus, the use of such models is limited to very simplified considerations.

Or, secondly, the oscillator is described by an equation solved during simulation. The prototype for a model of this category is the Van der Pol-equation: Here, a second order nonlinear Ordinary Differential Equation (ODE) describes the output voltage of a triode oscillator, using a polynomial to approximate its nonlinear characteristic [298]. An extension of this polynomial in order to model solid state oscillators is not trivial, because in addition to the function describing the device current, nonlinear capacitances need to be taken into account. Furthermore, neither the operating point and common mode behavior of differential oscillators nor its phase noise characteristics are incorporated in a model based on the Van der Pol-equation.

In the context of large signal network analysis, different nonlinear modeling techniques of the second type are investigated in literature. They approximate the nonlinearity of the circuit by radial basis functions, multivariate polynomials, or artificial neural networks, the latter showing the most accurate results [299]. The dynamics are either contained by using delays to maintain the notion of time [300], or in form of an

ODE that is solved by the simulator [301].
However, all these methodologies yield *input-output* models of microwave multiports and thus cannot be directly applied to oscillators, which only exhibit *one* microwave output. Nevertheless, some of the basic concepts used to develop these methodologies are adopted in the presented oscillator model.
The approach proposed in the following describes the oscillator's behavior in state space, i.e. by a system of first-order ODEs. The nonlinear relationship that is contained in these equations is represented by an Artificial Neural Network (ANN), similar to [299]. It is thus a non-physical black box model that is capable of incorporating the strong nonlinearities occurring in integrated microwave oscillators as well as its dynamics.
The novel modeling technique is very general: By reducing the order of the system to the minimum of two that is necessary to describe an oscillation, the evolution of the system state can be described in a two-dimensional state space. Depending on the architecture of the oscillator, the system state is then mapped either to a single-ended or differential output. This mapping also adds bias points and common mode behavior, which are faithfully reproduced by the model. The use of multilayer perceptron ANNs with two hidden layers to reflect the nonlinear characteristic of the oscillator allows for an accurate and easily applicable modeling of rather complex oscillators. This provides the capability to model oscillators where the system response is modified by a control voltage (model of a VCO).
To include phase noise in the model and to start the oscillation in a well defined manner, a random signal is injected to an artificial noise port of the oscillator.
In order to describe this novel approach in sufficient detail, the remainder of this chapter is structured as follows: Section 8.2 introduces the theory of nonlinear oscillations, multilayer perceptron neural networks and the state space representation of nonlinear systems. Section 8.3 details the different aspects of the novel modeling technique, notably the structure of the model, the way in which phase noise is injected and the generation of data that is well suited to make the neural network represent the nonlinear behavior of the oscillator. Furthermore, the modeling flow is presented. Section 8.6 contains results that show the capabilities and performance of the model. A conclusion is drawn in chapter 9.

8.2 THEORETICAL BACKGROUND

8.2.1 *System Description in State Space*

A nonlinear, time-invariant, deterministic system can be mathematically described by a state equation

$$\dot{\mathbf{x}}(t) = \frac{d\mathbf{x}(t)}{dt} = \boldsymbol{\phi}\left(\mathbf{x}(t), \mathbf{u}(t)\right) \tag{8.1}$$

that characterizes the dynamics of the system state $\boldsymbol{x}(t)$, and an output equation

$$\mathbf{y}(t) = \boldsymbol{\psi}\left(\mathbf{x}(t), \mathbf{u}(t)\right) \tag{8.2}$$

that maps $\boldsymbol{x}(t)$ to the system's output vector $\boldsymbol{y}(t)$ of size N_y. The vector $\mathbf{u}(t)$ contains the N_u scalar inputs of the system. The N_x-dimensional

space on which $\mathbf{x}(t)$ is defined is called the system's *state space*. The vector function $\boldsymbol{\phi}(\,)$ describes the nonlinear relationship between the system state and its derivative. Because $\dot{\mathbf{x}}(t) = \frac{d\mathbf{x}(t)}{dt}$ describes the dynamical evolution of the states in direction and magnitude, it is also called the *velocity vector*. The vector function $\boldsymbol{\psi}(\,)$ contains the relationship between system state and system output.
If a system's state is known at one point in time, all its future states and outputs are defined by the state equation and the future inputs of the system. While in an input-output system (like a mixer or an amplifier) the influence of the inputs on the system state is dominant, the evolution of an oscillator's state depends primarily on its former states. An input is only needed to start the oscillation by deviating the system from its singular point at $\dot{\mathbf{x}}(t) = \mathbf{0}$.
Equation (8.1) is a system of mutually coupled ODEs. To put an Nth order ODE into the form of (8.1), the states $x_n(t)$ are assigned to the sought-after function $v(t)$ and its $N-1$ derivatives according to

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ \vdots \\ x_N(t) \end{bmatrix} = \begin{bmatrix} v(t) \\ \dot{v}(t) \\ \vdots \\ v^{(N-1)}(t) \end{bmatrix}. \tag{8.3}$$

The notation $v(t)^{(N)} = (dt)^N/(d)^N v(t)$ is used. This results in the state equation

$$\begin{bmatrix} \dot{x}_1(t) \\ \vdots \\ \dot{x}_N(t) \end{bmatrix} = \begin{bmatrix} x_2(t) \\ \vdots \\ f(x_1(t) \dots x_N(t), \mathbf{u}(t)) \end{bmatrix}, \tag{8.4}$$

consisting of N scalar first-order ODEs, yielding the same solution for $v(t)$ as the initial Nth order ODE. The comparison of (8.1) and (8.4) shows that the vector function $\boldsymbol{\phi}(\,)$ is reduced to a scalar function $f(\,)$, because the first $N-1$ equations of (8.4) are trivial.
The state space representation lends itself to the use in the oscillator model, because its dynamics are described as a system of mutually coupled ODEs, and thus it is straight-forward to implement in VHDL-AMS. Furthermore, it provides an intuitive perspective on how to correctly model an oscillation and allows the visualization of the system behavior by plotting its trajectories in state space. These trajectories are an ideal aid when training the neural networks used to represent the circuit's nonlinearities (cf. section 8.4.1).

8.2.2 *Nonlinear Oscillators*

To describe the behavior of an electrical oscillator, nonlinear autonomous ODEs can be employed. To illustrate the behavior of the oscillator, it is instructive to consider its trajectory in the phase plane, where the oscillator voltage is plotted on the abscissa and its first derivative on the ordinate. The phase plane corresponds to the two-dimensional state space of an oscillator. The evolution of the states is represented by the tangent vector on the trajectory and thus equivalent to the velocity vector $\dot{\mathbf{x}}(t)$. Due to the autonomous nature of the considered ODEs, the trajectories are independent of time.
The phase space trajectories of electrical oscillations exhibit two characteristic equilibrium states: The first one is an unstable singular point

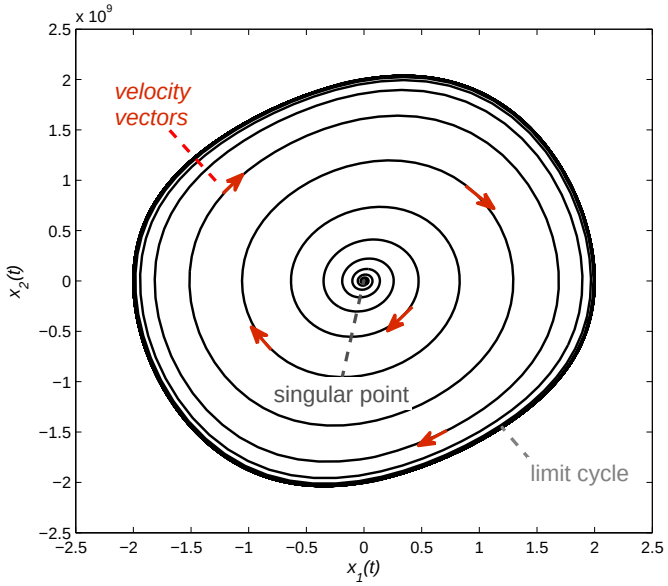


Figure 8.1: Plot of the trajectory of a Van der Pol-oscillator, simulated in VHDL-AMS. Singular point $\dot{\mathbf{x}}(t) = 0$ for $\mathbf{x}(t) = 0$.

at $\mathbf{x_{start}} = \mathbf{x}(t_0)$, where the velocity vector $\dot{\mathbf{x}}(t_0)$ is 0. This point corresponds to the bias point of the oscillator, with $x_{start,1} = v_{bias}$. Due to the instability of this point, any small deviation will lead to the start of the oscillator. The trajectory of the oscillation's start-up has a spiral form, where the mean distance of $\mathbf{x}(t)$ from the singular point, which corresponds to the oscillation's amplitude, is increasing with time (cf. Fig. 8.1).
The second equilibrium state is an attractive limit cycle, resulting from the limitation of the oscillation amplitude. This is a periodic orbit which all trajectories approach for $t \to \infty$. The basin of attraction, i.e. the area in state space that leads to oscillations ending on the limit cycle, contains the whole inside of the limit cycle, and at least the vicinity of the outside of the limit cycle that can be reached due to external influence, like noise. Otherwise, small deviations from the limit cycle that lead to an increased amplitude of oscillation would yield the system state to leave the limit cycle and be attracted by an other equilibrium state. While this behavior is not critical in real systems, it can occur in improper models. Thus it is important to pay attention to this effect (cf. section 8.4.4).
Note that the above explication applies only in the case of soft startup conditions. For further details on the theory of nonlinear microwave oscillators, refer to [302, 303].

8.2.3 *The Van der Pol-Oscillator*

To illustrate the theory of nonlinear electrical oscillations, the equation proposed by Van der Pol [298] to describe triode oscillators is used. The classical formulation is

$$\ddot{v}(t) = \alpha \left(1 - v(t)^2\right) \dot{v}(t) - \omega^2 v(t). \tag{8.5}$$

By defining the state vector of the Van der Pol-oscillator as

$$\begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} = \begin{bmatrix} v(t) \\ \dot{v}(t) \end{bmatrix}, \tag{8.6}$$

equation (8.5) can be rearranged to yield the velocity vector

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \begin{bmatrix} x_2(t) \\ \alpha\left(1 - x_1(t)^2\right) x_2(t) - \omega^2 x_1(t) \end{bmatrix}. \tag{8.7}$$

Because the system output is equivalent to the first state variable $x_1(t)$, the output equation reduces to

$$[y_1(t)] = [x_1(t)]. \tag{8.8}$$

From (8.5)-(8.8) it is clear that, besides the system's states, inputs and outputs, only the function $f(t) = \alpha\left(1 - x_1(t)^2\right) x_2(t) - \omega^2 x_1(t)$ is necessary to describe the behavior of the triode oscillator.
To illustrate the two equilibrium states of the Van der Pol-oscillator, the trajectory of one solution (calculated by a simple VHDL-AMS model) is given in figure 8.1.

8.2.4 *Model-Order Reduction*

In the case of the Van der Pol-oscillator, the differential equation is based on a polynomial approximation of the triode's anode current. This association of the circuit's complete nonlinearity to a single component is not feasible for an integrated microwave circuit, where the influence of a multitude of components (i.e. nonlinear capacitances, etc.) create the nonlinearity.
The complete state space representation of an integrated oscillator can be obtained from its schematic. To represent the circuit's behavior at microwaves correctly, this schematic has to include the parasitic elements extracted from layout. The order N of such a circuit is given by the number of its independent LC energy storages. The model of a complex oscillator taking into account all its parasitics therefore exhibits a large order ($N >> 100$). When using this kind of state space model, all currents and voltages inside the circuit are known, which is essential during circuit design.
However, the internal states of the system are not important for system level simulations, as long as their influence on the output is taken into account by the simplified model. Thus, even if the same accuracy at the system outputs must be maintained, a great order reduction is possible by removing the relationship between system states and energy storage elements.
The discussion of the Van der Pol-equation in section 8.2.3 shows that the trajectory of an oscillation can be described in a two-dimensional state space. This can be illustrated by the fact that the oscillation physically consists of the periodic exchange of energy between two dominant energy storages. This reasoning leads to the conclusion that the system order of an oscillator can in general be reduced to two. Thus, an embedding approach to find the intrinsic system order as described in [299] is usually not necessary.
Note that the modeling technique described in this paper can easily be extended to yield higher order models, if for a particular oscillator it turns out that an order reduction to more than two is more adequate.

However, for a properly designed oscillator a reduction to two should be possible.
As the observable second order dynamics of the oscillator are included in the output and its derivative, it seems sensible to use them as system states as in the case of the Van der Pol-equation. This works well for single-ended oscillators. However, when dealing with two related outputs as for differential oscillators, the system state needs to be defined in a way that it can be mapped to the two outputs equally well. If each output and its first derivative were defined as individual system states, the modeling of the interaction between the outputs would be hardly possible. Thus, these two cases have to be distinguished:

1. **Single-ended oscillator:** Figure 8.2 shows the schematic of a typical single-ended Colpitts VCO. Analog to (8.6), the output voltage and its first derivative can be used as its reduced states:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} = \begin{bmatrix} v_{out}(t) \\ \dot{v}_{out}(t) \end{bmatrix}. \tag{8.9}$$

   Similar to the Van der Pol oscillator, the state equation is then given by

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \begin{bmatrix} x_2(t) \\ f(x_1(t), x_2(t), \mathbf{u}(t)) \end{bmatrix} \tag{8.10}$$

   and the output equation is simply the first line of (8.9), i.e.

$$[y_1(t)] = [x_1(t)]. \tag{8.11}$$

   The scalar function $f()$ describes the nonlinearity of the oscillator and takes as arguments both the system states and the input vector $\mathbf{u}(t)$ that contains the oscillator's inputs like the noise current $i_n(t)$ and the control voltage $v_{control}(t)$ (cf. section 8.3.1). Due to the simple output equation, a second non-linear function that maps the oscillator's states to its output is not necessary.

2. **Differential oscillator:** To model both even and odd mode of a differential oscillator, two outputs need to be defined. If each of them is modeled individually as in the single-ended case, four system states result. In addition to this increased number of system states, their phase relation is undefined. The result is a

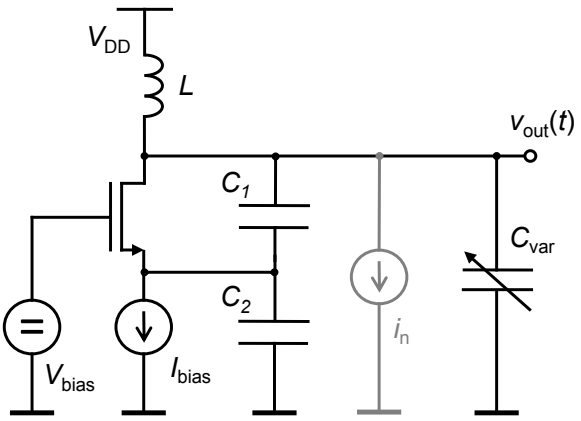


Figure 8.2: Simplified schematic of a typical single-ended VCO

model that is not capable of correctly representing the oscillator's behavior.
To avoid this problem, the two system states for the differential oscillator's behavioral model are based on its odd mode: the differential output voltage $v_y(t) - v_x(t)$ and its derivative are selected to represent the system state according to

$$\begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} = \begin{bmatrix} v_y(t) - v_x(t) \\ \dot{v}_y(t) - \dot{v}_x(t) \end{bmatrix}. \tag{8.12}$$

The advantage of this choice is the observability of the system's state from the output port of the oscillator. Furthermore, this state is related to both of the outputs in the same way. The output voltages $v_y(t)$ and $v_x(t)$ are illustrated in figure 8.3 in the VCO taken as example for the differential case throughout this paper.

The dynamics of the system state $\mathbf{x}(t)$ are then given by the velocity vector

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \begin{bmatrix} x_2(t) \\ f(x_1(t), x_2(t), \mathbf{u}(t)) \end{bmatrix} \tag{8.13}$$

that contains the scalar function $f()$ to describe the circuit's non-linearity as in the single-ended case.
The output equation for this reduced order oscillator maps the two states to the oscillator's outputs, while taking into account the parameters and inputs from $\mathbf{u}(t)$ according to

$$\mathbf{y}(t) = \boldsymbol{\psi}(x_1(t), x_2(t), \mathbf{u}(t)). \tag{8.14}$$

The system's output vector contains the nodes of the oscillator observable at the output of the behavioral model. The elements

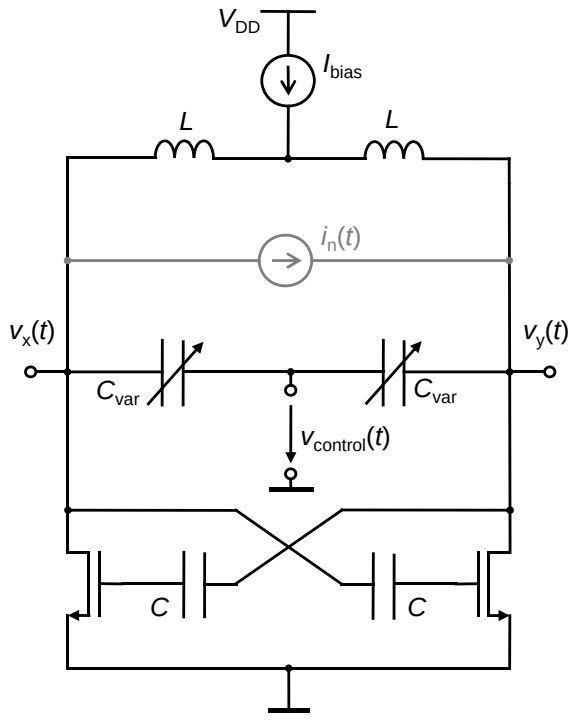


Figure 8.3: Simplified schematic of a typical integrated state-of-the-art VCO with differential outputs

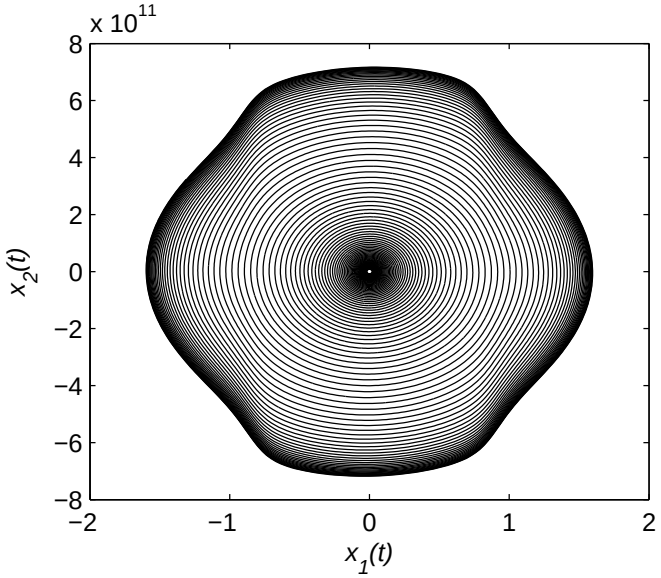


Figure 8.4: Trajectory of a 60 GHz differential Colpitts oscillator in the two-dimensional state space as defined in (8.12)

of $\mathbf{y}(t)$ are the voltages at both outputs of the oscillator (called x and y), thus forming the vector

$$\mathbf{y}(t) = \begin{bmatrix} v_x(t) \\ v_y(t) \end{bmatrix}. \tag{8.15}$$

Note that these outputs contain both even and odd mode of the oscillator, while the former one is not directly embodied by a system state, but added by the mapping in (8.14).

Mathematically, the order reduction from N to two can be seen as a projection of the oscillator's trajectory from the initial, N dimensional state space to the two-dimension state space of the behavioral model. By this projection, the relationship between system states and circuit components is removed and information about the original, circuit-related states of the oscillator is lost. Plotting the two newly defined states of the oscillator helps to verify that the new state space still contains a trajectory correctly describing the oscillation. If the trajectory is not intersecting with itself, and still shows the typical form of figure 8.1, the order reduction is valid.

An example for a trajectory obtained from simulations using the microwave circuit simulator ADS[1] is given in figure 8.4. The oscillator is a differential Colpitts VCO having the simplified schematic given in figure 8.3. The reduced states of the oscillator are calculated according to (8.12) from the output voltages of the ADS simulation. The higher complexity of this oscillator is reflected by the form of its limit cycle: It shows a more irregular shape compared to the limit cycle of the Van der Pol oscillator displayed in figure 8.1 (which is due to the fact that the drain-source saturation voltage of the transistors cannot fall below a certain value). Thus, the trajectory exhibits a dent at each side of the rectangle.

Even the behavior of highly nonlinear oscillators can be described in a

[1] ADS 2005A, copyright 2005 by Agilent Technologies

two-dimensional state space, however, the form of its trajectory becomes more difficult to approximate and depends heavily on parameters like the control voltage. For this task, the simple second-order polynomial of the Van der Pol-equation is insufficient. In the proposed model it is replaced by a function that contains the relevant nonlinearities of the employed transistors and varactors, including large-signal effects like the transition from one operating region to another or nonlinear capacitances.

8.2.5 *Artificial Neural Networks*

Due to the ease of their parametrization and the accuracy they yield when approximating non-linear functions, Artificial Neural Networks (ANNs) are employed in the proposed model. They are used to describe the oscillator's nonlinear behavior which is represented by the scalar function $f(\,)$ in (8.10)/(8.13) and the vector function $\boldsymbol{\psi}()$ in (8.14). This section briefly introduces them.

8.2.5.1 *Multilayer perceptrons*

An ANN is a structure that resembles the human brain in containing neurons (i.e. nodes) interconnected by synapses (i.e. connections) in order to build a complex structure that is capable of reproducing sophisticated relationships.
A class of artificial neural networks that can be employed to perform a nonlinear input-output mapping of general nature is a Multilayer Perceptron (MLP) [304]. It can thus approximate the nonlinear vector functions $\boldsymbol{\phi}(\,)$ and $\boldsymbol{\psi}(\,)$ of equations (8.1) and (8.2), and more specifically the scalar function $f(\,)$ of (8.10) and (8.13).
The MLP's input consists of source nodes that correspond to the arguments of the function $f(\,)$ it approximates. One or more hidden layers create the computational power of the network. Furthermore, one or more output nodes constitute the output layer and correspond to the function value(s) of $f(\,)$.
The three distinctive properties of an Multilayer Perceptron (MLP) are [304]:

- It contains a nonlinear activation function to calculate the neuron values. This function introduces the nonlinearity of the MLP and needs to be smooth in order to create a network that can be trained by the error back-propagation algorithm (cf. section 8.2.6). A common choice is the hyperbolic tangent $\tanh()$. It exhibits a smooth transition from -1 to $+1$. As a consequence the outputs of the MLP need to be normalized to this range. Furthermore, it is convenient to also normalize the inputs, especially when using the ANN to model mm-wave oscillators, where otherwise the different inputs exhibit totally different orders of magnitude.
- It possesses one or more hidden layers, that are not directly accessible from the outside.
- It contains a high degree of connectivity. Each node is connected to every node in both the preceding and the following layer by weighted synapses.

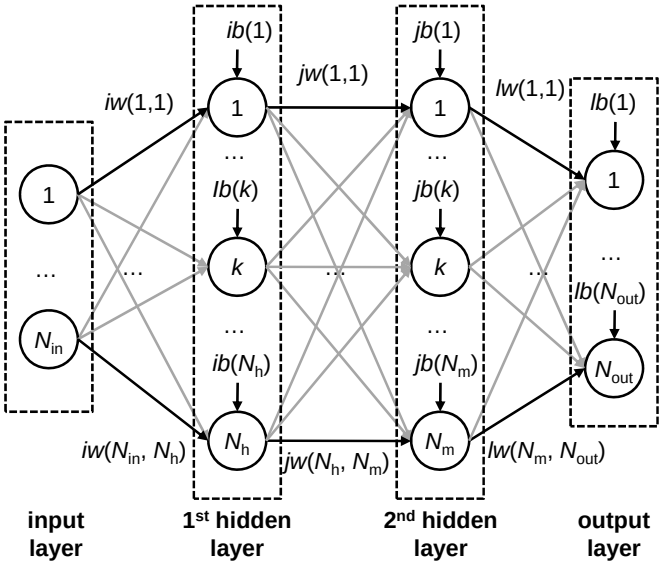


Figure 8.5: Schematic of a multi-layer perceptron with two hidden layers.

The structure of a multilayer perceptron network with two hidden layers is sketched in Fig. 8.5. The neuron values within this structure are calculated by

$$n(k) = \tanh\left[\sum_{j=1}^{M}(n_{in}(j)w(j,k)) + b(k)\right] \tag{8.16}$$

with $n_{in}(j)$ being the jth neuron of the precedent layer containing M neurons, $w(j,k)$ being the weight assigned to the path from this neuron to the current one, and $b(k)$ its bias value. Knowing its weights and biases and as well as, if applicable, the normalization factors completely characterizes the MLP.

8.2.5.2 *Neural networks to approximate nonlinear functions*

To approximate an arbitrary continuous function it is sufficient to use a MLP with only one hidden layer, provided its number of neurons is sufficiently large. This is the essence of the universal approximation theorem for nonlinear input-output mapping [305] applied to MLPs. However, it is only an existence theorem and does not guarantee that a solution with one hidden layer is the most practical or even optimum one. In fact, when using only one hidden layer the neurons of the MLP tend to interact with each other globally. Thus, when approximating functions like the one present in an oscillator, the improvement of one point in the approximation will typically lead to the worsening of another one [304].
To avoid these kinds of problems, two hidden layers are advantageous. Here, the first hidden layer typically reproduces the local behavior, while the second hidden layer contains global features of the function to be approximated. Thus, curve-fitting becomes more manageable.
That is why MLPs with two hidden layers are recommended to approximate the function $\boldsymbol{\phi}(\,)$ and $f(\,)$, respectively. Only for the weakly nonlinear function $\boldsymbol{\psi}(\,)$ that maps the system state to the system output, and for simple single-ended oscillators MLPs with a single hidden layer

are advantageous to avoid increased complexity.
The necessary number of neurons N_h in the first and N_m in the second hidden layer depend much on the peculiarities of the oscillator to represent and are thus determined empirically: In the training process, these numbers are decreased iteratively until the maximum desired Mean Squared Error (MSE) is exceeded. This is necessary because the complexity of the function to approximate is not easily quantified and converted to the number of required neurons.

8.2.6 *Training by Error Back-Propagation*

The learning process (i.e. training of the neural network) may be viewed as a curve fitting problem [304]: During training, the weights and biases of the ANN are adjusted in order to enable the ANN to perform a desired input-output mapping (e.g. the function $f(\,)$ of (8.10)/(8.13)). A training data set containing input-output pairs is presented to the ANN for this purpose. In addition to approximating the mapping for each input-output pair, the ANN will also generalize the training data and thus be able to map inputs never presented in the training process to their appropriate outputs.
A popular method to train an MLP is error back-propagation. The general algorithm works as follows: First, the weights ($iw(k), jw(k)$ and $lw(k)$) and biases ($ib(k), jb(k)$ and $lb(k)$) are initialized by random values. Next, the output of the MLP is computed based on the input part of the training data. Then, the error between the output from the training data set and the calculated output is determined.
Next, it needs to be determined to what degree this error can be assigned to which weight or bias-values. To be able to do this, local gradients are introduced that contain the influence of each precedent node to the error at the actual node. Because the error is known directly only at the output layer, it has to propagate backwards into the network to determine the error at the neurons in the hidden layers. After the influence of each weight and bias on the error is determined, they are adjusted accordingly. The error back-propagation process is repeated until a given criteria (e.g. MSE below a certain bound, gradient below a certain bound, maximum iteration count, etc.) is reached. Further details on this method are given in [304].
Note that the design of the training data set is an essential part of the training process. The MLP can only approximate and generalize a behavior it is trained to before. In section 8.4 this issue is discussed with respect to the oscillator model.
While the calculation of the output values of the MLP as a function of the inputs and net parameters, sometimes referred to as forward propagation, constitutes an integral part of the VHDL-AMS model, the training procedure has only to be done once to build the oscillator model. The convenient tools of the Matlab Neural Networks Toolbox[1] have been employed to train the MLP using the Levenberg-Marquardt back-propagation algorithm.

[1] Matlab R2007a, copyright 1984-2007 by The MathWorks

8.2.7 *Drawbacks*

The neural network architecture used to represent the nonlinearities works perfectly fine with respect to accuracy of approximation and manageability. Nevertheless, it exhibits two weaknesses. The first one originates from the fact that the parameters are determined by a training process: to get a good approximation by the neural network, several training runs starting from random initial values have to be compared. Based on this, the network having the minimum MSE is picked. Thus, the optimal solution is not found in a deterministic way, and though the MSE of this solution is small, one can not be sure where this error will occur and how well the network will generalize behavior it is trained on. This is not the case for a physical model.
Second, the solution of a system of equation that contains perceptron neural networks with hyperbolic tangent basis functions is more computationally intensive then for example an approximation that contains polynomials or radial basis functions. So for less stringent accuracy requirements, an approximation using this kind of functions may be the better choice.

8.3 THE NOVEL MODELING-APPROACH

The behavioral modeling methodology based on the theoretical background presented in the previous section is applicable to a large variety of LC-oscillators. Two representative examples, one given by the single-ended circuit in figure 8.2, the other by the differential VCO of figure 8.3, are used in the following to illustrate the proposed methodology.
Especially the latter circuit exhibits all important characteristics of a state-of-the-art VCO: It is fully differential, with outputs $v_x(t)$ and $v_y(t)$. The tank is comprised of symmetrical inductors L and varactors C_{var}, whose capacitance values are controlled by $v_{control}(t)$. A cross-coupled Colpitts architecture is used, recognizable by capacitive voltage dividers comprising the capacitors C and the gate source capacitances C_{GS} of the MOSFETs. The VCO is designed to exhibit an oscillation frequency around 60 GHz.
The current source $i_n(t)$ that is visible in the schematics of both oscillators is not present in the original design. It is added as a means to inject a small, noise-like signal into the tank. This signal serves several purposes: It starts the oscillation in a more controlled way then numerical inaccuracy would, it can be used to generate more robust training data by varying the trajectory of the oscillator (cf. section 8.4), and it creates a port at which to inject noise to the tank in order to generate phase noise in the $1/f^2$ region (cf. section 8.3.2).
Note that a complete schematic of an oscillator that is used for low level simulation (e.g. in ADS or SPICE) would include a more complete biasing network, possible output buffers, inductors and/or transmission lines for matching and all the parasitics being extracted from layout. The novel model is created to exhibit the behavior of this entire circuit.

8.3.1 *Model Structure*

The model structure for single-ended and differential oscillators are different as a consequence of the difference that exists between their state space descriptions given in section 8.2.4.

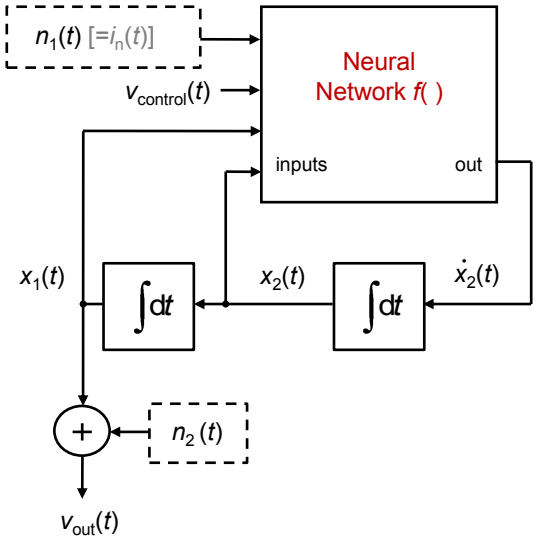


Figure 8.6: Block diagram of the oscillator model for the case of a single-ended output and one control input ($v_{control}(t)$). Blocks with dashed margin represent white Gaussian noise generators.

Figure 8.6 gives the model structure for the case of **single-ended oscillators** like the one of figure 8.2. The state equation (i.e. (8.10)) is represented by the upper part of the diagram: The output of the ANN is fed back to its inputs using two integrator blocks that embody the derivatives of the differential equation. The neural network employed in this part incorporates the strong nonlinearity, which is mathematically contained in the function $f()$. In addition to the two state variables, the ANN has two other inputs, represented by the input vector

$$\mathbf{u}(t) = \begin{bmatrix} v_{control}(t) \\ i_n(t) \end{bmatrix}. \tag{8.17}$$

The input $v_{control}(t)$ is the control voltage applied to change the capacitance of the varactors. The model will be capable of representing the influence of this voltage not only on the oscillation frequency, but also on any other properties of interest (e.g. the tank amplitude or the startup time). It is the only external input in this example, but similar inputs are possible to represent model parameters like the bias currents of the circuit. However, the number of inputs should be limited to those present in the fabricated circuit. Otherwise the reduction of computation time with respect to a circuit level model is low, which reduces the interest of employing the behavioral model.
Input $n_1(t)$ corresponds to the artificial current source $i_n(t)$ inserted into the schematic. In the VHDL-AMS model this input of the ANN is connected to a random number generator that creates white Gaussian noise of standard deviation σ_1 (cf. section 8.3.2).
Consistently with (8.11) the single-ended oscillator's output voltage is directly derived from the first system state. However, white Gaussian noise of standard deviation σ_2 is added to the output voltage in order to emulate the noise floor (cf. section 8.3.2).

The structure of the proposed model for **differential oscillators** is presented in figure 8.7. The diagram given there is adapted to VCOs like the one of figure 8.3. The comparison to the structure of the model

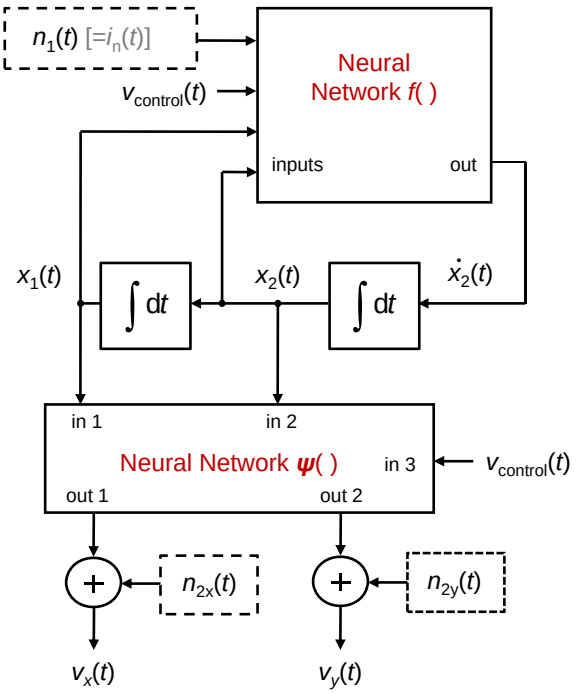


Figure 8.7: Block diagram of the oscillator model for the case of differential outputs ($v_x(t), v_y(t)$) and one control input ($v_{control}(t)$). Blocks with dashed margin represent white Gaussian noise generators.

for a single-ended oscillator shows that the part that embodies the state equation stays the same. However, a second artificial network is added to implement the nonlinear function $\psi()$ used for the output mapping described by (8.14). The block diagram for this part does not contain feedback: The states $x_1(t)$ and $x_2(t)$ are simply mapped to the output voltages, which results in less stringent accuracy constraints for the ANN employed. The third input represents any influence of the control voltage on this projection. It is equivalent to the input of $f()$ of the same name.
The blocks with dashed outlines in figure 8.7 contain the noise signals $n_{2x}(t)$ and $n_{2y}(t)$. They add white Gaussian noise of standard deviation $\sigma_{2x} = \sigma_{2y} = \sigma_2$ to the differential output voltages in order to emulate the noise floor (cf. section 8.3.2).
The central role of the states $x_1(t)$ and $x_2(t)$ becomes obvious from this diagram: They are connected to both of the neural networks as well as the integrator blocks.

8.3.2 *Phase Noise Emulation*

Independently of the physical explanation that is employed, most theories about phase noise in oscillators (cf. [241] for an in-detail overview) assume that the phase noise spectrum can be divided into three regions as introduced by Leeson [237]. More precisely, a flat, $1/f^2$ and $1/f^3$ region are distinguished, corresponding to the asymptotic slope of their characteristic in the double logarithmic phase noise spectrum.
The present behavioral oscillator model is designed to emulate phase noise in the flat and $1/f^2$ region. At this stage, the model does not take into account the contributions creating the $1/f^3$ region, which would

translate into increased complexity.
For sake of simplicity, physical processes are not considered when building this part of the model. Rather, the original, more complex circuit model, or measurements of a realized oscillator (if available) are used do determine the actual phase noise characteristics. (Depending on the phase noise model used in the circuit simulation, more or less physical noise mechanisms are taken into account in the former case [241].)
From the phase noise spectrum obtained this way the different regions are identified, and the positions of the asymptotes characterizing them are extracted. Based on this knowledge, the phase noise part of the behavioral model is parametrized.
To inject noise that is transposed to phase noise in the $1/f^2$ region, a current source i_n is inserted in parallel to the tank of the oscillator, as illustrated in figures 8.2 and 8.3. If this source has the mean-square spectral density $\overline{i_n^2}/\Delta f$ and the tank impedance is $Z(\omega)$, this current source will yield a voltage v_n with mean-square spectral density

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f}\,|Z(\omega)|^2 \tag{8.18}$$

that is superimposed on the tank voltage v_{tank}.
Assuming that the tank impedance consists of the total tank inductance L_{tot} in parallel with the capacitance C_{tot} (C_{tot} contains the varactor(s), the capacitive voltage divider, as well as all other parasitic capacitances), and any losses are exactly compensated by the active part of the circuit, the resulting tank impedance is given by

$$Z(\omega) = \frac{j\omega L_{tot}}{1-\omega^2 L_{tot} C_{tot}} = \frac{j\omega L_{tot}}{1-\left(\frac{\omega}{\omega_0}\right)^2} \tag{8.19}$$

with $\omega_0 = 1/\sqrt{L_{tot}C_{tot}}$ being the resonance frequency. When considering phase noise, the frequencies of interest are close to the carrier, so $\omega = \omega_0 + \Delta\omega$, where $\Delta\omega$ represents the small deviation from the carrier frequency. Thus, $Z(\omega)$ may be approximated by

$$Z(\omega) \approx \frac{j\omega_0^2 L_{tot}}{2\Delta\omega}, \tag{8.20}$$

neglecting all small and higher order components.
As a result, the mean-square spectral density of the tank voltage due to the injected current is

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f}\left(\frac{\omega_0^2 L_{tot}}{2\Delta\omega}\right)^2. \tag{8.21}$$

Due to the equipartition theorem of thermodynamics, half of this power density appears as phase noise. Because $\overline{v_n^2}/\Delta f$ is proportional to $1/\Delta\omega^2$, the spectrum generated by the considered signal can be used to emulate the $1/f^2$ region. The initially flat noise current density is shaped by the filtering due to the LC-tank [133].
To generate the current density $\overline{i_n^2}/\Delta f$, a random number generator is used. It generates a normal distributed random variable with zero mean and standard deviation $\sigma_I^2 = \overline{i_n^2}$. To correctly fix the position of the asymptote for the phase noise in this region, it is thus sufficient to

fix the standard deviation σ_1.
A VHDL-AMS implementation of a random number generator for normal distributions can be found e.g. in [306]. It makes use of the `UNIFORM` - function provided by VHDL-AMS that can generate only uniformly distributed random variables, and converts them to normally distributed ones.
To add a noise floor to the oscillator output, the same type of random number generator, parametrized by the standard deviations σ_2, is used (in the case of the differential oscillator, two uncorrelated noise generators with standard deviations $\sigma_{2x} = \sigma_{2y}$, one for each output, are necessary). Because the shape of their noise spectrum is already flat as required for the noise floor, no special injection is needed. Thus, the noise can simply be added to the outputs of the oscillator as indicated in figures 8.7 and 8.6. The equipartition theorem holds here as well, which means that half of the added noise power is actually phase noise.

8.3.3 *Modeling Flow*

The modeling flow presented in this section assumes that the structure of the particular model has already been established, i.e. that the inputs, outputs and states of the reduced order model are defined and the number and kinds of neural networks are fixed. To create a model according to such a structure, several steps are necessary, as illustrated in figure 8.8.

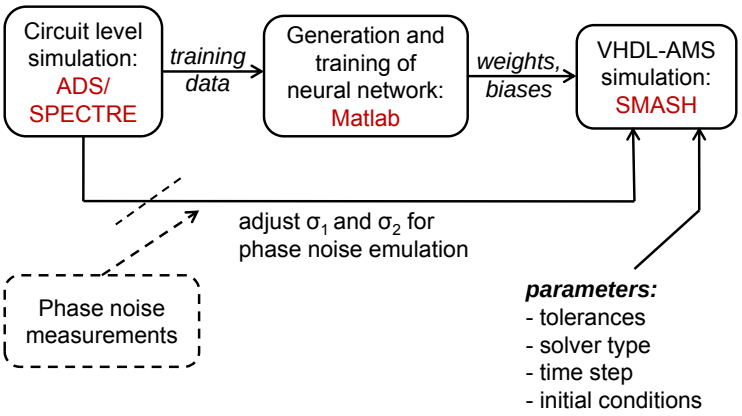


Figure 8.8: Modeling flow: from circuit level simulation to behavioral model

The model is based on an accurate, but rather complex circuit level model. This model is used to generate a dataset able to characterize the oscillator in all relevant states according to section 8.4. The dataset is imported to Matlab, where it is used to train the neural networks that constitute the nonlinearities of the model using the backpropagation algorithm previously described. Then the parameters of these neural networks are written to a datafile in an appropriate format. This datafile is then imported by a subroutine of the VHDL-AMS model, which uses the contained data to rebuild the mathematical representation of the neural networks according to (8.16).
To determine the standard deviations of the noise sources, either a phase noise simulation or, if available, phase noise measurements can be used. These standard deviations are entered directly as parameters to the VHDL-AMS model and will be used to create the random numbers

according to 8.3.2. Before running the simulation based on this model, important parameters of the simulation need to be set (cf. chapter 8.5).

8.4 PARAMETRIZATION OF THE MODEL

To match the model to a given circuit, the parameters of the neural networks representing $f(\,)$ and $\psi(\,)$ have to be found. This is done by fitting their response to a data set generated by a circuit level simulation. The theoretical background of this training process is given in section 8.2.6. Another crucial part to get a working model is the proper design of the training data. This section gives guidelines to training data design and presents the training results for the ANNs employed in the example of a differential oscillator that has a simplified schematic like the one of figure 8.3. The exemplary VCO is parametrized to oscillate around 60 GHz. The training in the single-ended case works accordingly, with the difference that only the ANN to approximate $f(\,)$ is present.

8.4.1 *State-Space as Training Aid*

To approximate a function by a neural network, the ANN must yield the function value as output for all inputs of interest. These relevant inputs are located in a specific, limited area of the function's input space. The dimension of the input space is the number of scalar inputs of the function.
In the case of both the single-ended and differential oscillator model, the states $x_1(t)$ and $x_2(t)$ are inputs of the employed neural networks, as displayed in figures 8.6 and 8.7. The state space of the oscillator is thus a subspace of the neural networks' input spaces. That's why the state space representation of the oscillator's behavior is very well suited for training data design. Previous considerations show that all practical inputs of the neural networks are located inside or on the limit cycle of the oscillator's trajectory.
Besides the states $x_1(t)$ and $x_2(t)$, the neural networks can have other inputs that act as parameters. The only parameter in the present example is $v_{control}$. Thus, for all valid control voltages (here from 0 V to 1 V) the function must yield correct values in the above mentioned part of the oscillator's state space.
If several parameters are used, all valid combinations of them have to be taken into account for training. Generating a complete training data set thus becomes more difficult for models with increasing number of parameter inputs.
The artificial noise input can be treated less strictly: Because the excitations on this port are small compared to the states but have a similar influence on the output, it is not necessary to consider this input as a separate dimension. Nevertheless, some small noise-like signals should be injected at this port to match the responses of circuit and neural network on these kind of excitations.

8.4.2 *Interdependence of Inputs*

The straight-forward way to generate the necessary training data is to sweep the inputs to get a coverage of the whole valid input space and calculate the outputs given by the original circuit level model based on

them. However, as obvious from figures 8.6 and 8.7, the inputs (and in the case of function f() the output as well) are connected outside the neural network and are thus not sweepable independently. This fundamental difference compared to a neural network approximating simple input-output relationships necessitates a different approach to training data design. Furthermore, the inputs of the neural networks are not identical to the inputs of the system (they are rather states, which are chosen to be related to the output), so they are not accessible in the circuit simulator without changing the circuit response.
Independent input parameters like v_{control}, however, can be swept to generate training data for the whole range of valid values. With reasonable spacing between two discrete values, the whole parameter range can be covered by a reasonable number of simulation runs. In the example of v_{control}, generation of training data for the six values $0.0\,\text{V}, 0.2\,\text{V} \ldots 1.0\,\text{V}$ yields an accurate model for all valid control voltages as can be confirmed by looking at the outputs of the model for $v_{\text{control}} = 0.5\,\text{V}$ in chapter 8.6.

8.4.3 *Training by Varying Trajectories*

A typical startup trajectory of an oscillator covers more or less densely the inside and the rim of the limit cycle, as shown in figure 8.9. However, due to the high gain of the transistors used in the particular circuit producing this trajectory, large regions of the state space remain uncovered by training data.
While for small gaps the neural network interpolates the behavior of

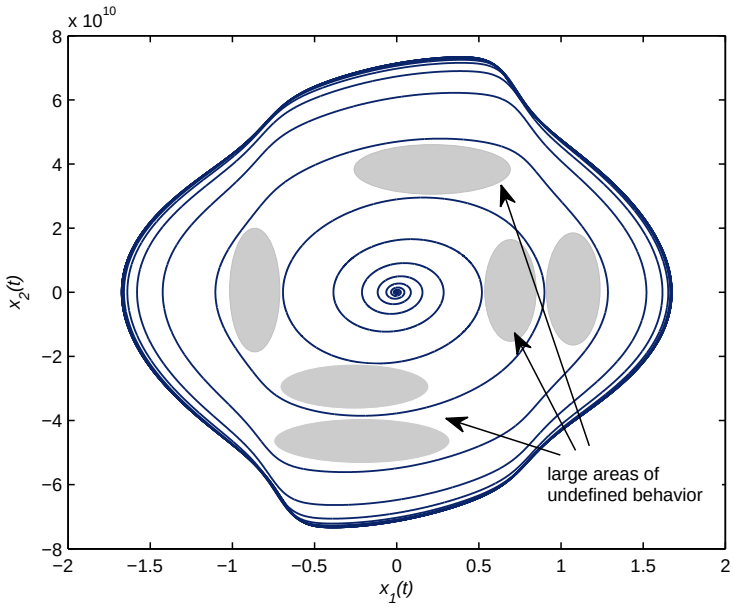


Figure 8.9: Trajectory of an oscillator with fast startup: large uncovered areas in the input space yielding neural networks poorly approximating the desired function.

the oscillator correctly, based on the provided training data, this is not true for large gaps: in the case of the second neural network, which is not part of a differential equation, this inaccuracy only increases the inaccuracy of the model output. The maximum error that can be

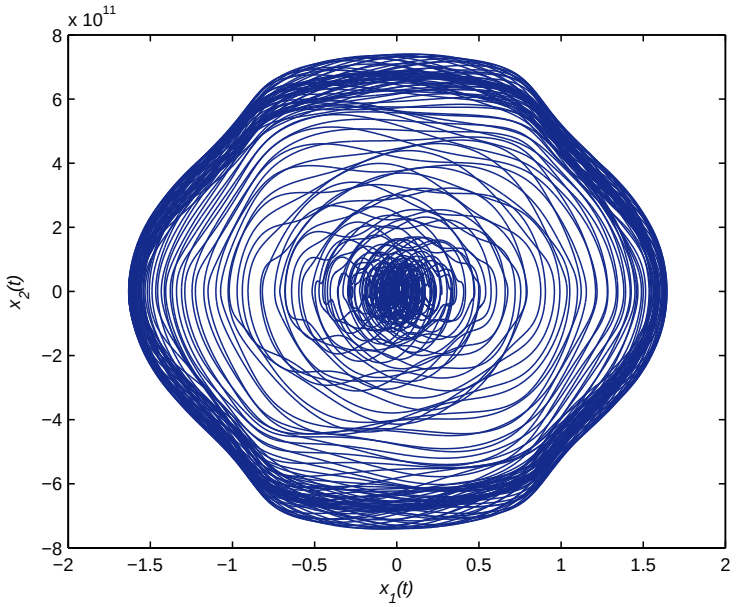


Figure 8.10: Dense trajectory due to the use of the artificial current source for injection of a current that influences the trajectory. The shown traing-data originates from several start-ups.

tolerated depends on the application.
For the neural network approximating $f()$, dense coverage is crucial though: this ANN is part of a differential equation whose solution at one time step mainly depends on the solution of the previous time steps (and its derivatives). Although small errors yield only a slightly inaccurate solution at one time step, these errors sum up over time, leading to a deviation from the valid trajectory. If the trajectory leaves the well characterized inside of the limit cycle, this can finally result in a complete failure of the solution.
Note that for oscillators with a slow startup this problem is less pronounced, because one startup contains many periods and thus densely covers the input space as shown in figure 8.4.
In order to generate dense training data from oscillators with fast transients, several startups are used. To change the conditions at and after startup in order to vary their trajectories, a high frequency, small amplitude signal can be injected to the artificial input port i_n (cf. figures 8.2 and 8.3). This signal must be differentiable, thus noise is not well suited. Either a sinusoid or a pulse train with smooth slopes may be used. As a result of this injection, used during several start-ups, a dense coverage of the input space is achieved as illustrated in figure 8.10. The neural network's response to excitations at this artificial port is matched to the circuit's response.

8.4.4 *Accuracy Issues*

Besides the dense coverage of the neural network's input space there are other important issues that have to be addressed during training in order to get an accurate, functional model.
As indicated in section 8.2.2, the behavior near the outside of the limit cycle has to be characterized as well. Otherwise, the differential equation can exhibit other, artificial attractors that are not present in the

real oscillator. These attractors can render the limit cycle unstable, in such a way that a large noise peak in steady state causes the oscillator to leave the limit cycle. To avoid this, the artificial input is used to generate steady state training data that deviates a certain amount from the ideal, noise-free trajectory. Thus, the function approximates the oscillator's behavior even in areas of the state space that are rarely encountered.
A potential source of inaccuracy is the error already present in the data used for training the ANN. All the more, because during the development of the oscillation an insignificantly small error amplifies and becomes considerable. To keep the error present in the training data set small, the circuit simulator needs to use extremely tiny time steps and small internal tolerances.
In this context, the accuracy of the derivatives that relate $x_2(t)$ to $x_1(t)$ and $\dot{x}_2(t)$ to $x_2(t)$ are of utmost importance. Because a forward difference approach needs an impractically small time step to yield small errors, a central difference is used to compute the derivatives. Note that numerical derivatives calculated by higher order differences are an option to minimize this error. The advantage is that their use does not slow down the VHDL-AMS model while improving model accuracy. Simple forward difference calculations yield errors as large as some ten millivolts with time steps of only some femtoseconds in the 60 GHz oscillator example, so they must be avoided.
Overtraining of the neural network also can become an issue: If the same set of training data is presented repeatedly during the training process, the neural network tends to specialize on this data, and thus looses its generalization property [304].

8.4.5 *Training Results*

The two networks of the model of the 60 GHz differential VCO are trained using training data prepared according to the guidelines provided in the previous sections. The data is obtained from ADS simulations. The number of neurons is determined experimentally to get a mean squared training error (MSE) in the range of 10^{-5}. Note that this accuracy can be improved by increasing the number of nodes. However, the optimum parameter set is then more difficult to find, and the training process takes more resources. Furthermore, an even better accuracy conflicts with the goal to achieve complexity reduction by means of the behavioral model.

8.4.5.1 *Neural Network to Represent* $f()$

The neural network to represent $f()$ uses 15 neurons in the first and 10 neurons in the second hidden layer. It achieves an MSE of $1.25 \cdot 10^{-5}$ with respect to the training data presented. The training data consists of six startup trajectories with different control voltages and modulated artificial input current, plus one frequency sweep done by increasing v_{control} continuously from 0 V to 1 V.
Figure 8.11 compares the response of the neural network for $v_{\text{control}} = 0\,\text{V}$ to the trajectory of a startup that ends in steady state. They correspond very closely to each other, illustrated by the fact that the trajectory is in some places slightly above and in other places slightly below the plane that represents $f()$.
Figure 8.12 shows the output of the neural network versus the used

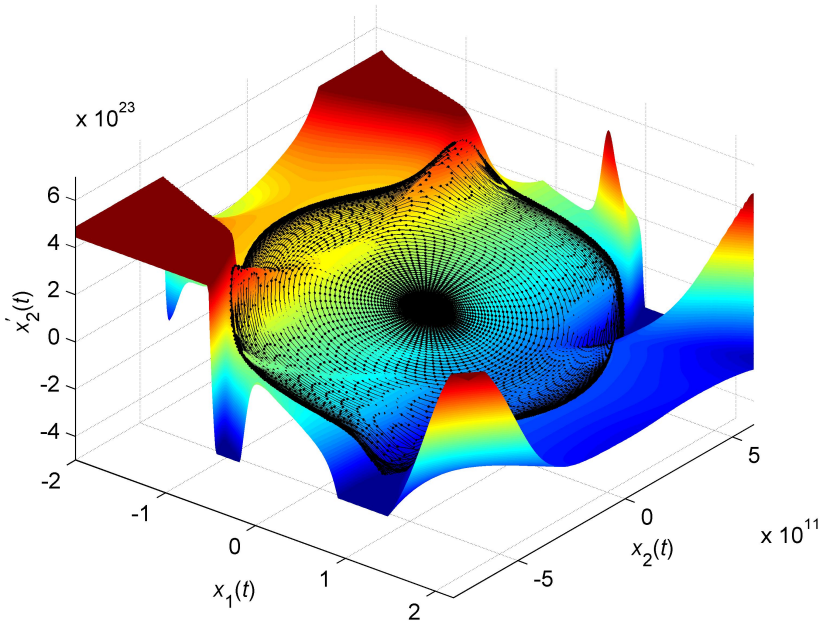


Figure 8.11: Function $f()$ approximated by the neural network (colored plane) versus trajectory used to train it (solid line with dots to indicate actual values), $v_{control} = 0\,V$.

training data over time for two different control voltages in steady state. Excellent agreement is observed, which confirms successful training for different control voltages. Higher maxima and a smaller period indicate the higher frequency of oscillation for $v_{control} = 1.0\,V$

8.4.5.2 *Neural Network to Represent* $\psi()$

The neural network to represent $\psi()$, i.e. the mapping from the system states to the two outputs, that is only necessary for a differential oscillator, contains a single hidden layer of three neurons. The training data used characterizes the same states of the oscillator as the one for $f()$. An MSE of $5.54 \cdot 10^{-6}$ is achieved.
In figure 8.13 its steady state response is shown. (Similar accuracy is achieved for the startup trajectory. It is not added to this graph for the sake of clarity.) The 180° phase difference between the v_x and the v_y output is graphically represented by the fact that the two quasi-planes containing the trajectories only intersect at the bias voltage $V_{bias} = 920\,mV$ and exhibit a symmetry to the plane $x_1(t) = 0$.

8.5 IMPLEMENTATION AND SOLVER ISSUES

The model structures according to figures 8.6 and 8.7 are implemented in VHDL-AMS. The results in section 8.6 are obtained from these implementations, which are detailed and illustrated by some code examples in appendix B. The simulation environment used is SMASH[1], which is chosen due to the particular requirements of the model (cf. section 8.5.1). An implementation of the model in other description languages

[1]SMASH 5.10.0, copyright 1992-2007 by Dolphin Integration

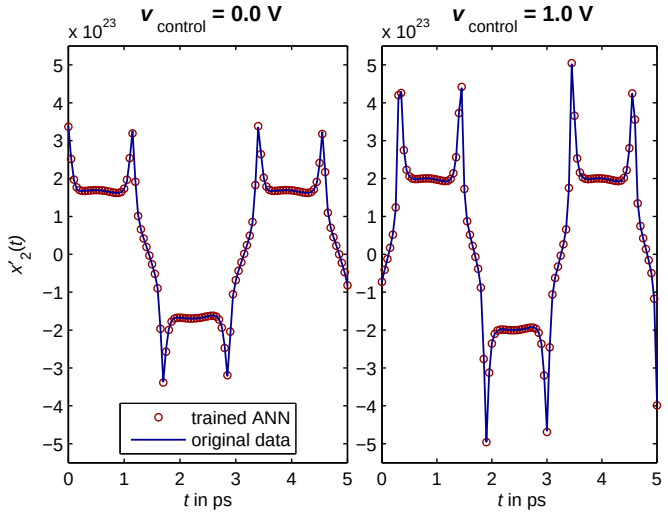


Figure 8.12: Original data (blue solid line) versus output of trained neural network (red circles) for two different control voltages (left: 0 V, right: 1 V)

and simulation environments is possible, as long as they provide similar directives and solver options as VHDL-AMS and SMASH.

8.5.1 *Solver Issues*

The correct numerical evaluation of the system of differential-algebraic equations described in VHDL-AMS demands several prerequisites. Otherwise, the simulation does not yield correct results despite perfect model equations.
First of all, the numerical algorithm employed has to be chosen wisely. While backward Euler or trapezoidal algorithms work only when using prohibitively small time steps, Gear's algorithm is stiffly stable [307] and works fine for a reasonable range of time steps (whose upper bound

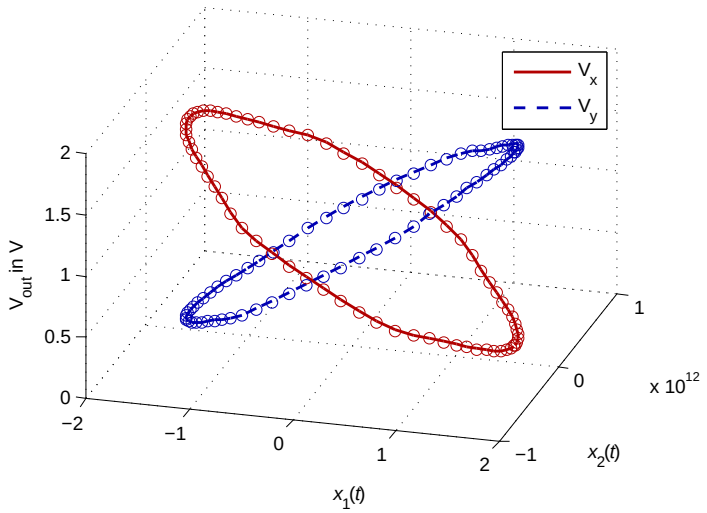


Figure 8.13: Mapping from the states x_1 and x_2 of the system to its output voltages (function $\psi(\,)$). dashed and solid line: original output, circles: output of neural network.

depends on the oscillation frequency). It is furthermore supported by the major simulation environments, among them SMASH.
Secondly, the operating point simulation needs to start from initial system states that lie inside the limit cycle. This ensures that the correct singular point that corresponds to the bias point of the oscillator is found. The reason for this is that the neural network representing the function $f(\,)$ is not trained far outside the limit cycle, and thus can exhibit artificial singular points there. Manually setting reasonable initial values for the state quantities remedies this problem.
The third issue concerns the tolerances maintained during the solution process. Due to the very high frequency mm-wave oscillators are working at, the states and their derivatives have largely different orders of magnitudes. For the 60 GHz VCO under consideration, $x_1(t)$ is of the order of 1 while $\dot{x}_1(t)$ is of the order of 10^{12}. Thus, the tolerances that need to be imposed on a quantity and its derivative are of totally different order of magnitude. To the best of the author's knowledge, SMASH is the only simulator that allows to set the tolerance value of the quantities and their derivatives independently. This is an essential feature without which it is not possible to solve the model equations correctly for mm-wave oscillators.

8.6 REALIZED MODELING EXAMPLES

This section gives three examples of the application of the proposed modeling technique to 60 GHz oscillators.

8.6.1 *Single-Ended Free-Running Oscillator*

The first validation of the proposed modeling approach is based on a single-ended 60 GHz Colpitts oscillator whose simplified schematic is the one given in figure 8.2. The implemented model structure corresponds to figure 8.6. However, as no voltage control is used, no inputs except the one for the artificial current $i_n(t)$ are required.
Due to the simplicity of this oscillator, an ANN with only one hidden layer consisting of 10 neurons proved sufficient to generate an accurate model. More details on the training of the ANN used for this model are given in [286], where this single-ended oscillator model is published.

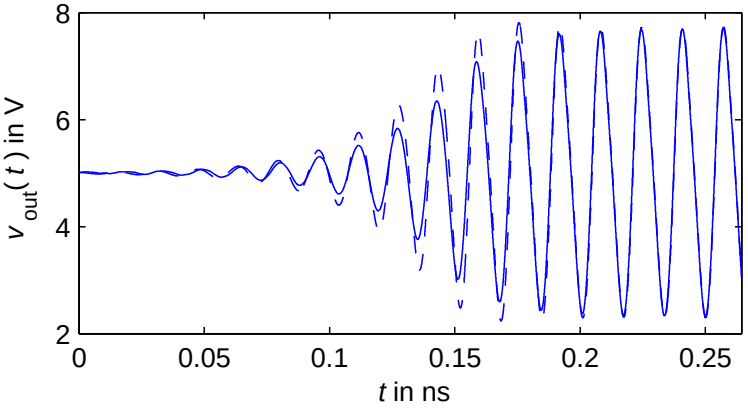


Figure 8.14: Startup of the single-ended oscillator: VHDL-AMS model (solid line) versus ADS response (dashed line)

In figure 8.14 the output waveform produced by the VHDL-AMS model is compared to the original ADS output. Their DC operation points correspond exactly, yielding a value of 5.0 V. The two signals slightly differ in the transient region, because the order N of the VHDL-AMS model is only two, which in this particular case is not sufficient to follow the small overshoot shown in figure 8.14. If the transient is to be simulated more accurately, N needs to be increased to three.
The steady state, however, is reproduced very accurately: The frequency is 61.08 GHz instead of 61.22 GHz in the original circuit, and the output voltage ranges from 2.32 V to 7.71 V instead of ranging from 2.30 V to 7.73 V. These results are obtained when using a maximum time step of 10 fs in SMASH. If the maximum time step is increased to 100 fs, the amplitude accuracy diminishes, yielding a voltage range of 2.34 V to 7.64 V. The benefit is the decrease of simulation time for a signal of 2 ns from 6.8 s to 1.6 s.
Note that many of the possible improvements discussed in the previous sections (like the use of central differences to calculate the velocity vector, employing two hidden layers in the ANN, etc.) where not implemented during the creation of this model. Still, the achieved accuracy is very good.
For further results obtained by this model (in particular, the phase noise plot) refer to [286].

8.6.2 *Differential Colpitts-VCO*

The results presented in this section belong to the differential 60 GHz Colpitts VCO taken as example throughout this chapter. The parameters of the employed neural networks correspond to the ones obtained by the training process documented in section 8.4.2. If not mentioned otherwise, $v_{\text{control}} = 0.5\,\text{V}$. This voltage has not been employed for the startups in training. The ADS results which the VHDL-AMS simulations are compared to are created exclusively for model verification. Thus, the simulation results in this section do not represent fitted curves, but rather show the excellent generalization properties of the model. To reduce the influence of the solver accuracy on the results, the maximum time step is chosen to be 50 fs for both VHDL-AMS and ADS.
Figure 8.15 compares oscillator startups generated by the VHDL-AMS model and ADS. The excellent agreement in steady state is demonstrated by the zoomed-in view in the same figure. The 180° phase difference between the two outputs is well maintained by the behavioral model. The minimum and maximum values are 0.147 V and 1.731 V (VHDL-AMS) versus 0.137 V and 1.745 V (ADS). The oscillation frequency is 61.16 GHz (VHDL-AMS) versus 61.15 GHz (ADS).
The transient envelopes as a whole correspond very well. The amplitude difference is about 60 mV around $t = 1.05\,\text{ns}$ due to the fact that the behavioral model is only of order two and thus cannot represent all the dynamics necessary to exactly simulate the startup process. However, the achieved accuracy is more than sufficient for a behavioral model. This is also confirmed by the transient simulations of a real-world VCO discussed in section 8.6.3.
Figure 8.16 gives a plot of the even and odd mode behavior of the oscillator. The swing of the odd mode oscillation is 1.612 V_{pp} (VHDL-AMS) versus 1.585 V_{pp} (ADS). A small discrepancy during the transient is observed here as well.

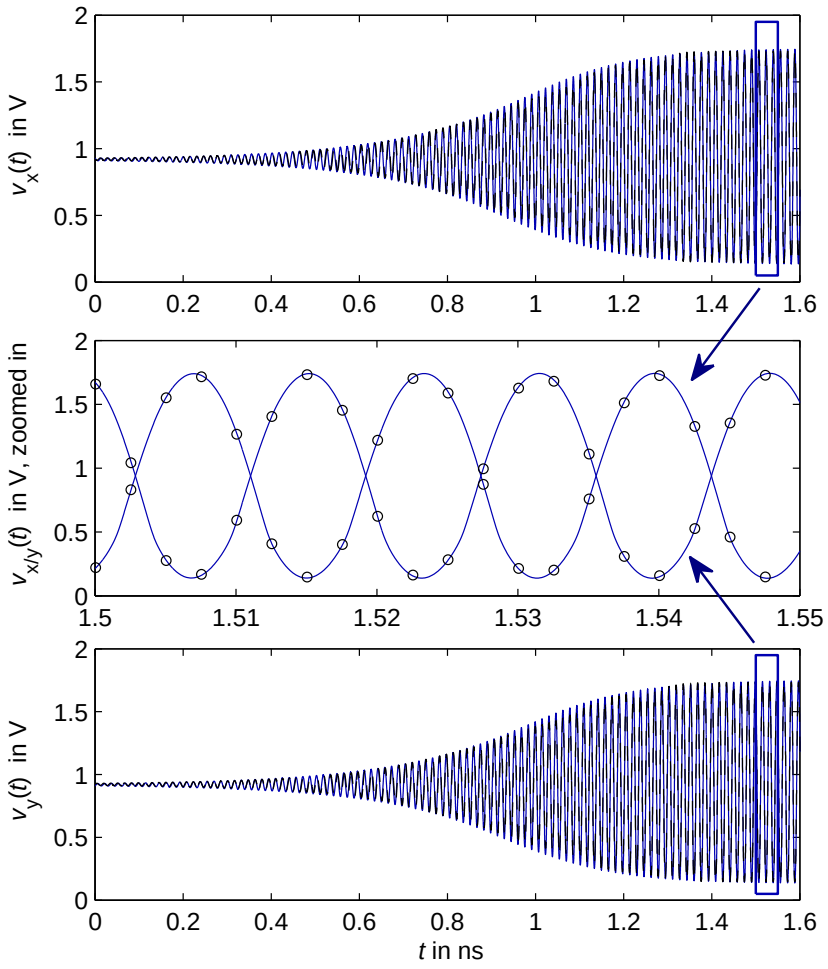


Figure 8.15: Output of the VHDL-AMS model (dotted black line or markers) versus ADS simulation results (solid blue line) for $v_{control} = 0.5\,V$

The even mode plots show the very close agreement of the bias voltage (919 mV VHDL-AMS versus 921 mV ADS) and the response in steady state, even though the model is not optimized in this regard. In the transient part of the even mode plot the agreement is slightly degraded, for the reason discussed above. However, considering the mV scale of the ordinate, this error has small impact on the overall simulation.
Figure 8.17 shows the results of a frequency sweep when continuously increasing $v_{control}$ from its minimum to its maximum value. The lowest frequency is 58.79 GHz (VHDL-AMS) versus 58.72 GHz (ADS), the highest frequency is 63.91 GHz (VHDL-AMS) versus 63.79 GHz (ADS). The slight phase difference between the VHDL-AMS curve and the ADS-curve apparent from the zoomed-in view is due to this slight difference in frequencies. Compared to the dispersion due to process variations an error of this magnitude is negligible.
Note that during the change of $v_{control}$ the two curves follow each other very closely. This reflects the fact that the behavioral model correctly represents the dynamics when changing $v_{control}$. The model can thus be used to simulate systems where these dynamics are important, as for example Phase Locked Loops (PLLs).
Figure 8.18 shows the phase noise plot created by the VHDL-AMS simulation in SMASH. The asymptotes can be placed by setting the

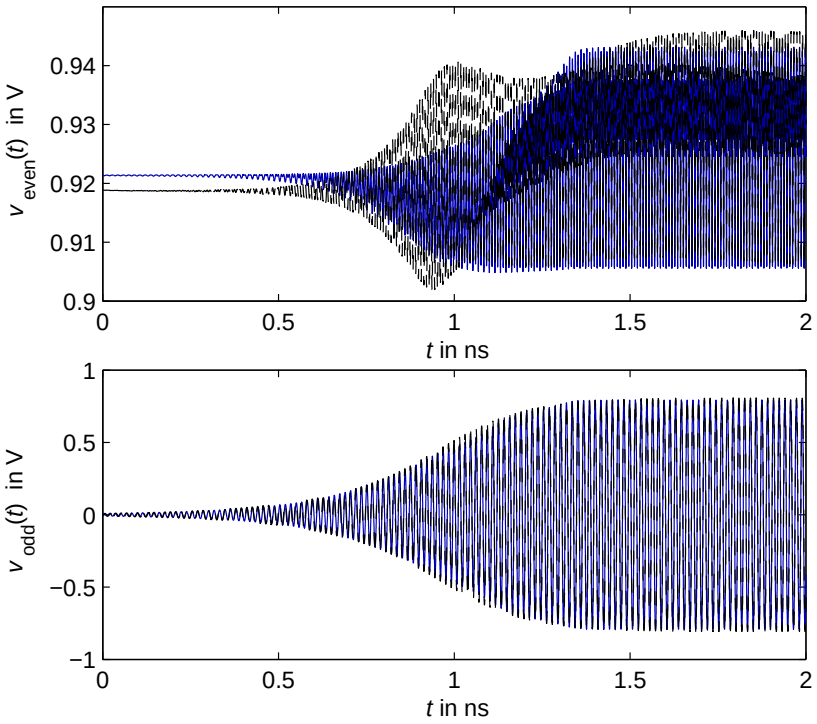


Figure 8.16: Output of the VHDL-AMS model (dotted black line) versus ADS simulation results (solid blue line) in even mode ($v_{even}(t) = (v_x(t) + v_y)/2(t)$) and odd mode ($v_{odd}(t) = (v_y(t) - v_x(t))/2$).

standard deviations σ_1 and $\sigma_{2x/y}$ in order to closely resemble the original phase noise plot. The greater density at higher frequencies, accompanied by stronger deviations from the asymptotes, are due to the fact that the simulation is done on a linear scale, but the plot is logarithmic. The slight decrease of the noise level in the flat region at highest frequencies is due to the fact that the additive Gaussian noise generated is not actually white, but its power density decreases when approaching the sampling frequency.

8.6.3 *Integrated 60 GHz VCO in 65 nm CMOS including Buffers*

In order to demonstrate the applicability of the proposed modeling technique to real oscillators fabricated in a sub-micron CMOS semiconductor process, it is applied to the 60 GHz VCO in 65 nm CMOS technology whose design is detailed in part I of this thesis (cf. to part I, section 4.3 for more details).
The simplified schematic (with neither bias circuitry nor extracted parasitics) is shown in figure 8.19. The Colpitts VCO uses differentially tuned accumulation-MOS varactors, which are represented during simulation by BSIM4 models. The BSIM4 model is also used for the transistors. The inductors are characterized by $2-\pi$ models extracted from electromagnetic field simulations. Source-follower buffers are employed to minimize loading of the oscillator core. All component values and device widths are annotated in the corresponding schematic in figure 8.19. The artificial current source $i_n(t)$ is added to the schematic after the design phase to generate the training data following the description given in section 8.4.3.

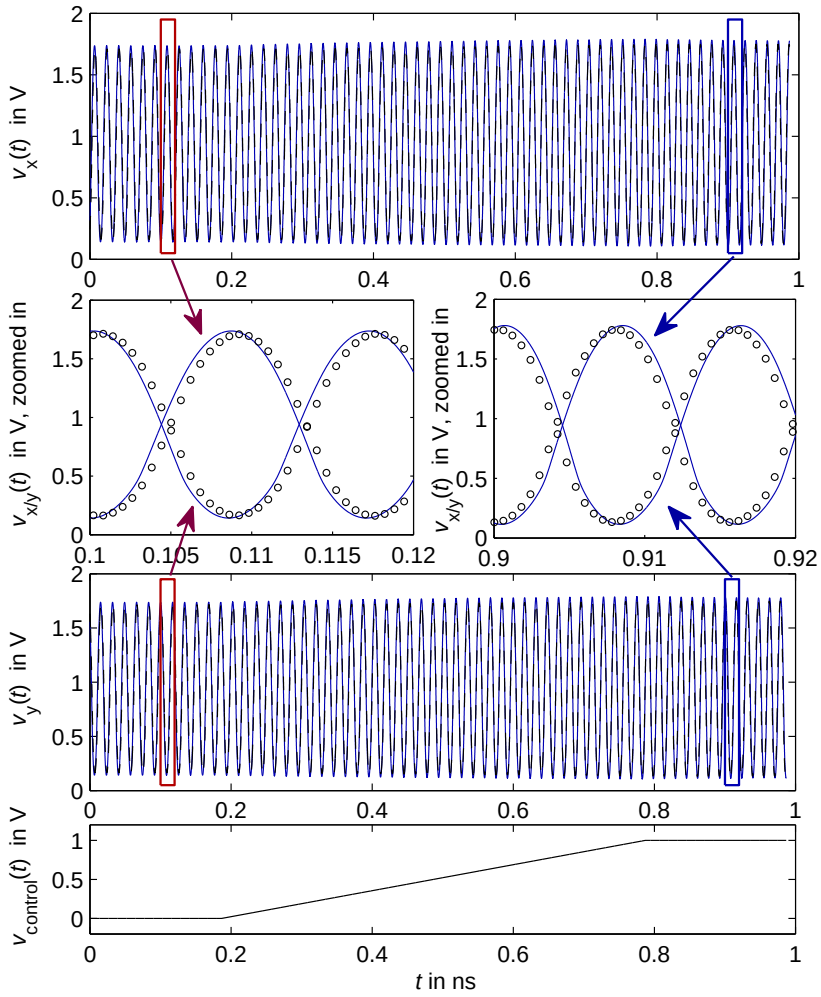


Figure 8.17: Output of the VHDL-AMS model (dotted black line or markers) versus ADS simulation results (solid blue line) for control voltage sweep

The circuit simulator SPECTRE, which is part of the Cadence framework, is used to calculate the circuit behavior based on the extracted schematic. To give an impression of the complexity of the oscillator, table 8.1 summarizes the circuit inventory established during SPECTRE simulation. This entire circuit is taken into account during model generation, and the evaluation of the behavioral VHDL-AMS model is done with respect to SPECTRE simulations of this circuit.

nodes	938
equations	2560
BSIM4	140
capacitor	2166
inductor	16
resistor	2318

Table 8.1: Circuit inventory of the SPECTRE model

As before, the state vector of the behavioral model comprises the difference of the output voltages, $v_y(t) - v_x(t)$, as first state variable and the

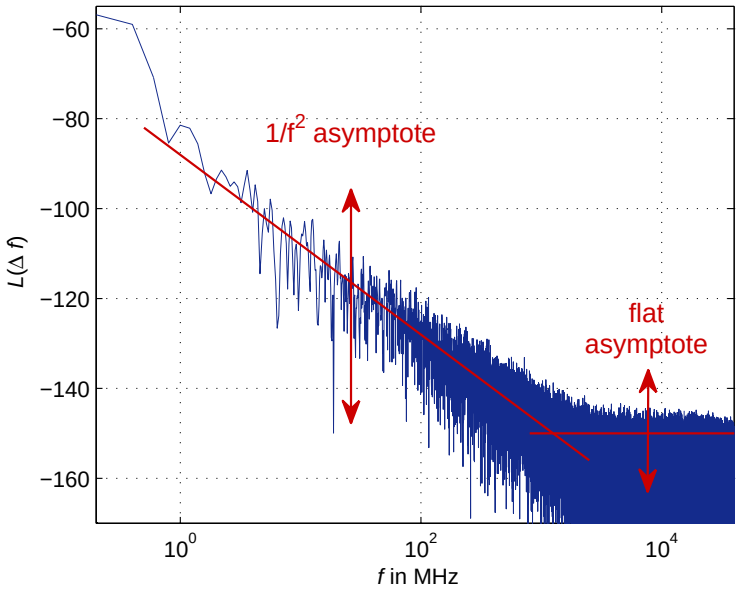


Figure 8.18: Phase noise characteristics shown by the VHDL-AMS model. The height of the asymptotes is set by σ_1 and σ_{2x}/σ_{2y}.

first derivative thereof as second state variable. Note that the output buffers are included inside the VHDL-AMS model, so $v_y(t) - v_x(t)$ does not correspond to a voltage observed across a circuit element.
The structure of the VHDL-AMS model is the one of figure 8.7. The ANN used to approximate $f()$ contains 18 neurons in the first and 13 neurons in the second hidden layer. The ANN used to represent $\psi()$ employs 3 neurons in a single hidden layer. The training employs startup waveforms with $v_{control}$ varying from $-0.7\,V$ to $0.7\,V$ in steps of $0.1\,V$ and yields an MSE of $2.30E-5$ for $f()$ and an MSE of $1.59E-4$

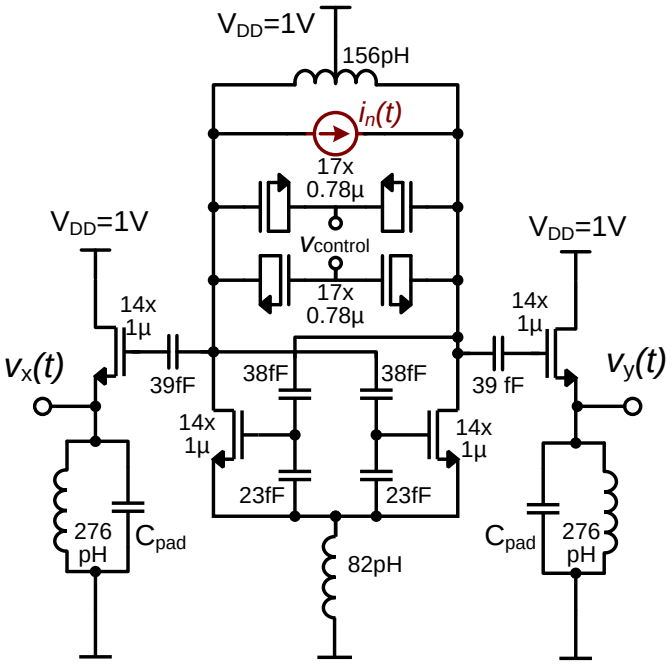


Figure 8.19: Schematic of the 65 nm CMOS 60 GHz VCO

for $\psi()$. ANNs with fewer neurons yield only little worse MSEs. The VHDL-AMS model based on these ANNs is used to do the performance evaluation in the following sections.

8.6.3.1 *Accuracy of the behavioral VHDL-AMS model*

The behavioral model's steady state accuracy is demonstrated by comparisons of both the trajectories and the tuning curves between the SPECTRE circuit model and the behavioral VHDL-AMS model.

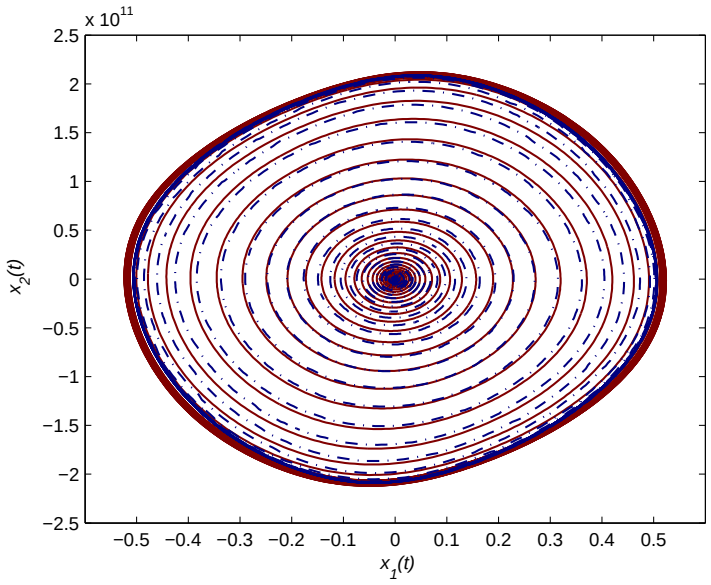


Figure 8.20: Trajectory obtained from SPECTRE-simulation (red, solid line) versus VHDL-AMS model (blue, dotted line)

Figure 8.20 plots the oscillation trajectories for $v_{\text{control}} = 0\text{V}$. They resemble each other very closely. The form of the limit cycle attained in steady state has the same shape for both of the models. This confirms that an enormous order reduction is possible even in the case of a real 60 GHz sub-micron CMOS VCO: the system order can be successfully reduced from more than two thousand to two. Differences between the two trajectories can be explained by the influence of noise and the solvers' accuracies, which are difficult to align between the two simulation environments.
Furthermore, the accuracy in steady state can be confirmed by the tuning curve of figure 8.21, where the control voltage is swept over the whole tuning range ($v_{\text{control}} = -0.7\,\text{V}$ to $+0.7\,\text{V}$). Excellent agreement is achieved, showing that the nonlinear curvature of the tuning curve is indeed also present in the behavioral model, even though the varactors are not explicitly modeled.
To assess the accuracy in the transient regime, figure 8.22 shows the startup for two different control voltages. Good agreement between circuit model and behavioral model can be observed in both cases. The fact that the amplitude differs by several mV between both models is explained by the different tolerances of the solver, despite using the same maximum time-step of 50 fs. Higher accuracy can be obtained by employing smaller time steps at the expense of longer computation time, as used for training data generation (cf. section 8.4.4).
The fact that startups for two different control voltages (and thus

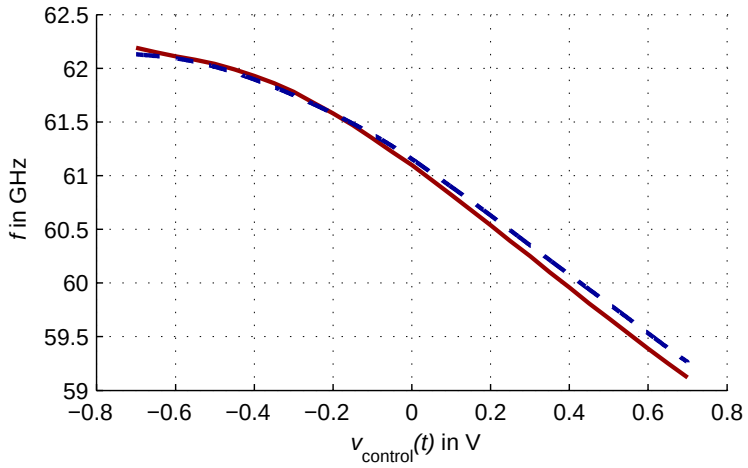


Figure 8.21: Tuning-curve of the oscillator, SPECTRE (solid line) versus VHDL-AMS (dashed line)

oscillation frequencies) show different transient envelopes (compare figure 8.22 (a) and (b)) is also correctly taken into account by the behavioral VHDL-AMS model.

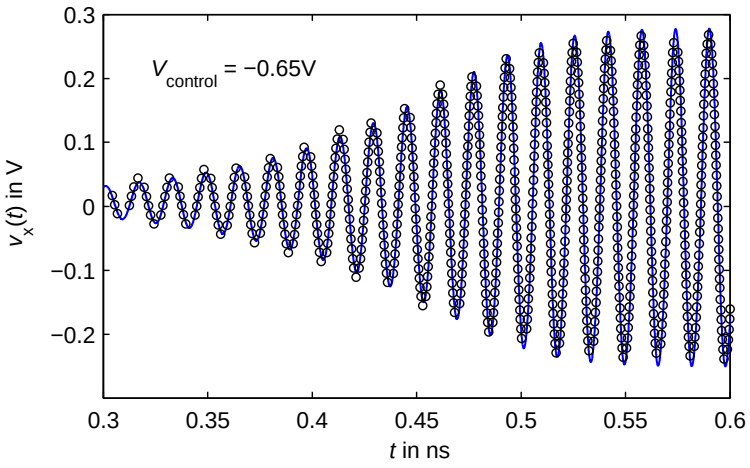
8.6.3.2 *Computation Time Comparison*

In order to assess the speed-up achieved by the behavioral model with respect to the circuit model, their simulation times are compared in table 8.2.

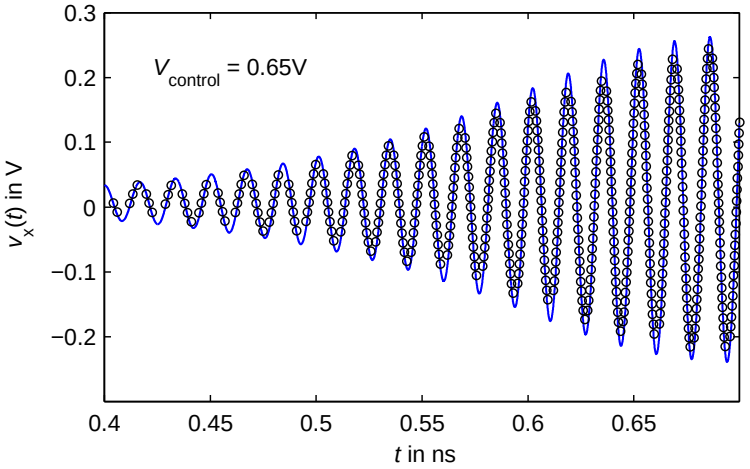
SPECTRE simulation, with transient noise	30 min 43.6 sec
SPECTRE simulation, without transient noise	23 min 43.7 sec
VHDL-AMS simulation	1 min 13.2 sec

Table 8.2: Simulation time for start-up and subsequent steady state that take together 10 ns of virtual time

The SPECTRE simulation is executed on a machine equipped with two 3.2 GHz Intel PENTIUM 4 processors and 3 GB RAM, using Cadence 5.10.41. The VHDL-AMS simulation is executed on an Intel Core 2 6700 2.66 GHz processor with 3 GB RAM, using SMASH 5.10. Both simulations are done single-threaded.
The simulation scenario consists of the start-up and subsequent steady state for $v_{control} = 0V$ which takes in total 10 ns. The maximum time step chosen is 50 fs, the relative accuracy is 1e-5, and the used solver is *Gear*.
In the case of the SPECTRE simulation, two different setups are evaluated: The default case is a transient simulation which does not take into account noise. This is the only one supported in older versions of SPECTRE. However, because the behavioral VHDL-AMS model does simulate transient noise, this kind of simulation is more appropriate for comparison. Thus its execution time is also given.
In both cases the comparison confirms the effect expected from the order reduction: A tremendous speed-up by a factor of up to 25 is achieved for the present simulation setup, while maintaining the accuracy shown in the previous section. This speed-up is less pronounced for circuits of lesser order, because the achievable order reduction is



(a) $v_{\text{control}} = -0.65\text{V}$



(b) $v_{\text{control}} = +0.65\text{V}$

Figure 8.22: Startup waveform at output x of theVCO. VHDL-AMS model (markers) versus SPECTRE-simulation (solid line).

smaller. On the other hand, an even higher speedup would be possible when optimizing the implementation of the reduced-order model. Altogether, the strong interest of replacing the circuit level model by the proposed behavioral VHDL-AMS model after the design phase is confirmed. The computation time necessary to create the training data and train the ANNs is compensated by much faster execution of the behavioral model.

9 CONCLUSION ON BEHAVIORAL MODELING

Part II of this thesis discussed the possibility of replacing highly complex device-level models that are employed in the design of RFICs by behavioral models for the purpose of system simulation.
Behavioral models can allow both the reduction of simulation time and the complete simulation of large systems consisting of analog, digital and mixed-signal building blocks. The combined simulation of heterogeneous building blocks is possible, because the behavioral models can be implemented using VHDL-AMS, an analog and mixed-signal extension to VHDL: as VHDL is usually employed during the design of digital circuits, their behavioral models are available after design phase. They can thus be combined with the behavioral VHDL-AMS models to simulate, for example, the behavior of a complete radio interface.
The contribution of this thesis to the behavioral modeling of mm-wave circuits is detailed in chapter 8: a methodology to create behavioral models of microwave oscillators that can be implemented in VHDL-AMS was developed. The model is based on data obtained from a transistor level simulation that is used during design phase (cf. part I). This low level simulation employs models of high order and complexity. The novel modeling methodology uses this data to parametrize a model structure of only second order. However, this reduced-order model is capable of approximating a high degree on nonlinearity by artificial neural networks. The proposed technique is applicable to state-of-the-art VCOs (like the one designed in part I of the thesis), whose behavior concerning transient, steady state and phase noise is faithfully reproduced by the presented model. Comparison of the outputs of the proposed model and circuit level simulations show excellent agreement in all operating regimes, while the behavioral model achieves a reduction in computation time of up to 96%.
The field of application of such an accurate behavioral model are simulations where the complexity of an extracted circuit model is too high, yet an accuracy close to the one of such a transistor level model is desired. Examples include simulations of PLLs and SoCs or even SiPs, where the influence of the oscillator's peculiarities is decisive to assess the system performance. While still simpler models that avoid actually solving differential equations by just plotting the (pre-calculated) solution are faster, they suffer from a reduction in both accuracy and flexibility.
The work on the presented oscillator modeling technique is completed, whereas models for the other analog and mixed-signal building blocks of the radio interface introduced in part I need to be developed (a first step in this direction is the implementation of a model for RF MEMS shunt switches and phase shifters in VHDL-AMS presented in appendix C). Furthermore, the undesired interaction between these blocks both due to electromagnetic coupling and substrate currents needs to be analyzed and taken into account during system simulation by adjusting the behavioral models accordingly.

GENERAL CONCLUSION

This general conclusion briefly summarizes the most important contributions of this thesis. More detailed conclusions, and perspectives on future work, can be found in the conclusion on transceiver front-end design (chapter 6) and in the conclusion on behavioral modeling (chapter 9). The scientific articles disseminating the work of this thesis are listed on the following page.
The scientific contributions of this thesis can be arranged according to their hierarchical level:

- **On the device level**, novel guidelines to accurately simulate and measure passive devices have been developed. They facilitate the use of spiral inductors in 60 GHz RFICs, improving circuit performance with respect to designs based on distributed elements.
- **On the component level**, several 60 GHz building blocks with record performance, especially with respect to circuit size and power consumption, have been realized in 65 nm CMOS. The design success is both based on active and passive devices optimized for the use at 60 GHz and specific mm-wave design and layout techniques. The realized building blocks include:
  1. A high-gain two-stage cascode LNA optimized with respect to power consumption and circuit size.
  2. A differential 60 GHz Colpitts VCO with record efficiency and very high output power.
  3. A broadband high-gain down-conversion mixer with minimum LO power requirements and very small circuit size.
  4. The first 60 GHz double balanced dual-gate up-conversion mixer in CMOS.
- **On the front-end level**, a very detailed literature review concerning 60 GHz transceiver architectures has been conducted, leading to the adoption of a direct conversion topology due to its potential to realize the best compromise between low-power consumption and high versatility. Based on this choice and the afore-mentioned building blocks, the in-phase branch of a direct conversion receiver, consisting of Low Noise Amplifier (LNA), VCO, down-mixer and buffers, has been successfully realized. The measurements show a record performance with respect to power consumption and excellent conversion gain from 60 GHz to baseband. At the same time, the occupied die area is the smallest found in literature for a comparable 60 GHz receiver front-end.
- **On the system level**, a novel technique to create behavioral models for mm-wave oscillators has been proposed. It uses a second order differential equation in state space representation to accurately describe the oscillator's dynamics. Its nonlinear characteristic is approximated by artificial neural networks. The resulting models achieve a drastic reduction of simulation time for complex circuits, while at the same time maintaining circuit-level accuracy with respect to start-up, steady state and phase noise of the oscillator.

PUBLICATIONS

The work outlined in this thesis has been published in the following journals and conference proceedings:

JOURNAL PAPERS

- Kraemer, M.; Dragomirescu, D. and Plana, R. (2010), "A High Efficiency Differential 60 GHz VCO in a 65 nm CMOS Technology for WSN Applications", *IEEE Microwave and Wireless Components Letters*, accepted for publication
- Kraemer, M.; Dragomirescu, D. and Plana, R. (2009), "A Nonlinear Order-Reducing Behavioral Modeling Approach for Microwave Oscillators", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 57, No. 4, part II, p. 991-1006, April 2009

INTERNATIONAL CONFERENCE PAPERS

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APPENDIX

A BRIEF OVERWIEV ON VHDL-AMS

Being backward compatible to VHDL, VHDL-AMS supports both a structural hardware description using hierarchical netlists and a behavioral description. In the case of digital circuits the latter one is event-driven and uses *concurrent statements* to describe the circuit's behavior. It employs a discrete model of time.
To allow the modeling of analog circuits, VHDL-AMS adds *simultaneous statements* as a second means of behavioral description: they are used to implement ordinary differential and algebraic equations, whose continuous time solutions are calculated by a numerical solver. In the following, analog behavioral modeling based on these simultaneous statements is briefly introduced.

QUANTITIES The unknowns in the algebraic and differential equations are analytic functions of time: they are represented by a *quantity*, which is a new class of floating point object in VHDL-AMS. An example of the explicit declaration of four exemplary real quantities U, U1, U2 and I is given by:

```
quantity U,U1,U2,I : REAL;
```

In addition to that, quantities are also implicitly declared by adding keywords like `'dot` to an existing quantity (when adding `'dot` to a quantity, a new quantity is created that contains its first time derivative).

SIMULTANEOUS STATEMENTS To formulate *simultaneous statements*, the == operator is employed as separation between left hand side and right hand side of the equation:

```
U1 == R*I;
I == C*U2'dot;
U == U1+U2 tolerance "HIGH";
```

Each of the algebraic (first line) and differential (second line, due to the `'dot` keyword that creates a derivative) equations formulated by simultaneous statements constitutes one line of the system of equations solved by the numerical solver. The solver establishes the equality of left hand side and right hand side within a given tolerance that may be explicitly indicated after each simultaneous statement as shown in the code example.
Even though partial differential equations would be convenient to model wave propagation on transmission lines and in free space, as well as electromagnetic coupling, they are not yet included in the VHDL-AMS standard. This limits the simultaneous statements to the description of circuits consisting of lumped elements. However, P. Nikitin *et al.* propose their implementation by adding the missing spacial dimension using a distributed equivalent circuit. They also suggest an extension of VHDL-AMS in this regard [308].

CONSERVATIVE SYSTEMS VHDL-AMS also provides a way to easily implement conservative systems (e.g. an electrical circuit obeying Kirchhoff's law). Conservative behavior is introduced by defining certain

quantities (e.g. U and I) as so called *branch quantities*. These definitions makes use of the keywords `through` and `across` as illustrated in the listing below:

```
terminal t1,t2: electrical;
quantity U across I through t1 to t2;
```

First, two *terminals* t1 and t2 need to be declared by indicating their nature (here electrical). Then, one branch quantity representing the difference in potential (e.g. the voltage U) *across* these terminals, and another branch quantity representing the flow (e.g. the current I) *through* these terminals can be assigned.

CONVERSION STATEMENTS In order to connect a circuit part that uses continuous time quantities of VHDL-AMS to a classical, digital VHDL circuit, conversion statements exist. For analog-to-digital conversion, the `'above( )` directive creates an event if a given threshold is exceeded. The following code assigns the state '1' to the digital signal s if the quantity U crosses 1, otherwise s remains in state '0':

```
s <= '1' when U'above(1.0) else '0';
```

For digital to analog conversion, two possibilities exist. Either, the digital *signal* is directly assigned to a *quantity*. In this case, the fact that a discontinuity occurs if the signal changes states has to be indicated using the `break` directive:

```
U == s;
break on s;
```

Alternatively, the `'ramp` directive can be used. It allows the specification of a transient time for the rising and falling edges to introduce a more physical, continuous transition, for instance by:

```
U == s'ramp(1.0e-6,1.0e-6)
```

The above examples only briefly introduced some characteristic properties of VHDL-AMS. Further details can be found in [283, 284]. Appendix B provides some code examples to illustrate how the novel models proposed in this thesis are implemented in VHDL-AMS.

B

STRUCTURE OF THE OSCILLATOR MODEL'S VHDL-AMS CODE

The core of the VCO model is a VHDL-AMS entity with four ports, p1 to p4. The first port is connected to a grounded noise current source, implemented as described in [306], in order to provide i_n. Port two and three represent the oscillator's outputs v_x and v_y with respect to ground. Two series noise voltage sources [306] that generate the additive noise for the flat region of phase noise are series-connected externally to these ports. The oscillator's output signal including phase noise is taken at the open pins of these noise sources. The forth port is connected to the $v_{control}$ input.
In the architecture definition of the Voltage Controlled Oscillator (VCO) entity, the currents through and voltages across the terminals are defined as quantities according to:

```
quantity In through p1 to ELECTRICAL_REF;
quantity voutx across p2 to ELECTRICAL_REF;
quantity vouty across p3 to ELECTRICAL_REF;
quantity vcontrol across p4 to ELECTRICAL_REF;
```

Other quantities are associated to the normalized inputs, the state variables and their derivatives, the nodes of the neural networks, and other auxiliary variables:

```
quantity In_norm :      real tolerance "NORMALIZED";
quantity x1      :      real tolerance "NORMALIZED";
quantity x2      :      real tolerance "NORMALIZED";
quantity dx2_dt  :      real tolerance "NORMALIZED";
quantity Vcontrol_norm :        real
                         tolerance "NORMALIZED";
                      ...
quantity nodeh1  :      real_vector(1 to 15);
quantity nodeh2  :      real_vector(1 to 10);
```

The TOLERANCE keyword specifies the tolerance used by the solver to evaluate different groups of quantities.
After defining the quantities, constants are defined that contain the parameters of the neural networks, such as weights, biases and normalization constants. To load the actual values from the text files exported by Matlab, functions created for this purpose are called in the initialization process.
The body of the entity's architecture between the begin and end keyword consists of the definition of the state space equations according to (8.13) and (8.14), the definition of the equations describing the two neural networks according to (8.16), and the associated normalization and denormalization.
To implement the derivatives that appear in the state equations, the 'dot- statement is used:

```
x2 == x1'dot * norm_const1;
dx2_dt == x2'dot * norm_const2;
```

The more complex equations describing the neural network make use of the GENERATE statement to automate the formulation of lengthy equations:

```
BuildInputLayer: FOR i IN 1 TO 15 GENERATE
nodeh1(i) == tanh(      w1(i*4+1) * x1 +
                  w1(i*4+2) * x2 +
                  w1(i*4+3) * In_norm +
                  w1(i*4+4) * Vcontrol_norm +
                  b1(i) );
                  END GENERATE;
-- build second hidden layer here:
                   ...
-- output layer:
dx2_dt == tanh( w2(1) * nodeh2(1) +
                  w2(2) * nodeh2(2) +
                   ...
                  w2(10) * nodeh2(10) +
                  b2(1) );
```

Note that in the code fragment above, `w1(), w2(), b1()` and `b2( )` are vectors containing the weights and biases of the neural network. Due to the lack of matrix operators in the VHDL-AMS definition [282] these equations cannot be written more efficiently.

C

VHDL-AMS MODEL OF RF MEMS SWITCHES AND PHASE SHIFTERS

In the following, a way to model the behavior of a Radio Frequency (RF) Micro Electro Mechanical System (MEMS) capacitive shunt switch using VHDL-AMS is detailed. The presented implementation is based on an equivalent circuit using both lumped and distributed elements. The actuation of the RF MEMS switch is done according to a digital control signal. By employing a scaling factor, the model can easily represent the behavior of RF MEMS switches having different geometries for center frequencies from 20 GHz to 94 GHz, and beyond.
The excellent agreement between measurements and VHDL-AMS simulations is demonstrated by the example of a 60 GHz RF MEMS switch. The VHDL-AMS model of a RF MEMS based phase shifter is also presented. It is based on the switch model and a model of a transmission line. Excellent agreement in phase shift between VHDL-AMS and ADS simulations is achieved.
The following sections describe RF MEMS capacitive shunt switches and the implementation of their equivalent circuit model in VHDL-AMS. Its use in order to create the model of a more complex phase shifter circuit is detailed in section C.4.

C.1 RF MEMS CAPACITIVE SWITCHES

A die photo of a 60 GHz RF MEMS capacitive shunt switch is shown in figure C.1. It consists of a metal bridge suspended over a Coplanar Waveguide (CPW), where the size of the bridge defines its capacitance and thus influences the frequency of operation. An actuation voltage of around 30 V causes the pull-in, i.e. the short-circuiting of the signal path to ground by substantially decreasing the capacitance from its up-state value C_{up} to its down-state value C_{down}. For an in-detail explication of this RF MEMS switch refer to [309].

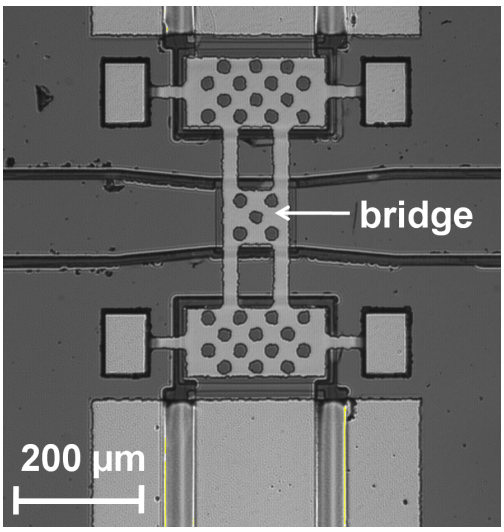


Figure C.1: Die photo of a 60 GHz RF MEMS switch

The equivalent circuit model of the RF MEMS capacitive shunt switch proposed by J.B. Muldavin *et al.* [310] is given in figure C.2. The only element that changes from up-state to down-state according to the switching signal s_d is the capacitance C.

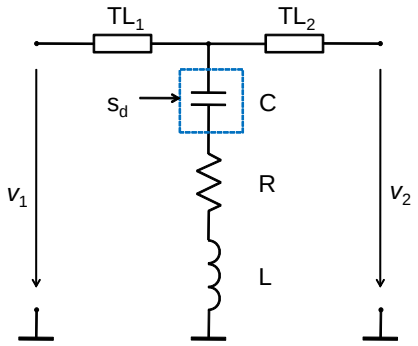


Figure C.2: RF MEMS switch equivalent circuit model

In [309], an approach is introduced which allows to scale the dimensions of a reference RF MEMS design done at 20 GHz in order to obtain a switch working at a frequency that can be specified between 20 and 94 GHz. Based on the scaling factor K_x used to design a particular switch, the parameters of its equivalent circuit model are determined according to

$$C_{up/down,x} = C_{up/down,1}/K_x^2, \tag{C.1}$$

$$L_x = L_1/K_x, \tag{C.2}$$

and

$$l_x = l_1/K_x, \tag{C.3}$$

where l_x is the length of the transmission lines, L_x is the inductance value, and $C_{up/down,x}$ are the capacitance values for the new device. The resistance R is assumed to be constant over frequency. The parameters of the reference device, indicated by 1, are given in [309] together with the scaling factors K_x for various frequencies.

C.2 THE VHDL-AMS MODEL

The VHDL-AMS model contains two principal parts: The first part is the resonating core, which uses a VHDL-AMS process to change the capacitance value according to the switching signal s_d. In order to simulate the switching time correctly, the two discrete capacitance values are mapped to a VHDL-AMS quantity using the keyword `'ramp`. This keyword allows changing the capacitance value gradually from C_{down} to C_{up} during the specified time interval. The equations describing the currents and voltages of the model core are implemented using simultaneous statements (indicated by ==). The essential part of the associated VHDL-AMS code is:

```
switchit : process ( sd ) is
begin
```

```
        if (sd = '0') then
        cap_discrete <= capup;
        elsif (sd = '1') then
        cap_discrete <= capdown;
        end if;
end process switchit;
cap == cap_discrete 'ramp(uptodown_time, downtoup_time);
i==cap*v1 'dot;
v2 == R * i;
v3 == L * i 'dot;
v == v1+v2+v3;
end architecture default;
```

The second part is the Transmission Line (TL) model. It makes use of the solution of the TL equations by assuming that there is an incident and a reflected wave propagating on the line. The signal $V_{to}(t)$ is the incident voltage waveform at the beginning of the TL, while $V_{back}(t)$ is the reflected voltage waveform at the end of the TL. To obtain the voltage waveforms at any other location, the signals $V_{to}(t)$ and $V_{back}(t)$ are delayed, according to wave velocity and position on the line, using the `'delayed` statement of VHDL-AMS. The associated current waveforms are calculated by dividing the voltage waveforms by the line's characteristic impedance Z_0. To take into account loss, an exponentially applied attenuation factor α is specified.
Eventually, input and output voltages and currents are the superposition of these incident and reflected waves after experiencing the associated delay and attenuation. The essential part of the VHDL-AMS code implementing the TL model is:

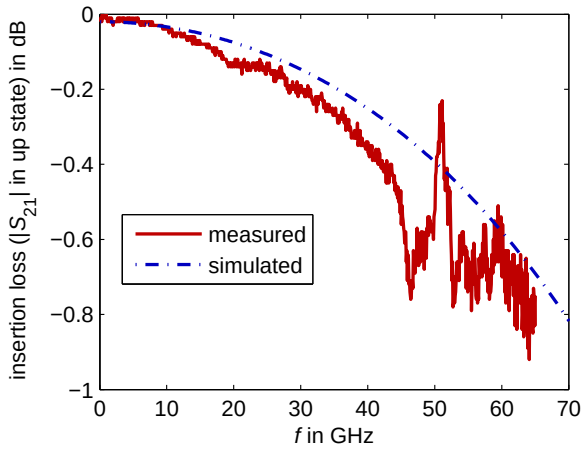
```
architecture default of Line is
quantity Vto: VOLTAGE;
quantity Vback: VOLTAGE;
quantity Vin across Iin through p1 to p2;
quantity Vout across Iout through p3 to p4;
begin
Vin==Vto+Vback 'delayed(l/c*sqrt(eps))
        *exp(-alpha*l);
Iin==Vto/Z0-Vback 'delayed(l/c*sqrt(eps))
        *exp(-alpha*l)/Z0;
Vout==Vto 'delayed(l/c*sqrt(eps))
        *exp(-alpha*l)+Vback;
Iout==-Vto 'delayed(l/c*sqrt(eps))
        *exp(-alpha*l)/Z0+Vback/Z0;
end architecture default;
```

Note that though physical loss mechanisms (which are mainly constituted by skin effect and dielectric loss) depend on frequency, the presented model uses a constant attenuation α which is exact only for one frequency. The implementation of an explicit frequency dependence of α is not possible, because the model has to work in time domain to ansure compatibility with digital VHDL models.
In order to more correctly take into account loss, a transmission line model similar to the one implemented in [311] can be used. The partial differential equations describing the TL are represented by a ladder network with sufficient elements to account for the distributed nature of the TL. While being able to model loss mechanisms that are frequency dependent, the parameterization of this kind of model is more difficult.

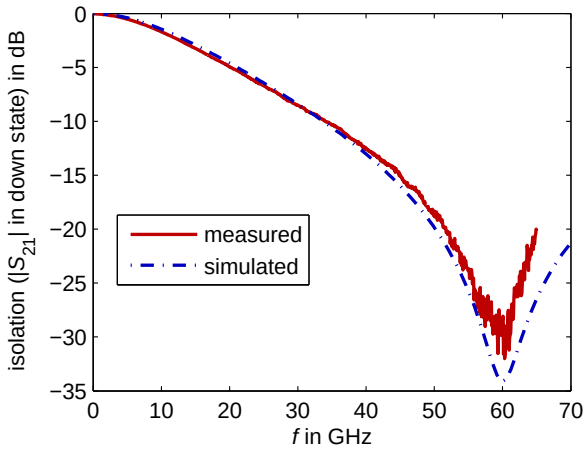
Furthermore, the computation time increases considerably with respect to the suggested simple model, thus jeopardizing the effort to reduce complexity and computation time.

C.3 RF MEMS MODEL RESULTS

In figure C.3a the insertion loss of a 60 GHz RF MEMS switch in up-state is plotted. The general agreement between measurements and VHDL-AMS simulation is good. The variations of the insertion loss can be explained by the difficulty of measuring low loss transmission factors at these frequencies. In figure C.3b the isolation is shown. Both resonance frequency and the associated strong attenuation of the signal are faithfully reproduced by the model. These results confirm the validity of the TL model described in section C.2 for RF MEMS switch modeling.



(a) insertion loss (in up-state)



(b) isolation (in down-state)

Figure C.3: Transmission measurement versus VHDL-AMS simulation of the 60 GHz RF MEMS shunt switch in up- and down-state

C.4 VHDL-AMS MODEL OF PHASE SHIFTERS

One application of RF MEMS switches in a heterogeneous communication system as the one described in part I of this thesis are phase

shifters. They are used to change the beam direction of antenna arrays. The VHDL-AMS model developed in section C.2 is employed in the following to simulate the 60 GHz one bit single pole double throw switched line phase shifter presented in [312]. Figure C.4 shows the schematic of this circuit. The outermost switches M1, M4, M5 and M8 are blocked in up-state and serve as capacitors for matching purposes. The switching signal 'S' is used to commute between a long TL and a short TL, with the goal of attaining 45° phase difference between the two paths. The TLs between the RF MEMS are used as interconnect and for matching purposes (refer to [312] for circuit details).

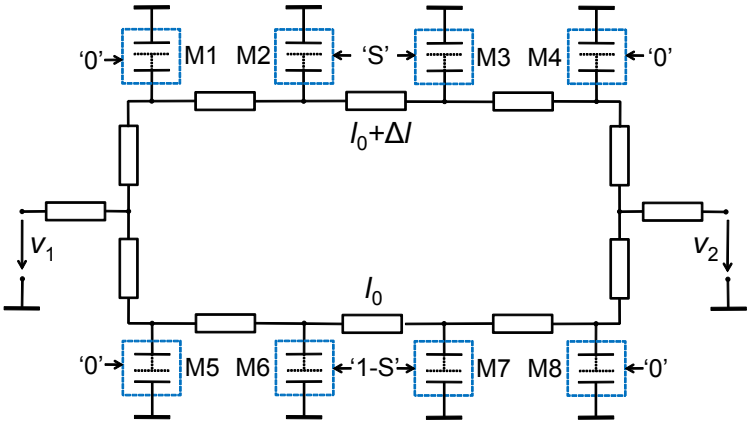
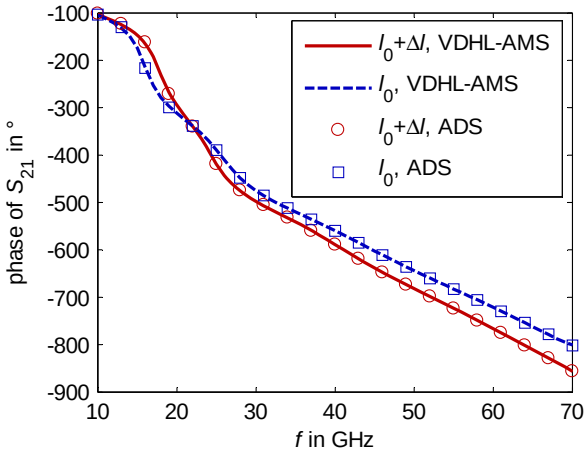


Figure C.4: Schematic of switched line phase shifter composed of RF MEMS capacitive switches and TLs

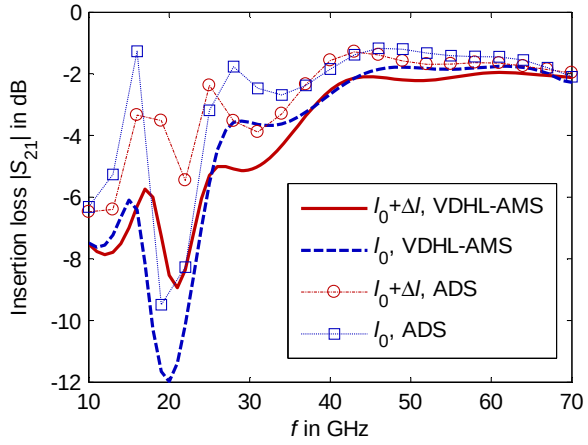
In order to model the phase shifter, its schematic is implemented in VHDL-AMS by connecting the adequately parametrized TL and RF MEMS switch models according to Fig. C.4. No additional elements are required. The resulting netlist constitutes the phase shifters' VHDL-AMS model.
Figure C.5a and figure C.5b compare the results of the VHDL-AMS model to results obtained from ADS simulations for the two states of the phase shifter. Concerning insertion phase (figure C.5a), excellent agreement was achieved between both models. The relative phase shift at 60 GHz is 44.93° (VHDL-AMS) versus 44.96° (ADS).
Concerning insertion loss (figure C.5b), the VHDL-AMS model's accuracy is very good in a large band around 60 GHz, but decreases towards lower frequencies. This has two reasons: First, as mentioned in section C.2, the TL models are only accurate at one frequency (depending on the attenuation coefficient α, here given at 60 GHz), while for lower frequencies loss is overestimated. Second, the VHDL-AMS model uses exactly the characteristic impedance Z_0 specified, while in ADS the simulated value slightly differs from the specified one.

C.5 CONCLUSION

A simple and yet accurate RF MEMS shunt switch VHDL-AMS model, based on an equivalent circuit has been developed. Its performance was confirmed with respect to measurements.
The application of the model to simulate a 60 GHz switched line phase shifter showed excellent agreement in phase shift at all frequencies,



(a) Insertion phase



(b) Insertion loss

Figure C.5: Magnitude and phase of the transmission coefficient in both states of the phase shifter, ADS simulation versus VHDL-AMS simulation

while its insertion loss is accurately modeled in the band around the operating frequency. The presented VHDL-AMS model has been published in [289, 292].