



ELECTRICAL SIMULATION METHODOLOGY DEDICATED TO EMC DIGITAL CIRCUITS EMISSIONS ANALYSIS ON PCB

J.M. Dienot, Yves Demarcq

► To cite this version:

J.M. Dienot, Yves Demarcq. ELECTRICAL SIMULATION METHODOLOGY DEDICATED TO EMC DIGITAL CIRCUITS EMISSIONS ANALYSIS ON PCB. 3rd International Workshop on Electromagnetic Compatibility of Integrated Circuits, Nov 2002, Toulouse, France. pp. 61-64. hal-00517791

HAL Id: hal-00517791

<https://hal.science/hal-00517791>

Submitted on 15 Sep 2010

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

ELECTRICAL SIMULATION METHODOLOGY DEDICATED TO EMC DIGITAL CIRCUITS EMISSIONS ANALYSIS ON PCB

Jean-Marc DIENOT, Yves DEMARCQ

Groupe d'Etudes en Compatibilité Electromagnétique de Tarbes

GECET - IUT de Tarbes

1 rue Lautréamont 65016 Tarbes cedex

jm.dienot@iut-tarbes.fr

1. Presentation of the study

Electronic CAO tools are actually efficient and helpful for circuit designers separately in many domains : RF, low-signal circuits, electromagnetic, power circuits... Nevertheless, they have to take in account the reconciliation in the future of complex electronic commands boards associated to power energy converters system integrated on closer structures, and the upsurge of electric/electromagnetic couplings in a large frequency band . In this context, we present a global modelling methodology for EMC considerations on Electronic Printed Circuit Board (PCB) and some applications for oriented EMC simulations. In a first time, we optimise an electrical models library dedicated to the simulations of EMC emissions of digital integrated component, including all the passives and actives elements used for EMC measurement test benches developed. In a second time, we propose global studies with the aid of time-domain simulator(Saber, MawellSpice) to realise a virtual experiment of considered phenomena. Results of measured and simulated EMC signals on test PCB with single digital component are presented to analyse and conclude about different contributions of the electrical elements of the board with their electrical environment for EMC comportment and characteristics.

2. Characterisations and associated electrical models for digital component emissions.

EMC emissions present around logical components on PCB are : DC supply coupling, input output coupling, direct radiated emission[1]. With the realisation of single layer PCB board including elementary digital components (buffers/inverters), we have developed the following characterisations for our purpose :

- Conducted measurements on the access of the component(tracks, connectors) by the way of voltages and current probes : transient shape of the signals, which can be translated in frequency domain by FFT.
- Close radiated measurements, H or E type, made over the most radiating elements of the board : supply and ground tracks, input/output tracks. These measurements are essentially issued from the fast transitions of current during each commutation. They are performed either in time domain, or frequency domain (Spectrum analyser).

In a similar way, we have implanted electrical modelling of components of the test benches developed[2]. A range of versatile equivalent electrical models for each part of test boards and methods of parameter extraction are proposed :

- Electrical model of the gates of the logical function for the active component, Spice format (Physical/empirical/external). Values of the parameters models are fitted from initials values provided by the component designers and by additional I-V static and dynamical characterisations.[2]
- Electrical models of passives elements of the board : package, tracks, connectors, capacitor, supply. The topologies of these models are from RLC cells type. Parameter values are issued from designers or are calculated with analytical formulas for conductors (TLT). Electromagnetic numerical calculus using PEEC concept are also used, with the aid of EM code, for particular configurations [3].
- Electrical models of measurement elements : capacitive and inductive coupling models of conducted and field probes are issued from parametric electromagnetic calculations taking in account the different insertion positions around the test boards.

Complete models corresponding to the test boards have been validated by measurements-simulations adjustments in conduction and close radiation. With the respect of electrical and functional comportment of the logical signals, they seem to be reliable to reproduce EMC signals in time-domain and frequency domain until 500 MHz, with optimal calculations time under SPICE simulator as Saber and MaxwellSpice[4].

3. EMC simulations analyses for PCB parameters studies.

We use tools previously described to analyse the different roles of the elements of the circuits for electromagnetic emissions on and close the PCB [5]. We lead a simulation methodology testing sensibility of various values of the parameters of the models, to analyse their effect on the simulation of EMC signals characteristics. The aim is to refine each model, active and passive, so to have object oriented electrical models which can take in account different dispersion of functional conditions of the real test bench :

- Functional parameters dispersion: Supply amplitude, clock amplitude, clock frequency.
 - the variation of the clock amplitude are inefficient in the range of commutation of the component

- the variation of the supply amplitude result in variations of the amplitude of conducted emissions, but not on the resonant frequency.
- Close radiated type H measurement and simulation show good concordances, and linear variation with the variation of the distance probe.
- Clock frequency has an effect on spectrum amplitude of close radiated field.
- **Board components dispersion** : gate output load, capacitance, supply tracks length.
 - the variation of the capacitive load, simulated and measured, show principally a variation of the conducted emissions amplitude, and a lesser variation of the resonant frequency.
 - the variation of the tracks length can be simulated in a first way by changing the RLC cells values and their distribution [6]. Simulation show expected results, as principally a variation of the resonant frequency of the EMC signals.

4. Global simulation for EMC analysis on PCB.

The previously conclusions on the validity boundaries of the use of the EMC models of the components of PCB are the first step for introducing a methodology of computational analyses of EMC perturbations, that we called Virtual Experiment for the EMC. For this approach, complementary studies oriented for the EMC emissions previsions are presented :

- For the same logical function of the gate studied, different components issued from various commercial designers have been tested in measurement and simulation. The variations of EMC signals characteristics are principally issued from the different fabrication technologies, which change the electrical consumption and the transients limits of the components. These variations have been simulated by adjusting internal parameters of the gate Spice model (transconductance Kp, threshold voltage) for each component tested(Fig 1)

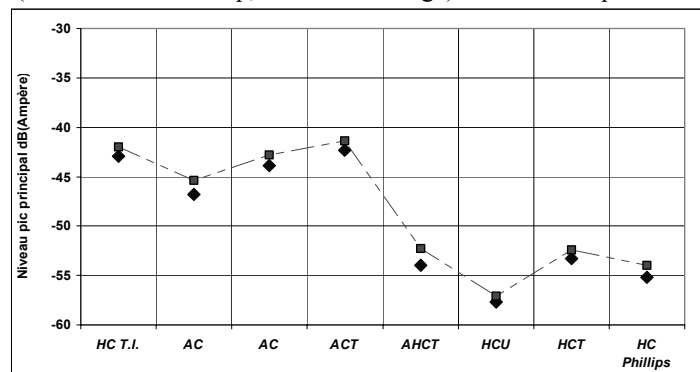


Figure 1 : Comparison of EMC conducted levels of technologies family measured and simulated.

- Similar comparisons with CMS packages of the same logical circuit have been realised. With an adjustment of internal model of the active part, of the model of packaging and of the length of the tracks for the connections on the component, EMC signal characteristics are in concordance with the measured ones. It shows lower peak levels for EMC spectrum but a different frequency repartition with previous studies .
- Programmable Array Logic (PAL) technology has been introduced in our EMC simulation approach. The logical function similar to HC04 family has been implanted in 22V10 PAL Package. Characterisation of close field near the ground track is compared on a similar PCB than HC test circuit(Fig. 2). It indicates a shift in the resonant frequency of the PCB, and an increase of 5-6 dB of the peaks levels.

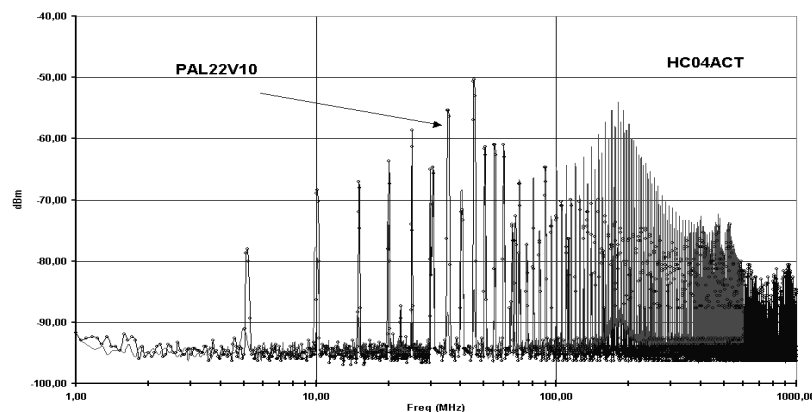


Figure 2 : EMC spectrum responses of PAL 22V10 and HC04 (measures)

EMC simulation of the response of this circuit has been realised by using an empirical functional model (macromodel) for the active part and slight changing of passives connections introduced by the package implanted on the test PCB. Simulated spectrum is representative of the EMC characteristics for this component (Fig. 3)

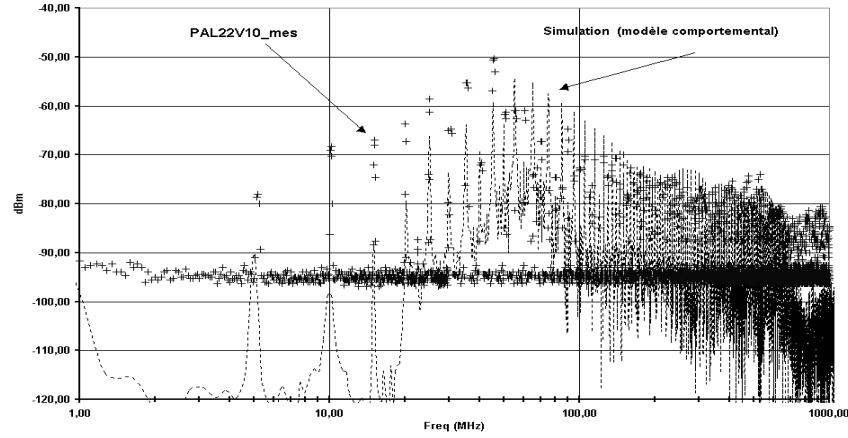


Figure 3 : EMC spectrum responses of PAL 22V10 measured and simulated

- d) The single gate study is extended at the others gates inside the package of the digital circuit (HCU04, buffers/inverters) to simulate EMC characteristics on the complete PCB. The reliability of the electric schematic is tested by adding progressively initial gate models to simulate the EMC signals with increasing component commutation and additional connexions between the gates.

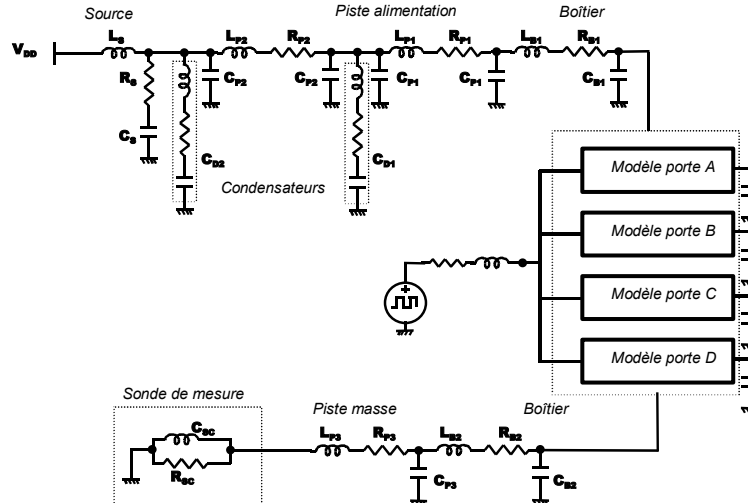


Figure 4 : Complete electrical schematic for the conducted emission simulation on the ground track of component HCU04 on PCB.(parallel)

Good concordances are observed between measurement and simulation of EMC characteristics for the use of 2, 4 then 6 gates in parallel (Fig 5, a). Level of conducted emission (maximum peak) increases to 70mA, with no significant shift of the spectrum frequencies. Variation of time simulation with a nodal simulator (MaxwellSpice) also becomes rapidly prohibitive (10 x time of single gate simulation).

EMC signal on the ground track with 2, 4 or 6 gates in cascade show a slight shift of frequencies spectrum and a stationary level of the peaks in spite of additional consumption with the number of the gates (Fig. 5, b). This indicates the need of a refinement of gates interconnection models with RCL cells to take in account propagation time and input/output loads of the gates, to obtain a better simulation result for this case.

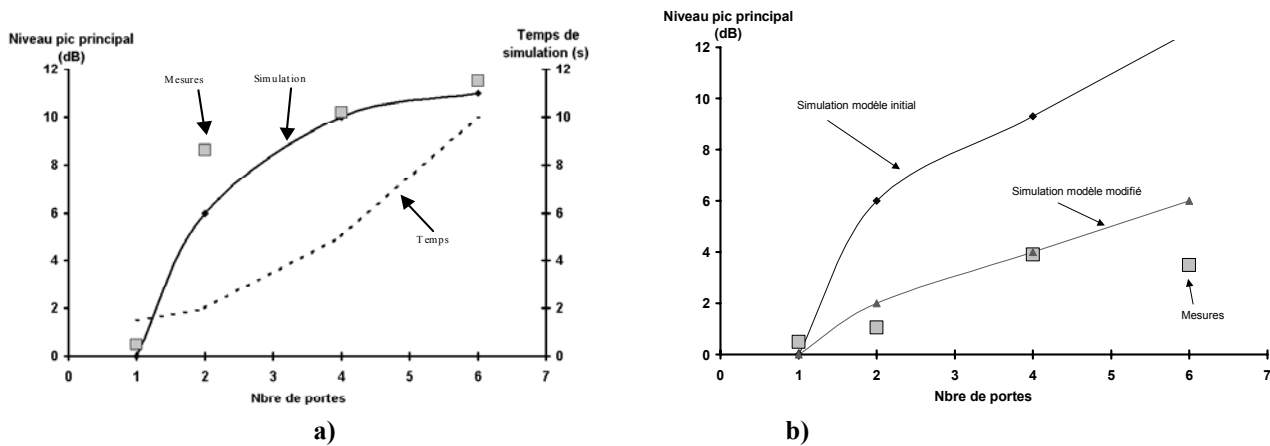


Figure 5 : EMC levels simulated with parallel (a) and cascade (b) logical gates of digital circuit HC04

5. Conclusions

The study presented here is to demonstrate that actual models and simulation tools could be efficient to construct a virtual experiment for an electrical simulation of EMC perturbations of circuits. With the aid of protocol measurement devoted for EMC consideration, and the implantation in Spice simulators of the electrical models associated, we have analysed the reliability and the contributions for EMC simulations of different parameters and electrical functional conditions to the conducted and close radiated emissions of digital components fixed on PCB single layer. From this base model library and methodology associated, minimal effort of complementary modelling is sufficient to obtain good EMC simulation results for various technology of digital components or different implantation of circuits on PCB. For example, good close field spectrum representation on different points of the test PCB can be obtained by our simulation approach.

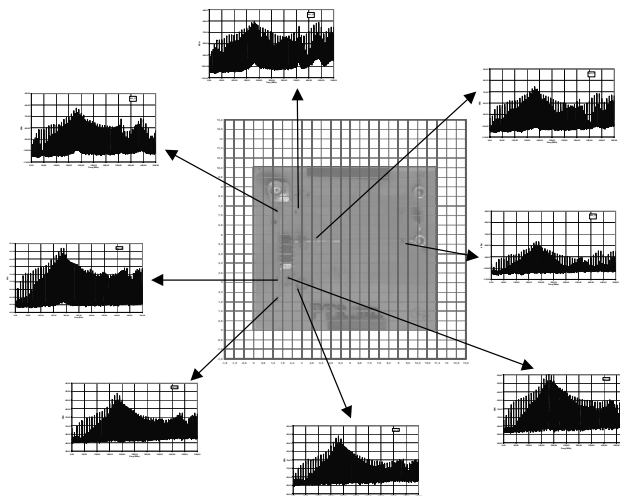


Figure 6 : EMC levels simulated on different points of a test board

This study is designed to include in the future EMC simulation in global tool as virtual experiment and virtual prototype to anticipate EMC coupling in a complex system, like semi-conductor converters associated with electronic driving (programmable logic, DSP, drivers...).

REFERENCES :

- [1] LUBINEAU M. et al. " Vers un modèle CEM des circuits intégrés", CEM COMPO 2000, Toulouse, 27-28 Juin 2000.
- [2] DUBREUIL, "Expérimentation virtuelle pour la CEM : application aux perturbations issues de composants numériques", Thèse de l'Université P. Sabatier, 30 Octobre 2001, Tarbes,
- [3] ANSOFT, Maxwell Spicelink, Technical notes, 1999
- [4] DUBREUIL F., DIENOT J.M., " Une méthode cohérente pour la prédiction des perturbations CEM de composants numériques ", Revue de l'Electricité et de l'Electronique, Juillet 2000.
- [5] CHEN XI, "Parametric analysis method for the construction of a conducted mode emission model", CEM COMPO 2000, Toulouse, 27-28 Juin 2000.
- [6] X. SUN, J. CHILO, "Lignes signal en technologie silicium : du modèle distribué au modèle localisé", Colloque OMD, Le MANS, 3-5 Sept 2001.