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A Reliability Test on PBGA Packaging Through Piezoresistive Stress Sensor

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***Abstract-* Plastic packaging is the mainstream on microelectronic packaging technology at present. As the continuous requirements for smaller but higher density products, failure and reliability issues on MEMS/MOEMS packaging because of the hygroscopic swelling mismatch stress become more and more serious. To this end, this paper presented the stress monitoring methodologies as well as the reliability tests on a typical PBGA (Plastic Ball-Grid-Array) packaging due to hygroscopic effects through the measurements with the piezoresistive stress sensors. It is concluded from the experiments in this work that the hygroscopic mismatch stress is significant for the packaging, and the Weibull reliability model is suitable for the PBGA packaging. In addition, piezoresistive sensors were proven useful for monitoring the stress on the chip inside the packaging structure.**

I. INTRODUCTION

It is well known that plastic materials absorb moisture in a humid environment, but not for the metals and the silicon/glass chips. For typical plastic MEMS/MOEMS packaging, the hygroscopic swelling mismatch on the materials inside the plastic packaging structure lead stress and reliability issues which are seriously concerned for the MEMS/MOEMS packaging designer. Furthermore, as the packaging technologies are continuously moving toward higher performance, smaller scale, and higher density, moisture-induced effects such as the aforementioned hygroscopic swelling stress and the reliability issues becomes increasingly important for the MEMS/MOEMS packaging.

Many studies on moisture-related effects on microelectronic packages have been documented, and it was found that polymer materials exhibited a considerable amount of hygroscopic stress/strain [1]. However, direct hygroscopically-induced silicon die stress measurements and experiments on packaging reliability issues due to moisture effect are seldom available. To this end, we use the piezoresistive sensors as the stress monitoring tool on typical PBGA packaging with 160 balls in this work because the sensors provide in-situ, real-time, and nondestructive stress measurements with relatively low cost. In this paper, Section 2 reports the test sample preparations and the theoretical model for the piezoresistive sensors; the experimental procedure described in Section 3 was designed based on the JEDEC standard as well as the procedures reported in the literature. Moisture-induced effects such as the moisture absorption/desorption rates were also performed. Section 4 and 5 are respectively the experimental results for the hygroscopic and the reliability measurements with discussions, and Section 6 is the brief conclusions of this study.

II. THE TEST SAMPLES AND THE THEORETICAL MODEL

Because of the ability of in-situ and nondestructive stress measurements with relatively low cost [2-4], piezoresistive stress sensors manufactured on test chip surfaces were employed in this study as the stress measurement tools for typical PBGA packaging with 160 balls. Figure 1 shows the test chip layout where A, B, C, D, and E are the sensor locations, and Figure 2 shows a typical 3-element sensor rosette for this work. The dark areas in Figure 2 are the piezoresistors for stress monitoring, and the typical resistance for the resistors is 29 KΩ. Because of the structure symmetry, the effective sensor distributions are extended from Figure 1 and the outcomes are shown in Figure 3. The size of the test chip shows in Figure 1 is 5100 μm by 5100 μm.

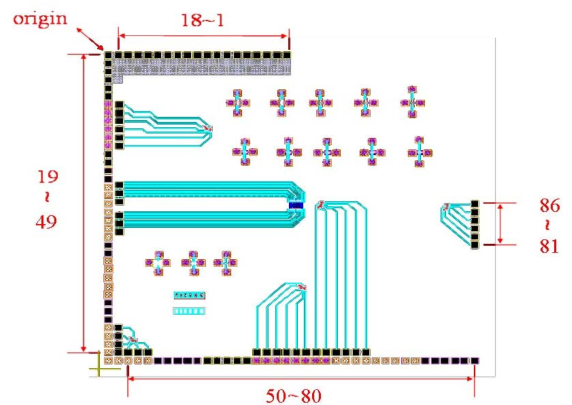

Fig. 1. The Test Chip Layout

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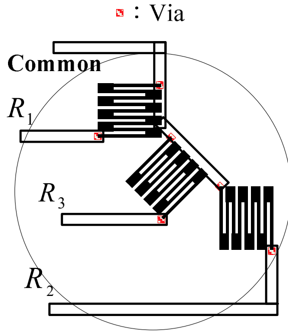

Fig. 2. The 3-element Sensor Rosette

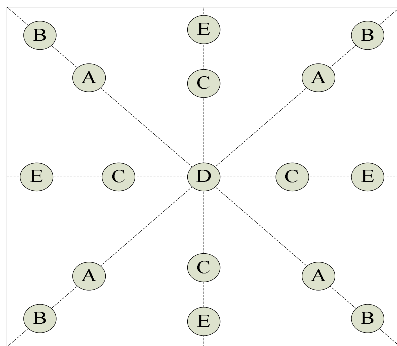

Fig. 3. The Effective Sensor Distributions on Chip Surface

Based on linear models of high concentration piezoresistors [3] as depicted in Figure 2, the relationship between the fractional resistance variations for resistors R_1 to R_3 and the stress and temperature can be written as:

$$\frac{\Delta R_1}{R_{10}} = \frac{\sigma_x}{2}(\pi_{11} + \pi_{12} + \pi_{44}) + \frac{\sigma_y}{2}(\pi_{11} + \pi_{12} - \pi_{44}) + \alpha_1 T \quad (1)$$

$$\frac{\Delta R_2}{R_{20}} = \frac{\sigma_x}{2}(\pi_{11} + \pi_{12} - \pi_{44}) + \frac{\sigma_y}{2}(\pi_{11} + \pi_{12} + \pi_{44}) + \alpha_2 T \quad (2)$$

where σ_x, and σ_y are the in-plane normal stresses and R_{i0} ($i = 1$, 2, and 3) are the initial resistances at the reference temperature, which is approximately 25°C. ΔR_i are the individual resistance variations. T is the temperature difference between the measuring point and the reference. α is the temperature coefficient; and π_{11}, π_{12}, π_{44} are the piezoresistive coefficients. In this work, we employ n-type piezoresistive sensors and Table 1 summarizes the calibrated temperature and piezoresistive coefficients for the sensors. Details of the coefficient calibrations are available in the reference [5]. Stresses in the following sessions were obtained from measuring the resistance changes at each piezoresistors, and then inverting Eqs (1), (2) with the calibrated coefficients listed in Table 1.

TABLE 1
The Extracted Coefficients for n-type Piezoresistive Sensors.

α (10^{-3}/°C)	$\pi_{11}+\pi_{12}$ (10^{-5}/MPa)	π_{44} (10^{-5}/MPa)
1.599	-12.93	-14.25

After parameter extracting, the test chips were packaged into PBGA packaging with 160 balls. The size of the packaging is 15 mm by 15 mm with 1 mm ball pitch, as represent in Figure 4. The ball diameter of the PBGA is 0.45 mm. The packaging samples were next mounted on a 70 mm by 70 mm BCB (Printed Circuit Board) to simulate the real operation conditions.

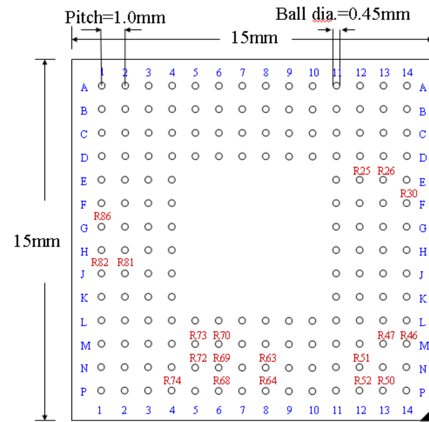

Fig. 4. The BGA Substrate Layout

III. THE EXPERIMENTAL PROCEDURE

The experimental procedure for the hygroscopic experiments was developed based on the IPC/JEDEC J-STD-020B standard [6]. Figure 5 is the experimental procedure for this work. As shown in Figure 5, the SAM (Scanning Acoustic Microscope) inspection was first performed and no delaminations were observed at the beginning of the experiments for all of the testing samples (not shown).

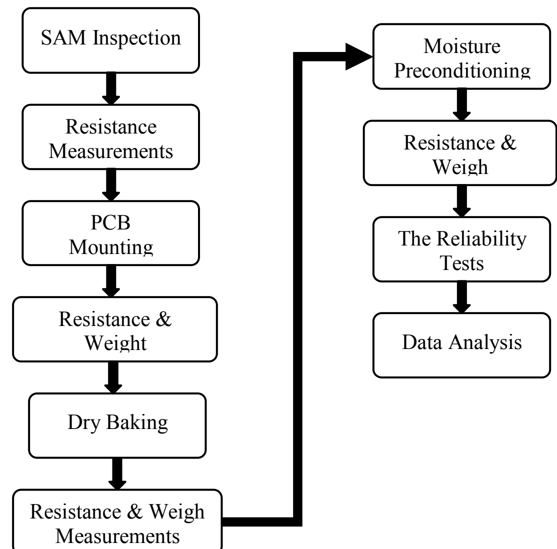

Fig. 5. The Experimental Procedure

We next measured the stress on test chip surfaces inside the packaging due to the board-mounting process by comparing the stress before and after the PCB mounting. The weights of the LFBGA packages were recorded using a Sartorius P200D electronic weight scale. The dry baking process was performed at 125°C for 24 hours to remove existing moisture that may have been introduced. Stress as well as sample weights were recorded before and after dry baking to obtain the differences due to the baking process. Moisture preconditioning was next performed at 85°C and 85 % relative humidity (RH) for 168 hours. Sample weight and internal stress were measured to characterize the moisture preconditioning procedure.

The temperature-humidity cycle test was next performed on the basis of JESD22-A100C standard [7] as the packaging reliability test process. That is, 8 hours of temperature cycling as shown in Figure 6 were performed on the testing samples under 95 % of RH environment. Resistances of the testing samples were continuously recorded during the cycling so that the relationships between time (or, cycle number) and stress at the A ~ E sensor locations were monitored. Furthermore, the time-dependent breakdown resistors were also recorded so that the cumulated failure distribution rates for the sensors during the temperature cycling were obtained.

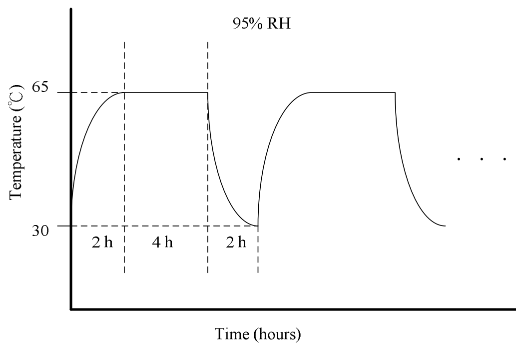

Fig. 6. The Time-Temperature Cycling

IV. THE HYGROSCOPIC MEASUREMENTS

We first measured the stress variation after the board-mounting process. Because the CTE (coefficient of thermal expansion) for the epoxy is larger than for the PCB (Print Circuit Board), when the samples were cooled from high temperature, the shrinkage of the epoxy with the chip was restricted by the PCB. Consequently, 12 MPa to 22 MPa of tensile stress were measured due to the board-mounting process as Figure 7 shows.

After measuring the weight change due to the dry baking process, about 0.5% of relative weights were evaporated. Figure 8 shows about -29 MPa to -47 MPa of compressive stress differences due to baking process were measured. This is because of the shrinkage on the polymer during the baking process, but not for the chips. Consequently, compressive stress was induced on the chip surface.

For moisture preconditioning, the moisture absorption reaches 0.5% of relative weights at about 75 hours, and 0.62% of relative weights were absorbed after 168 hours as shown in Figure 9. That is, the moisture content increased 0.12% in the packaging structure. Figure 10 indicates 48 MPa to 68 MPa of tensile stress were induced on the chip surface. This is because the polymer expanded after absorbing moisture, but not for the silicon chip.

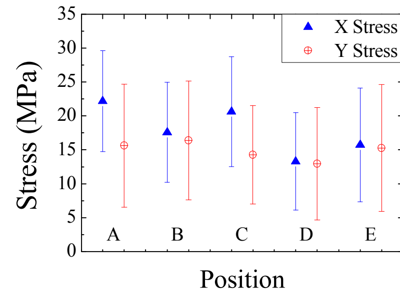

Fig. 7. Stress Due to the Board-Mounting Process

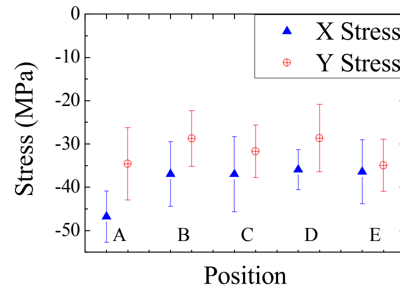

Fig. 8. Stress Due to the Baking Process

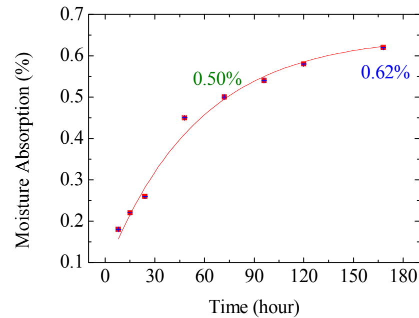

Fig. 9. Moisture Absorption of Relative Weights

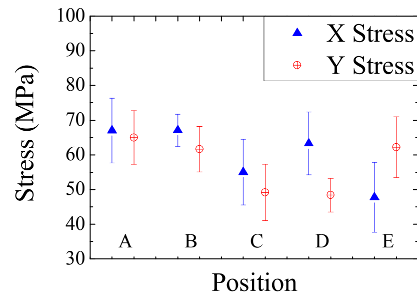

Fig. 10. Stress Due to the Moisture Preconditioning Process

Accordingly, it is concluded that: (1) Comparing with the literature and our early works, the trends and the magnitudes of the above experimental results are consistent. (2) The

hygroscopic mismatch stress is significant for the packaging, but not large enough to lead failures on the chips inside the packaging structure.

V. THE RELIABILITY MEASUREMENTS

We next perform the temperature-humidity cycling test for 500 cycles (4000 hours) to study the reliability issue, and we defined a resistor was "break" when more than 10% of the resistance changed, comparing with the original value, was measured. The cumulative failure distribution rate in Figure 11 is defined as the number of the failed device over the total device number. It is noted in Figure 11 that linear results were fitted between time and the cumulated failure rate on a log-log plot.

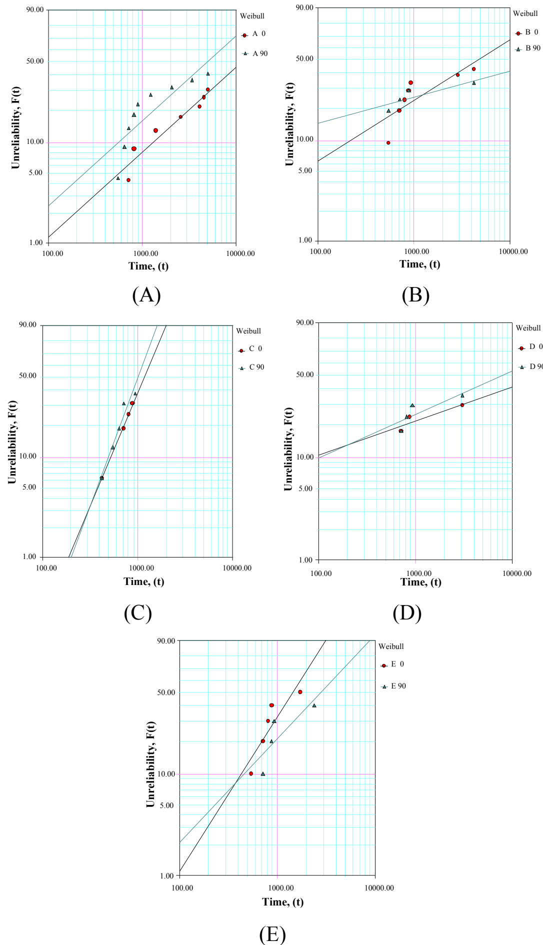

Fig. 11. A Typical Time-Failure Distribution Curve

We next analyzed the cycling data through the reliability software Weibull++ V6, as shown in Figure 12. The results in Figure 12 demonstrated that the Weibull reliability model is suitable for the PBGA packaging. It is also concluded from the results that the damage/failure rate is initially high so that the reliability was not good at the beginning. However, as the cycling increasing, the decreasing failure rate indicates better reliability.

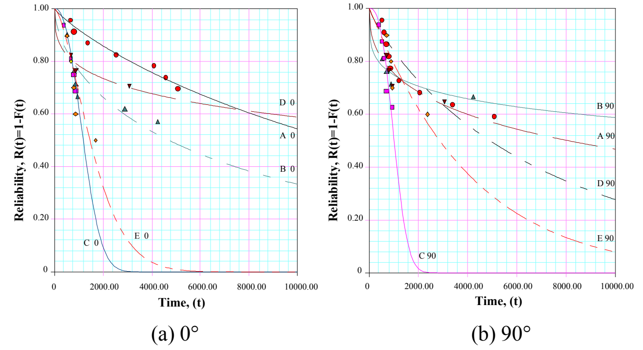

Fig. 12. The Weibull Reliability Model

VI. CONCLUSIONS

In this work, piezoresistance stress sensor was employed as the experimental tool to monitor the stress variations in the PBGA packaging in real-time and non-destructively. In accordance with the JEDEC standard, stress due to the board-mounting process, the baking process, and the moisture preconditioning process were obtained, and it was concluded that all of the processes do not lead chip damage. Furthermore, measurements from the temperature-humidity cycle tests for reliability analysis showed that the Weibull reliability model is suitable for the PBGA packaging.

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