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# A Busbar Like Power Module Based On 3D Chip On Chip Hybrid Integration

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*Abstract*—**The paper focuses on a new generation of power modules, trying to optimize the tradeoff between thermal and EMI managements. At the same time, the packaging approach is considered in order to simplify the implementation of the power dies while improving the reliability of the structure. The approach considers the hybrid integration of the power dies, one on top of the other into a 3D Chip On Chip configuration. Thanks to this structure, the power dies can be directly inserted within electrical plates, the whole structure emulating a busbar like power module. The paper presents the characteristics and the benefits of the approach. Then, it focuses on the practical characterization of two prototypes: a buck converter structure and a full bridge, single phase diode rectifier. Both of them are based on double sided thermal cooling and electro-thermal contacts are obtained by pressure. The prototypes exhibit great performances while offering really reduced parasitic and EMI coupling.**

***Keywords – component, packaging, press pack implementation, Chip on Chip approach, power/drive interaction,radiated field, electrostatic analisys.***

## I. INTRODUCTION

Power module market is dominated by motor drives applications (56%) and traction applications (10%) [1]. The common technology used in those power modules implementation is based on a solder attach between the die and a copper substrate for the backside of the chip **(Fig.1)**. This solder is in charge of the electrical and the thermal management of the die and at the same time it ensures the mechanical attach. On the front side of the chip, electrical management is mostly achieved by the wire bond technology. Maturity, flexibility and low cost are main factors which explain the large use of this technology [2]. However, new topologies and organizations of power devices are investigated, for example with the use of new chip generations [3][4].

Furthermore, even though automotive application is still a small part of the market (4%) [STO], it is growing strongly with about 19% per year. High power automotive applications present specific requirements: high ambient temperature, high number of thermal cycling, compactness…With those issues, the classical electro-thermal management of power modules must be revisited.

After a short survey of the industrial and academic technological solutions taking into account those new constraints, it is shown how technology and concepts are used to maximize benefits of the optimization of the thermal and EMI tradeoff, the electro-thermo-mechanical behavior and reliability

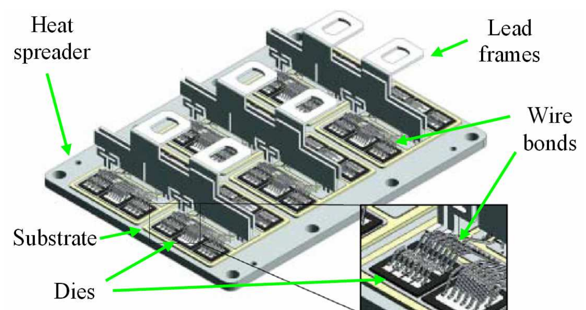


**Figure 1:** 3D view of a planar power module 3.3 kV, 1200 A [5]

A wire bond introduces some undesired parasitic inductances in the range of 10nH. The equivalent inductance will depend on the number of parallel wires and the total inductance of a power module can reach several tens of nano Henrys [6]. Moreover, the wire bonding technique prohibits the use of the power chip front side for heat exchange.

The last important issue related to classical power module concerns the planar distribution of the dies and the interconnects (pads, solder regions, copper leads). These approaches simplify the assembly and the thermal management of the power modules but large electrostatic and electromagnetic coupling are created.

To improve the global EMI behavior and to improve the characteristics and the reliability of wire bonds, interconnexions based on ribbons have been developed [8]. However, in this case, the planar packaging with a single sided thermal management and electrostatic coupling are kept up. Beside this, instead of wire bonding technology but introducing the 3D packaging approach [7][11], new die level implementation techniques are developed:

- nano copper wires interconnection [9]
- metal post interconnection [7]
- solder bump interconnection [10]
- dimple array interconnection [7]
- power overlay technology embedded power [2].

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Those technological alternatives are good solutions to decrease the stray inductance and to allow double sided cooling [12][13]. The new interconnexion techniques offer the possibility of a 3D distribution of the power dies. This leads to high power module compactness and greatly improved EMI behavior. However, the reliability and technological complexity of the implementation is still a limitation for their generalization.

Our 3D approach is inspired by the Busbar concept and is called the Chip on Chip concept (CoC). After presenting the concept, the paper focuses on two practical realizations. Then, a precise analysis of the electromagnetic behavior of the realized 3D Chip on Chip module is carried out thanks to simulation and practical characterizations.

## II. CHIP ON CHIP CONCEPT

### *A. Concept*

We have developed a power module based on the Chip On Chip (CoC) concept. The main goal of this approach is the integration of the power dies inside a busbar like 3D structure as depicted on **Fig.2**. Busbar interconnects are well known for their extremely low stray inductances [14]. The integration of power devices directly within a bus bar structure offers also the opportunity to minimize parasitic coupling within the switching cell but also among switching cells of a multi phase converter. Indeed, the busbar structure minimizes radiated and conducted EMI. For this structure to exist it is necessary to develop double side wide and simple to implement electrical and thermal paths since, in this new configuration, the heat can be removed from the bottom and the top faces of the power dies.

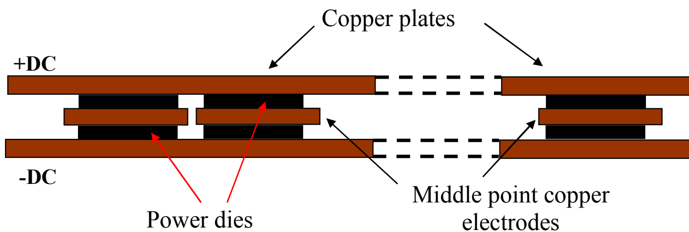


**Figure 2:** Power die assembly into a busbar like power module based on the Chip on Chip concept

### *B. Implementation*

Soldering, bump or copper bonding approaches can be used to assembly the whole structure [7][11]. However the global reliability of the module may be reduced. This is an important issue since several layers with various materials are sandwiched together in this approach. Such a structure, with various coefficient of thermal expansion (CTE) could quickly fail from excessive thermo-mecanical stresses. Therefore, another technique has been considered for its higher reliability and robustness. It is based on the low force press pack technique [16]. This approach is interesting since the power dies are assembled one on top of the other. High pressure is obtained at low force since the contact surface is reduced compared to classical planar and paralleled dies.

Practical demonstrators can be built in such a manner. Implementation is based on the stack of various elements **(Fig.3)**. The chips are packaged between two copper plates. A polycarbonate footprint allows the positioning of the chip and the molybdenum pin, all of them being inserted between the copper plates. Molybdenum layers are inserted on top of the dies. The quite similar CTE between molybdenum and silicon increases the robustness of the pressure contacts.

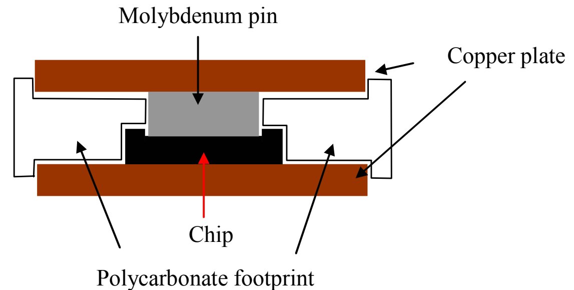


**Figure 3:** Implementation principle

### *C. Realizations*

Two practical demonstrators have been realized: a single phase rectifier and a power structure using an ordered switch, a buck converter. Their realization has been carried out in order to study and to analyze the concept and then to validate it.

#### *1) Single phase rectifier*

The first prototype is a single phase 400V-40A HF rectifier. **Fig.4** presents a side view of the assembly and the power module prototype is depicted on **Fig.5** and **Fig.6**. The module is composed by 4 power diodes SIDC81D60E6 (600V/200A; Size 9*9mm; Thickness 70µm) stacked between copper layers 1mm thick. The molybdenum pins are 2mm thick. All the structure is maintained between two heat sinks by a clamping system. The complete stack (without cooling and clamping system) is about 7mm thick. On **Fig.4** polycarbonate footprints are not drawn to allow better comprehension. A force sensor is inserted in the upper heat sink allowing the measurement of the clamping force. The time domain waveforms showing the regular operating of the device (**Fig.7**) are obtained under 500N clamping force.

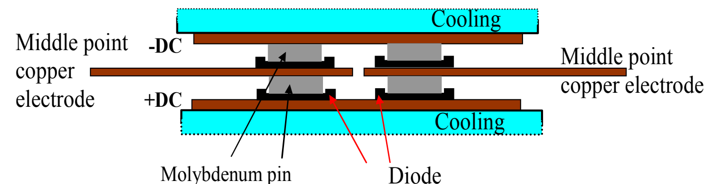


**Figure 4:** Side view of the rectifier

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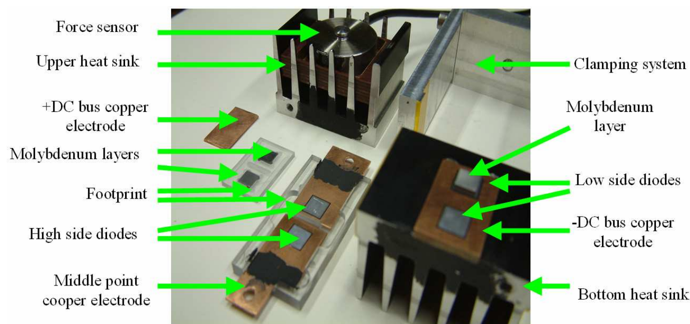


**Figure 5:** Picture of all pieces of the single phase rectifier chip on chip power module

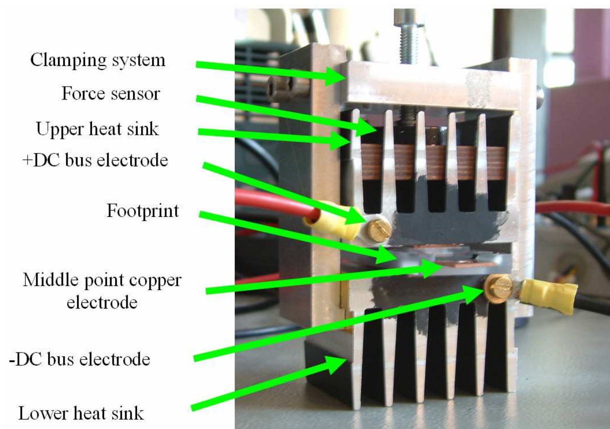


**Figure 6**: Single phase chip on chip power module

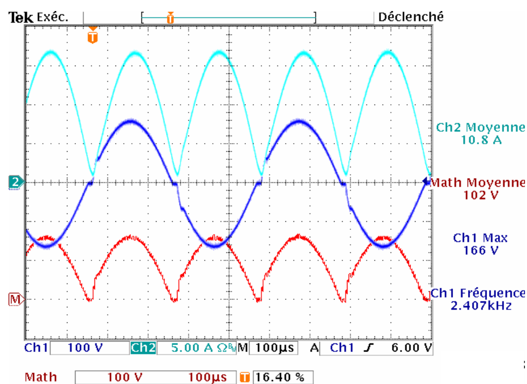


**Figure 7:** Time domain waveforms

It is important to notice the particular simplicity of the mechanical elements of the stack. The 1mm copper layers are just cut up with the good dimensions. A good roughness is obtained by a manual polishing. The polycarbonate footprints need a special care to guaranty the good positioning of the different pieces, but the mechanical properties of this material allow an easy manufacture. Actually, this power module is a very easy to make and easy to implement device. The only limitation of this approach comes from the thickness of the Molybdenum parts which increase considerably the distance between the copper plates. This leads to average EMI behaviour. In order to improve greatly this, Molybdenum contact should be removed and replaced with another element, less thick.

*2) Buck Converter*

This second prototype needs an ordered switch and a diode, it is a 400V-40A HF buck converter. The implementation principle is again based on the CoC concept.

In **Fig.8** we can see how the gate contact is brought to the chip gate pad. The gate contact is inserted in the middle copper plate and crosses the Molybdenum pin. The control path and the power path are deliberately separated. Benefits of this organization will be shown in Part III.

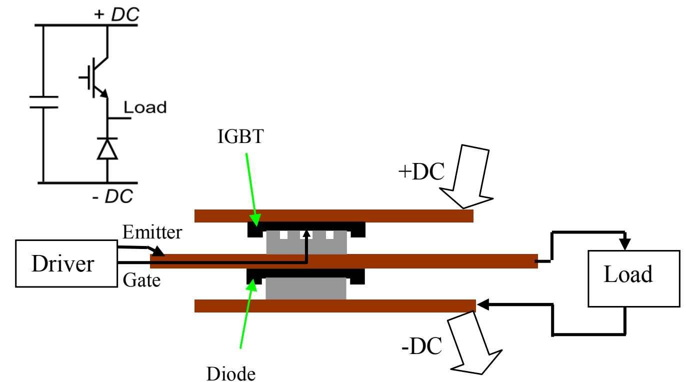


**Figure 8:** Electrical circuit and side view of the buck converter

**Fig.9** presents its practical implementation with double side cooling and clamping system. The power diode is a SIDC81D60E6 (600V/200A; Size 9*9mm; Thickness 70µm) and the IGBT is a SIGC121T60NR2C (600V /150 A; Size 11*11mm; Thickness 100µm) both from Infineon. The module thickness is around 6mm. Length and width are about 4cm and 2cm respectively.

A previous study [16] has shown that satisfactory electrical and thermal contacts are obtained for forces in the range of 500N. Then the operating clamping force is 500N.

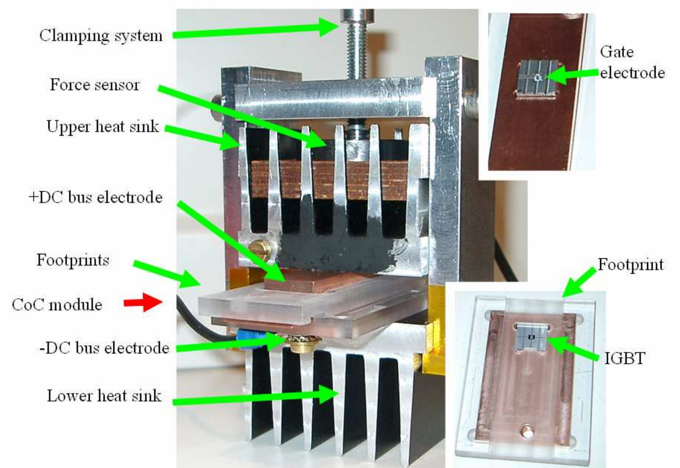


**Figure 9:** Buck converter power module based on the Chip on Chip 3D power module assembly

**Fig.10** presents time domain waveforms showing its regular operation. Operating frequency is about 20kHz. Almost no voltage overshot is visible at IGBT turns OFF.

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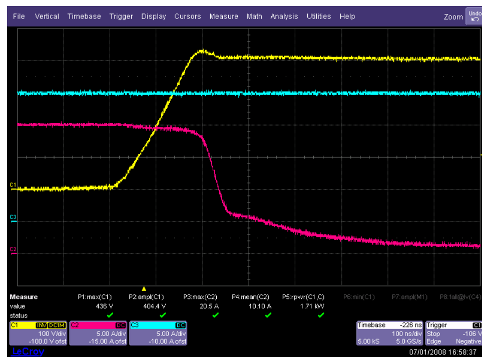

**Figure 10:** Switching waveforms of the buck converter

Both realized power modules, the rectifier and the buck converter, have illustrated the Chip On Chip concept. Electromagnetic benefits of this approach will be discussed now.

## III. ELECTRO-MAGNETIC ANALYSIS OF THE CHIP ON CHIP CONCEPT

The magnetic behavior of the Chip On Chip module presented **Fig.8** is outlined thanks to the equivalent schematic plotted in **Fig.11**. The 3D assembly gives in important contribution to radiated EMI reductions, maximizing the mutual magnetic coupling among the copper plates facing each others. As it is depicted on **Fig.11** magnetic interactions between the power circuit and the driver circuit are reduced as much as possible. Indeed the power current and the driving current share almost no common conductive path and their electromagnetic couplings are extremely reduced thanks to the 3D assembly. In a classical power module, there is most of time a stray inductance (wire bonding inductances **Fig.1**) at the emitter of the IGBT that is shared between the power conductors and the gate driver conductors. Besides, since heat removal is now performed on both sides of the power module, there is no more need for thermal and EMI compromises, allowing to place power dies as close to each other as possible. In the 3D modules, the heat is removed from both sides and copper conductors can be organized in 3D making possible the whole structure to be fully optimized from both thermal and EMI point of views.

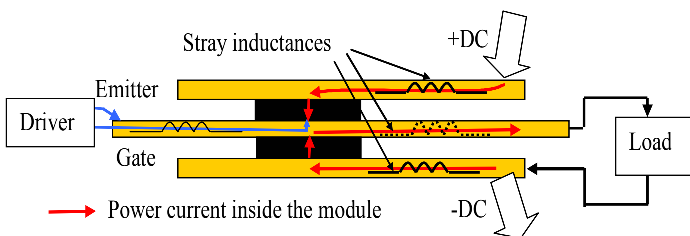


**Figure 11 :** Stray inductances on the press pack module

### A. *Magnetic Power/Drive interactions*

Decoupling between power and control circuits has been investigated. Experimental comparisons between a classical power module and a Chip on Chip power module show the benefits offered by the 3D structure with respect to the power/drive decoupling.

In **Fig.12** is depicted a commutation cell with the existing stray inductances present for each conductor in the module. It is also depicted the possible mutual coupling among inductances. Due to the common impedance coupling between power and drive conductors and the emitter stray inductances, a parasitic voltage is induced in the gate circuit during switching. This phenomenon leads to an increase of switching losses transitions, is at the origin of EMC problems and it requires to over rate power devices [15].

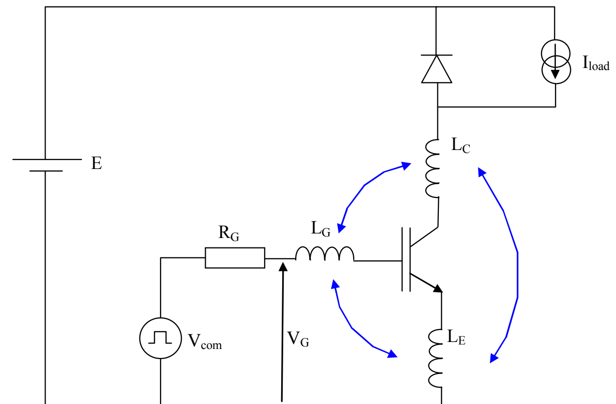


**Figure 12:** Representation of a switching cell for the power/drive interaction studies

The stray inductances are introduced by the electrical interconnections. For the investigation of the interactions, we decided to realize and to analyze modules without power chips. That allows to focus the observation on the interconnections and electrical interactions without the possible interaction with the power devices. A high frequency current generator is used for the experiment. The current is injected in the power circuit and the observations are carried out on both power and drive circuits. In **Fig.13** is depicted the experimental principle. Measurements have been carried out on two types of power modules: a planar module designed as a classical power module and a 3D CoC power module. In **Fig.14** is depicted the planar layout used for the experimental measures and simulations. It represents a possible layout for a switching cell. The copper heat spreader beneath the ceramic substrate (**Fig.1**) is not depicted but it is present for measurement and simulations

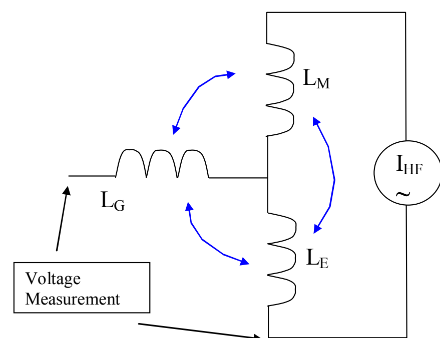


**Figure 13:** Power/drive interaction measurement principle

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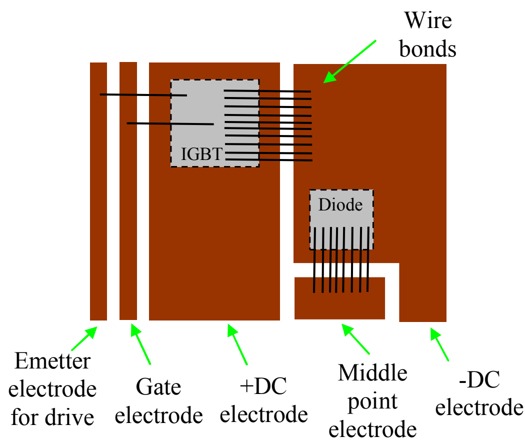


**Figure 14:** Planar module layout used for measures and simulation.

The measurement conditions are: the same current is injected for the both devices, a 4.4MHz sinusoidal current 1.2A peak to peak. As far as planar module is considered, observing the gate circuit showed that an induced voltage could be measured. This has been depicted on **Fig.15**. As it can be seen, the voltage amplitude is 200mV peak to peak. Since this voltage is 90° ahead from the current, the equivalent impedance is purely inductive. The waveforms being sinusoidal, this impedance can be computed and is equal to about 6nH. Such inductive effect could create a voltage on the gate circuit about 6V for a di/dt in the range of 1000A/µs. As far as the 3D module is concerned, we have not been able to measure a voltage on gate circuit under similar conditions. This clearly states on decoupling between power and gate circuits in our 3D packaging approach.

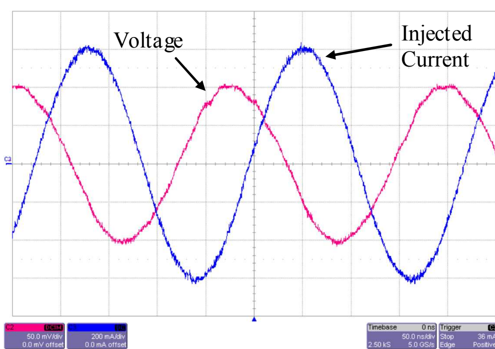


**Figure 15:** Measurement waveforms for a planar module

For the planar module, interactions between drive circuit and power circuit are clearly demonstrated. That's why a special care and an optimization of the planar power module layout with the minimization of the power/drive circuit coupling is always necessary and has been studied in [15]. With the Chip On Chip structure, a natural decoupling of the power circuit and the control circuit is achieved, simplifying the design while increasing the quality of the module.

## *B. Magnetic field simulations*

Compared to other modules, in a Chip On Chip power module, the parasitic inductance and self magnetic coupling are almost completely cancelled. Furthermore, the 3D module should also exhibit fairly good radiated and conducted EMI levels. This has been studied in simulations and as a first analysis, it can be seen that the 3D modules that has been realized exhibits comparable radiated magnetic field compared to the classical planar topology presented in **Fig.14** with a ground plane.

We considered that our device was operated at 20kHz switching frequency. The switching transitions introduced harmonic currents depending on the rise time. With regards to our switching conditions, it was interesting to estimate the magnitude of the magnetic induction with a 2MHz current excitation. **Fig.16** shows magnetic induction for a classical power module. The observation plan is in a parallel plan of the substrate located at 3mm above the copper surface. As expected, the maximum values are observed near the wire bonds. The radiated induction field of the 3D module in similar simulation conditions is depicted on **Fig.17** and **Fig.18**. As it could be expected, the maximum induction is located within the busbar like structure. For both modules, magnitudes are in the same range.

These results are obtained whereas the distance between the busbar like structure is 5mm. If this distance can be reduced to about 1mm, the magnitude of the radiated field is greatly reduced. A simulation has been carried out in order to estimate what could be the benefit of such implementation…

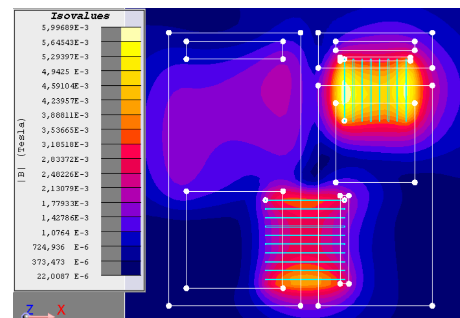


**Figure 16:** Induction of a classical buck converter

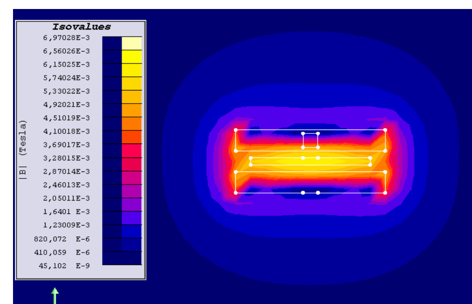


**Figure 17:** Induction of a Chip on Chip buck converter (front view).

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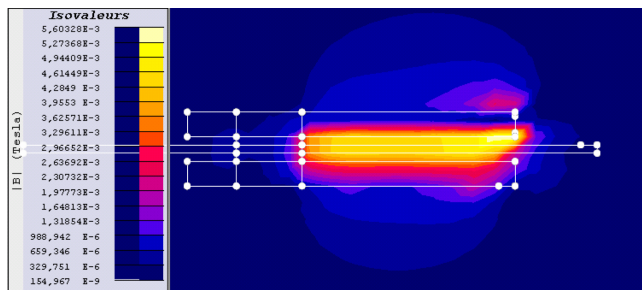


**Figure 18:** Induction of a Chip on Chip buck converter (side view).

The magnitude of the magnetic field for the two modules in two different directions (**Fig.19**) is plotted on **Fig.20**. We can see that depending on the orientation, the magnetic fields are greater in one solution or in the other.

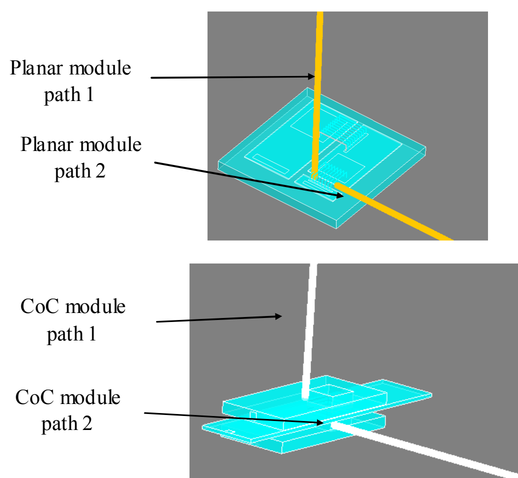


**Figure 19:** Induction measure paths

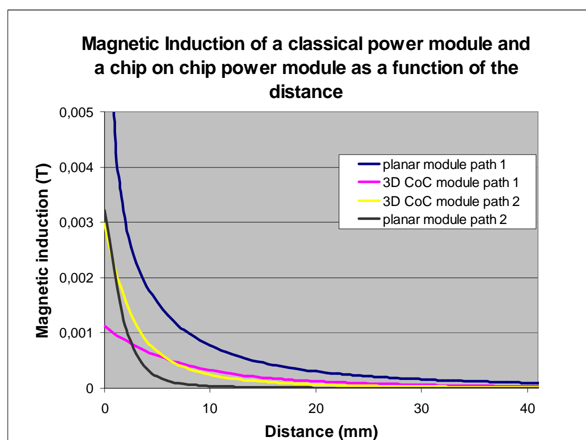


**Figure 19:** Magnetic induction as a function of the distance

These simulation results are encouraging because the structure of the 3D module is at the moment far from being a busbar like structure. This is due to the Molybdenum pieces which enlarge a lot the vertical distance among the copper layers. If the thickness can be reduced, we expect to greatly reduce the radiation magnitudes, making the 3D module a well suited solution for modular assembly at minimum design considerations.

## IV. Electrostatic Analysis of the Chip on Chip Concept

In order to study the conducted common EMI which are very sensitive to the power module structure, we have used the experimental setup of the previous section. This time, the current excitation has been replaced by a voltage excitation. As it is well known, common mode EMI propagation sources are mainly the voltage patterns located at each switching cell middle point. Then, depending on the electrostatic coupling of this electrode with respect to ground, common mode EMI propagation paths are more or less important. Since, the common mode EMI sources can't be reduced without acting on the switching patterns, it is mainly acting on propagation paths that can be lowered conducted common mode disturbances.

For planar based modules, there is a large common mode parasitic capacitor located underneath the lower side IGBT plus diodes power dies. As a result, common mode currents can be quite large and often, common mode filters are required. As far as our 3D sandwich structure is concerned, it is different since now, the middle point electrode has no direct electrostatic coupling with respect to ground. Indeed, it is located between two copper plates both of them being connected to plus and minus DC bus voltage potentials. As a result, there is no more common mode propagation path available for common mode current to circulate. This clearly appears on the equivalent schematic depicted **Fig. 21**.

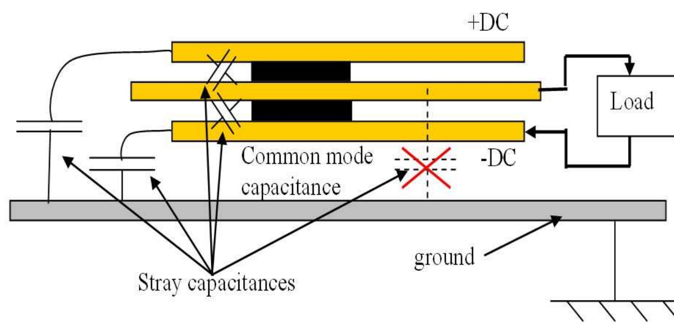


**Figure 21:** Equivalent electrostatic schematic of the 3D Chip on Chip module.

Experiments have been carried out on both planar and 3D packaging in order to check for this point. The plus and minus electrodes of both modules have been clamped to a DC voltage while the middle point electrode has been excited with a pulsed voltage source. Both modules are then put on a ground plane in order to check for common mode currents. This is an usual EMI testing procedure.

As it could be expected common mode current in the planar structure is visible (**Fig.22**). Thanks to the measurement, the parasitic capacitor can be estimated to about 10 to 20pF. On the other hand, on the 3D module (**Fig.22**), no characteristic current is visible. This means that a full electrostatic decoupling is obtained thanks to this packaging

approach. These results will have to be confirmed in a full practical implementation of the power module. This is out of the scope of this paper.

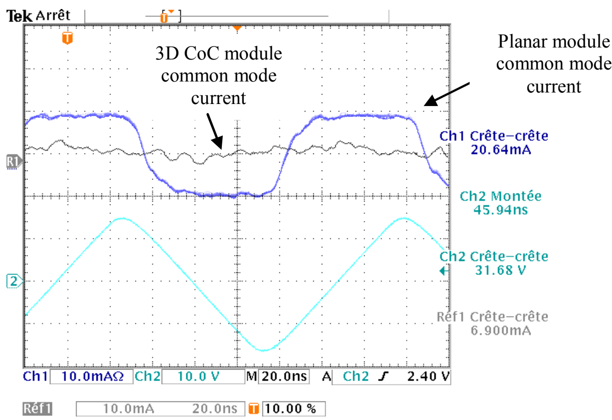


**Figure 22:** Common mode currents measurements for a planar module and a 3D module with a triangular excitation source.

## V. Conclusion

The paper presents an original power module assembly into a 3D configuration. The structure of the module is based on the Chip on Chip concept which is used here in order to separate electrical and thermal managements trying to take advantage of the third dimension. The realization and assembly of the structure is presented and discussed. It appears to be quite simple realize and to implement. The following part of the paper presents an analysis of the 3D power module. It appears that the studied 3D configuration exhibits a perfect decoupling between power side circuit and gate circuit. Besides, the power module is expected to offer extremely reduced switching cell inductance as a function of the assembly technology. Finally, the 3D assembly considered in this paper allows to confine conducted common mode EMI in a simple manner. Most of the observations are validated thanks to practical experiments.

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