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Peculiarities of RSFQ Applications with High- T_c Superconductors - an Approach for Design

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Abstract. The significant progress in the development of Rapid Single Flux Quantum (RSFQ) logic circuits indicates their potential for fast cryoelectronic device applications. The possibilities of realizing logic components based on this principle with high- T_c superconductive (HTS) materials have been studied by means of numerical computations. The most crucial task is to manage the trade-off between desired high critical currents and the loop inductances, which can not be made arbitrarily small. Parameter extractions for typical layout arrangements and dynamical simulations including thermal noise give justification for expecting small scale HTS-RSFQ implementations.

1. INTRODUCTION

The Rapid Single Flux Quantum (RSFQ) logic family is a superconductive kind of digital circuit technique in which the data are not represented by static voltage levels, but moreover by short transient voltage pulses. Their propagation in an arrangement of basic cells (Josephson junctions, coupled by an inductance L) goes ahead with the transfer of magnetic flux in the amount of the flux quantum $\Phi_0 = h/2e$ from cell to cell. The absence or presence of a flux quantum in a cell with storing properties is referred to as a binary '0' or '1', respectively [1]. So, all transmission and processing of the data is based on the directed and clocked propagation of single flux quanta. The RSFQ technique is based on the use of overdamped Josephson junctions, for which the condition $\beta_c = 2\pi I_0 R_N^2 C_J / \Phi_0 < 1$ with I_0 : the critical current, R_N : the normal resistance and C_J : the capacitance of the Josephson junction, holds. Because of the typical values of R_N and C_J , this requirement is already fulfilled in HTS Josephson junctions and has not to be maintained by means of additional shunt resistors. Up to now, a remarkable progress has already been achieved with low- T_c superconductors, where a variety of very high-speed circuits with low power consumption has become feasible on a system level [2-4]. Recently, the successful operation of some RSFQ modules with HTS materials has been shown [5-7]. For a stable operation of RSFQ devices at temperatures above 4.2K, the critical currents I_0 of the Josephson junctions have to be raised up to compensate the effects of thermal fluctuations [1]. However, the $I_0 L$ product of the single cells is restricted by the basic operation principle and increasing the critical currents requires a proportional decrease of the cell inductance. Thus, the realization of small inductances is an essential precondition for an RSFQ technique with high- T_c superconductors. Because the restrictions of diminishing L are much more stringent, the inductances have to be designed as small as possible. Subsequently, the critical currents are adjusted to the desired characteristic cell parameter $\beta = 2I_0 L / \Phi_0$. This gives rise for a review of the known attempts for obtaining small inductances. After a study of one contemporary concept, some conditions for adjusting I_0 are considered. In the end, a way of judging on the circuit's failure rate is shown.

2. INDUCTANCES IN THIN FILM APPLICATIONS

In superconducting structures, the device inductance is composed of a geometry-dependent part L_g and the kinetic inductance L_{kin} which is due to the inertia of the superconducting charge carriers. The latter part is of considerable amount in HTS thin film structures because of the small film thickness and the large magnetic field penetration depth. Furthermore, the small lateral structure dimensions cause an additional necessity for numerical field calculation in the investigation of the inductive situation.

For several thin film layout arrangements, the inductances have been computed. In this section, results of model calculations for a very promising situation are presented. All of the following calculations have been done using a 3D inductance calculation software for superconductive thin film structures [8]. For greater generality, in the structures the influence of the current penetration into the Josephson junction has not been taken into account. One way of achieving small inductance values consists in the preparation of slit-like holes with typical widths below $1\mu\text{m}$ and a length of several micrometers. This kind of structure has already proven to work well for a couple of HTS based RSFQ circuits (see e.g. [5]). One advantage could be seen in the good scaling behaviour of the inductance values with the slit length. This circumstance, which also has been verified experimentally [9], can clearly be demonstrated by means of computer calculations. For this purpose, narrow slits surrounded by a $w = 5\mu\text{m}$ wide thin film border of 200nm thickness were analyzed. Inductances were computed for slit widths in the range of $0.3\mu\text{m} \dots 1.2\mu\text{m}$. The slit length l was varied from $3\mu\text{m}$ to $20\mu\text{m}$ and magnetic field penetration depths λ between 150nm and 400nm were assumed. The calculation results are shown in Figs. 1 and 2.

Figure 1: Calculated inductance vs. width of the slit for several values of magnetic penetration depth. Increasing the slit length has only minor influence on the resulting inductance value. This effect becomes less pronounced with increasing λ .

Figure 2: Calculated inductance vs. slit length for several values of λ . A linear dependence between inductance and slit length can be observed.

It can be seen that the width of the narrow slit is of minor influence on the inductance, whereas the latter is nearly scaled by the slit length.

A certain drawback of this concept arises from the fact that it should be very hard to contact such a hole by Josephson junctions from other than the long sides. In fact, all of the known realizations show a parallel one-direction alignment of the Josephson junctions which causes restrictions in the designable circuit topologies.

3. SUITABLE CHOICE OF THE JOSEPHSON JUNCTION WIDTH

Presently, thin film grain boundary Josephson junctions are frequently utilized. Therefore, our considerations will focus mainly on this type of Josephson junctions.

The cross section area of a grain boundary Josephson junction relates its critical current I_0 to the technologically determined critical current density J_0 . With a given film thickness t the junction properties can be ideally expressed in terms of its width w_{JJ} . However, this quantity is strongly related to the inductive aspect of circuit design. Because of the typically small lateral dimensions, the kinetic inductance is of significant or even dominant magnitude. Thus, the width of the Josephson junction not only determines the critical current of the Josephson junction, but is moreover of great influence on the loop inductance. Narrowing the border width w and simultaneously the width w_{JJ} of the Josephson junction increases the cell inductance and decreases the critical current. Because of the nonlinear influence of w on L_{kin} , the inductance increase does not compensate the I_0 decrease. Therefore, the choice of the width w is an essential issue in the layout development. Additional design constraints result from considerations on the required noise immunity [10,11] and from the aim of avoiding a flux flow behaviour [11]. The reliable operation, characterized by a sufficient stability against noise induced accidental switching, is given for small ratios of the energy of thermal fluctuations to the Josephson coupling energy

$$\Gamma = \frac{k_B T}{(I_0 \Phi_0 / 2\pi)} \ll 1, \quad (1)$$

with k_B : Boltzmann's constant, T : temperature. For RSFQ circuits, the requirement $\Gamma^{-1} \approx 500$ is formulated as a demand for practical applications [1]. Therefore, Γ acts as a design objective, i.e. as an initial target parameter in the design flow. Relating the critical current I_0 to the Josephson junction geometry in the above mentioned way, a minimum Josephson junction width w_{min} follows as:

$$w_{min} = \frac{2\pi k_B T}{J_0 \Phi_0 \Gamma t}. \quad (2)$$

On the other hand, avoiding the long Josephson junction regime [12] leads to an upper limit of

$$w_{max} = 4 \lambda_J. \quad (3)$$

Combining both limits to

$$w_{min} = \frac{2\pi k_B T}{\Phi_0 J_0 \Gamma t} < w_{JJ} < w_{max} \approx 4 \sqrt{\frac{\Phi_0}{4\pi\mu_0\lambda J_0}}, \quad (4)$$

requirements on the choice of w_{JJ} in dependence of the technology-defined J_0 can be established. A typical situation for a specified temperature of 50K, film thickness t of 150nm and a magnetic field penetration depth $\lambda = 200$ nm is shown in Fig. 3. The x -axis range is chosen according to J_0 data reported in [13]. The graphs are parametrized by Γ , which influences the switching error rate of a Josephson junction and therefore acts as a design objective.

Eq. (4) has only a solution for $w_{max} > w_{min}$. This condition can be used to derive a criterion for the critical current density J_0 required for proper circuit operation. From Eq. (4) follows

$$J_0 > \left(\frac{2\pi k_B T}{\Phi_0 t \Gamma} \right)^2 \cdot \frac{\pi \mu_0 \lambda}{4 \Phi_0}. \quad (5)$$

This relationship can be utilized for determining the J_0 of the Josephson junctions, e.g. by choosing the misorientation angle of bicrystal substrates [12]. Comparing the graphs in Fig. 4 with typical data of bicrystal Josephson junctions (e.g. Fig. 2 in [13]), it becomes clear, that with the present state of the art, grain boundary Josephson junctions do not ensure a noise immunity sufficient for large integration levels.

Figure 3: Ranges of w_{JJ} vs. J_0 for different levels of noise parameter. Suitable values can be found between the w_{min} and the $4\lambda_J$ curves.

4. SIMULATIONS

For a better understanding of the degradation of the circuit performance under the influence of elevated noise levels, transient noise simulations have been carried out. These studies relate the actual device parameters to the prospective circuit performance. For this purpose we used the ELDO circuit analysis software [14], which was made fit for this task by the development of Josephson junction circuit models. Usually, the circuit under consideration is simulated over a time interval which duration has to be compromised against the computational costs. The number of noise introduced switching errors can be obtained from a comparison of the expected phase advance $\Delta\phi_{expected}$ at the output Josephson junction with the calculated one $\Delta\phi_{noise}$. Since every switching event causes a 2π phase leap, the number of switching errors follows from the integer part of $|\Delta\phi_{expected} - \Delta\phi_{noise}|/2\pi$. The validity of this approach has been proven by a comparison of a simulated error rate to a theoretical one which is given for overdamped Josephson junctions by

$$p = \frac{1}{4\pi R_N C_J} \left[\sqrt{1 + 4\beta_c \sqrt{1 - (I_b/I_0)^2} - 1} \right] \cdot e^{-\frac{\Delta u}{T}} \quad (6)$$

with the bias current I_b of the Josephson junction and its normalized potential wall $\Delta u = 2\sqrt{1 - (I_b/I_0)^2} - 2I_b/I_0 \arccos(I_b/I_0)$ [15, 16]. Every noise induced overcoming of Δu accidentally leads to a phase advance and means a switching error. The error rates resulting from the computer experiment were fitted to the thermal activation model relation $p_{error} = A \cdot e^{-\frac{B}{T}}$ [16]. For a Josephson junction with typical values $I_0 = 300\mu A$, $R_N = 2\Omega$, $I_b/I_0 = 0.8$, and $C_J = 0.1pF$, the error rate vs. T derived from noise simulations is shown in Fig. 5. The coefficients were determined to $A = 0.1463 \cdot 10^{12}s^{-1}$ and $B = 1483.0K$ and agree fairly good with the theoretical predictions of $A = 0.1468 \cdot 10^{12}s^{-1}$ and $B = 1219.3K$. Assuming that the behaviour of the entire circuit resembles that one of a single Josephson junction, the method was extended to circuits containing more than one Josephson junction.

The parameters A and B obtained from the fitting procedure can be used to predict a temperature range of stable operation. For the example in Fig. 5, the following error rates result from this extrapolation: $T=40K$: $p_{error40K} = 11.6 \cdot 10^{-6} s^{-1}$, $T=50K$: $p_{error50K} = 19.2 \cdot 10^{-3} s^{-1}$, and $T=77K$: $p_{error77K} = 6.32 \cdot 10^2 s^{-1}$. For gaining some insight in realistic scenarios, simple RSFQ circuits have been laid out with respect to actual technological rules and conditions. Subsequently, the implementation has been evaluated by this transient noise simulation approach. As an example, Fig. 6 shows the derived temperature dependence of the error rate for a particular RSFQ circuit with 21 Josephson junctions which is described in [17]. Below 30K, the circuit under consideration shows an extrapolated error rate of less than about one error per year.

Figure 4: Dependence of minimum J_0 on the desired noise parameter. Curves indicate the J_0 required for a given Γ^{-1} at various temperatures.

Figure 5: Numerically determined error rates for a single Josephson junction at several simulation temperatures (dots) and results of the fit to the extrapolation function (solid line).

Figure 6: Extrapolated noise induced error rate of a particular HTS RSFQ circuit (simulation results).

5. CONCLUSIONS

The aim of implementing RSFQ logic components with the presently available HTS technique imposes severe constraints on the design, layout, and the complexity of the circuits. The requirements on design and technology are rather high. Of great importance is the utilization of high- I_0 Josephson junctions. Here, a trade-off exists, because the cell inductances can not be diminished arbitrarily. In the paper, a design approach has been investigated quantitatively on the basis of numerical inductance calculations. The shape of the cell has been discussed together with the requirements on contemporary HTS grain boundary Josephson junctions. Furthermore, the connection of the final device reliability – expressed by Γ – and the Josephson junction's critical current density has been presented. Another topic of interest focused on the impact of noise on the operation of a circuit which is composed of a number of elementary cells. Transient noise simulations of the whole test circuit at temperatures above the cryogenic range resulted in fitting parameters for the extrapolation of the noise induced error rate at given temperatures. These estimations indicate a stable operation of a particular RSFQ circuit under investigation up to $T \approx 30K$.

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