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MODELLING.

STATIC AND HIGH FREQUENCY MODELLING OF VERTICAL CHANNEL MOS TRANSISTOR (V.MOS)

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Résumé. — Le but de cette communication est de décrire les méthodes d'établissement des modèles, en régime statique et dynamique petits signaux, du transistor à effet de champ à grille isolée à canal vertical (V.MOS). En prenant en compte les mécanismes de saturation de vitesse, il sera principalement montré que (i) la caractéristique de transfert courant drain-tension grille est linéaire (ii) les paramètres dynamiques hautes fréquences sont indépendants de la tension grille-source. Enfin, compte tenu de la configuration de la structure (drain N^--N^+ couvrant toute la surface) il apparaît que les fréquences maximales d'utilisation ne peuvent dépasser la gamme des UHF.

Abstract. — The aim of this paper is to describe the modelling methods of the vertical channel MOS transistor (V.MOS) under DC and small signal HF conditions. By taking into account the scattering velocity saturation mechanisms, it will primarily be shown that (i) the drain current-gate voltage transfer characteristic becomes linear and (ii) the dynamic HF parameters are independent of the gate-source voltage. Moreover it will appear that the maximum working frequencies cannot overcome the UHF range.

1. **Introduction.** — This paper gives the results of a static and dynamic small-signal analysis for the vertical N channel metal-oxide-semiconductor transistor. The originality of this modelling is the introduction of the following physical mechanisms, under DC conditions, (i) non uniform doping density in the source-drain direction (ii) saturation effects of the scattering velocity (iii) crystal heating due to the dissipated DC power. In dynamic range the treatment is based on : (i) the distributed configuration of the channel (ii) the mobility reduction (short channel effects) (iii) the influence of stray elements-access inductances, drain-diode capacitance and conductance, overlap capacitances.

Fig. 1. — Cross-section of the device : chip area 10^{-2} cm² ; number of channels : 128 ; channel length : $1.5 < L < 2.5$ µm; total channel width : $Z = 2.80$ cm ; gate oxide thickness : $x_0 \simeq 600$ Å ; thick oxide thickness : $x'_0 \simeq 6\,000$ Å ; N drift region length : 10 µm ; N region doping : 10^{15} cm^{-3} ; average channel doping : 8×10^{15} cm$^{-3} < N_A < 10^{16}$ cm^{-3}; overlap L' length $\simeq 0.7$ µm.

The tested devices were fabricated by using the anisotropic-etching process of silicon [1]. The source and drain electrodes are non-coplanar, and the configuration of the component is a multi-paralleled channel structure with a common drain at the bottom of the chip [2] (Fig. 1). The short conducting channels are defined by double-diffusion technology and the drain is an epitaxial N^--N^+ configuration for increasing the voltage handling capability, by avoiding the Punch-Through phenomenon, at saturation range. These devices are particularly well adapted for linear amplification in low and high frequency ranges.

2. **Ohmic range.** — In a MOS transistor the current flowing through a cross-section of the channel is described by the classical relationship

$$I_D = Z\mu_{eff}\, qN \frac{d\Theta}{dy} \qquad (1)$$

where μ_{eff} is the effective mobility of the carriers, qN the total charge in the inversion layer at the abscissa y, Z the channel width and Θ the quasi Fermi level-potential difference within the surface space-charge region. The charge qN is generally evaluated by the Poisson-equation integration in the semiconductor, associated with the continuity condition of the normal electrical induction at the Si-SiO₂ interface. In the case of V.MOS the effects of the non uniformity of the doping in the P-region is introduced by an expo-
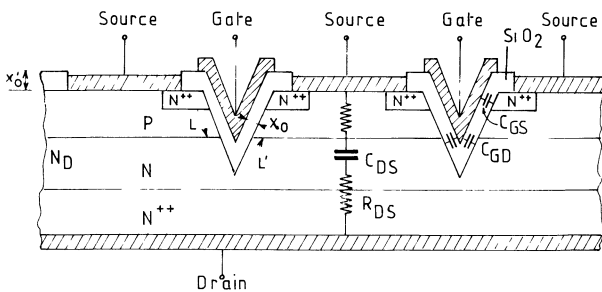
nential relationship between doping and source-drain coordinates [3] :

$$N_a(y) = N_S \cdot \exp\left[\frac{y}{L} \cdot \text{Log}\left(\frac{N_D}{N_S}\right)\right] \qquad (2)$$

L is the channel length, N_D and N_S the doping at the drain and source edges. On the other hand, the effects of the mobility reduction under longitudinal (E_y) and transversal (E_x) electrical fields must be introduced under the form [4] :

$$\mu_{eff} = \frac{\mu_0}{(1 + |E_y|/E_0)(1 + x_0|E_x|/\psi)} \cdot \qquad (3)$$

The self-heating effect under DC conditions is includ-

ed by (i) determining the crystal temperature using the thermal resistance concept :

$$T_c - T_a = (R_{th} + R_r) \cdot V_D I_D \qquad (4)$$

where T_c is the crystal temperature, T_a the ambient temperature, $V_D.I_D$ the dissipated power, R_{th} the chip-can thermal resistance and R_r the can-heat sink-ambient-thermal resistance and (ii) by taking into account thermal variations of the parameters governing the evolution of current. For example the low field mobility μ_0 follows :

$$\mu_0(T_c) = \mu_0(T_a) \cdot \left(\frac{T_c}{T_a}\right)^{-1.5} \cdot \qquad (5)$$

The current can be computed by the integration of the differential equation :

$$I_D = \frac{Z \cdot C_{0x} \cdot \mu_0(T_a)}{L(1 + V_D/LE_0)} \cdot \left[\frac{T_a + (R_{th} + R_r) V_D \cdot I_D}{T_a}\right]^{-1.5} \times$$

$$\times \int_0^{V_D} \frac{\psi[V_G' - \Theta - 2\,\varphi_F - (2\,q \cdot N_a(y) \cdot \varepsilon_{si} \cdot \varepsilon_0/C_{0x}^2)^{1/2} \cdot (\Theta + 2\,\varphi_F)^{1/2}]}{\psi + V_G' - \Theta - 2\,\varphi_F} \cdot d\Theta \qquad (6)$$

where V_G' is the *effective* gate voltage, φ_F the Fermi potential of the P region, C_{0x} the gate-oxide capacitance per unit area, V_D the drain voltage (Fig. 2). It can be deduced that (i) the threshold voltage V_T is mainly determined by the peak channel doping [10], (ii) the ON channel resistance is an hyperbolic function of the gate voltage (iii) the drain current presents a negative thermal coefficient.
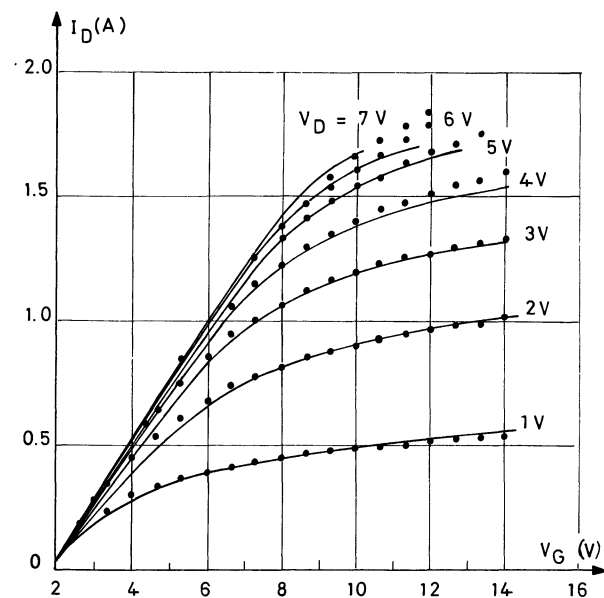

FIG. 2. — Drain current as a function of the gate voltage with drain voltage as parameter. DC conditions —— experimental values. ● Theoretical values ($R_{th} + R_r = 6$ °C/W).

3. **Saturation range.** — When the devices are biased in saturation range ($V_D > V_G - V_T$) we can neglect the channel shortening effect : the P-N$^-$ configuration of the channel-drain transition implies that the drain space-charge develops in the N$^-$-drain [5] (in classical MOST this extension occurs in the P region). In consequence, therefore the perfect saturation hypo-

thesis $\left(\dfrac{\partial I_D}{\partial V_D} \to 0\right)$ can be retained. In this regime the fundamental properties of the V.MOS are : (i) the current value is independent of the N$^-$-region configuration and properties, (ii) the transfer characteristic $I_D(V_G)$ becomes linear when the current reaches a critical value I_{DL} ; this second property must be correlated to the short channel length.

To explain the device behaviour we can, as first approximation : (i) neglect the thermal effects (pulsed mode), (ii) consider a uniformly doped P-region.

The transfer characteristic is approximated by the two relations :

$$I_D|_{V_G \to V_T} \simeq \mu_0 \frac{Z}{L} C_{0x} \frac{(V_G - V_T)^2}{2} \times$$

$$\times \frac{1}{1 + (V_G - V_T)/LE_0} \qquad (7)$$

$$I_D|_{V_G > LE_0} \simeq Z \cdot C_{0x} \cdot v_{sat} \frac{V_G - V_T}{2} \qquad (8)$$

where v_{sat} is the scattering limit velocity ($v_{sat} = \mu_0 \cdot E_0$). The second expression shows that in the linear drain

current-gate voltage region (Fig. 3), the current is independent of the length of the channel. In consequence the transconductance gm presents firstly an increasing part-with an initial slope equal to $\mu_0 \cdot \dfrac{Z}{L} \cdot C_{ox}$-and secondly a horizontal part-equal to $Z.C_{ox}.v_{sat}/2$, [6].
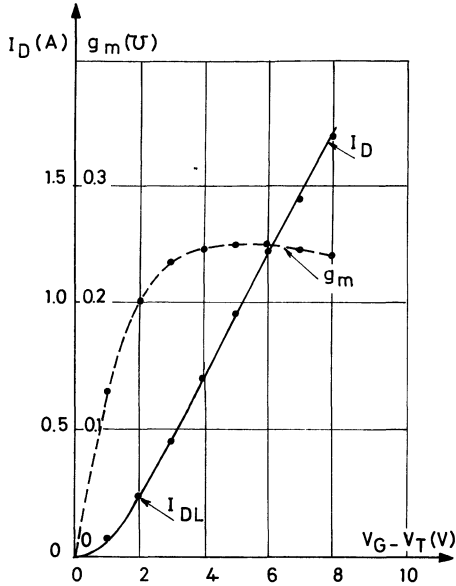

FIG. 3. — Drain current and transconductance as a function of the gate voltage (pulsed conditions) —— experimental values. ● Theoretical values.

4. Small signal HF analysis.

— The various steps of this analysis are as follows : (i) study of the dynamic properties in the active P region (channel), (ii) identification of the stray elements to establish the equivalent quadripole, (iii) comparison between theory and experiments, (iv) study of the power gain, which has been chosen as the figure of merit of the component.

4.1 ACTIVE CHANNEL BEHAVIOUR. — The following assumptions are made : (i) we neglect the Fermi potential and the bulk potential (2 $q.N_A.\varepsilon_{si}.\varepsilon_0/C_{ox}^2$) in view of the DC voltages applied to the electrodes (ii) the carrier mobility depends on the transversal and longitudinal components of the electrical field, (iii) linearization assumptions enable us to introduce $i(y, w)$ and $\varepsilon(y, w)$, i.e. the variations of current flowing and of the gate-channel voltage value in a section y, at pulsation w, (iv) thermal effect is not taken into account.

The active channel region is treated as a non-uniform transmission line. The first differential dynamic equation is obtained by linearising the current expression in a dynamic state and the second expresses the conservation of the current flow when the current-losses through the gate

$$\frac{\partial^2 i(y, w)}{\partial V_0(y)^2} - jw' \left[\frac{V_0(y)/V_G'^3}{1 + V_0(y)/\psi} \right] \cdot i(y, w) = 0 \quad (9)$$

$$\varepsilon(y, w) = \frac{1}{jw'} \frac{V_G'^3}{I_D . \psi} \times$$

$$\times \left[\frac{V_0(y)}{\psi + V_0(y)} - \frac{I_D}{\mu_0 ZC_{ox} \psi E_0} \right]^{-1} \frac{\partial i(y, w)}{\partial V_0(y)} \quad (10)$$

with

$$w' = w \left[\frac{\mu_0 (ZC_{ox})^2 V_G'^3}{I_D^2} \right] \quad (11)$$

and

$$V_0(y) = V_G' - \Theta(y) \quad (12)$$

For VHF and UHF ranges the solutions are obtained by using series expansion or asymptotic-function approximation. Using the current conservation law the variable gate current can be determined, and, by boundary conditions at the beginning and end of the channel the Y_{21} and Y_{11} admittance-factors in saturation range are calculated (for calculation methods see ref. [7]). These admittances are directly dependent of the following quantities : $\mu_0 \cdot \dfrac{Z}{L} \cdot C_{ox}$, LE_0, ZLC_{ox}, ψ and V_T, V_G.

4.2 EQUIVALENT CIRCUIT. — The V.MOS involves some stray elements due to the geometrical configuration and the technological process (Fig. 1). These
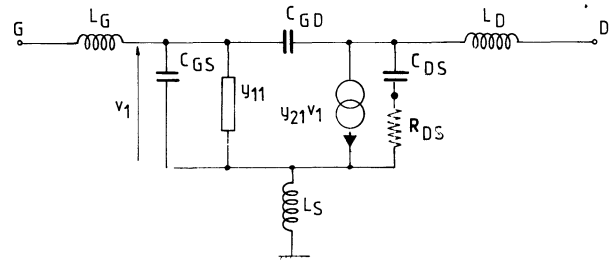

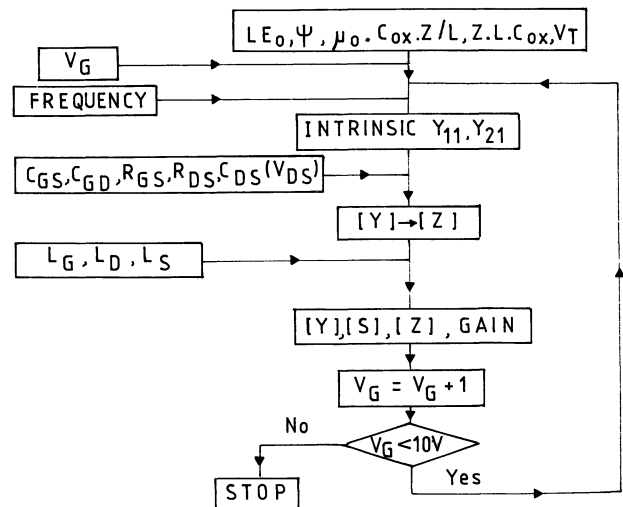FIG. 4. — Equivalent circuit used in this analysis (DC output conductance is not represented).

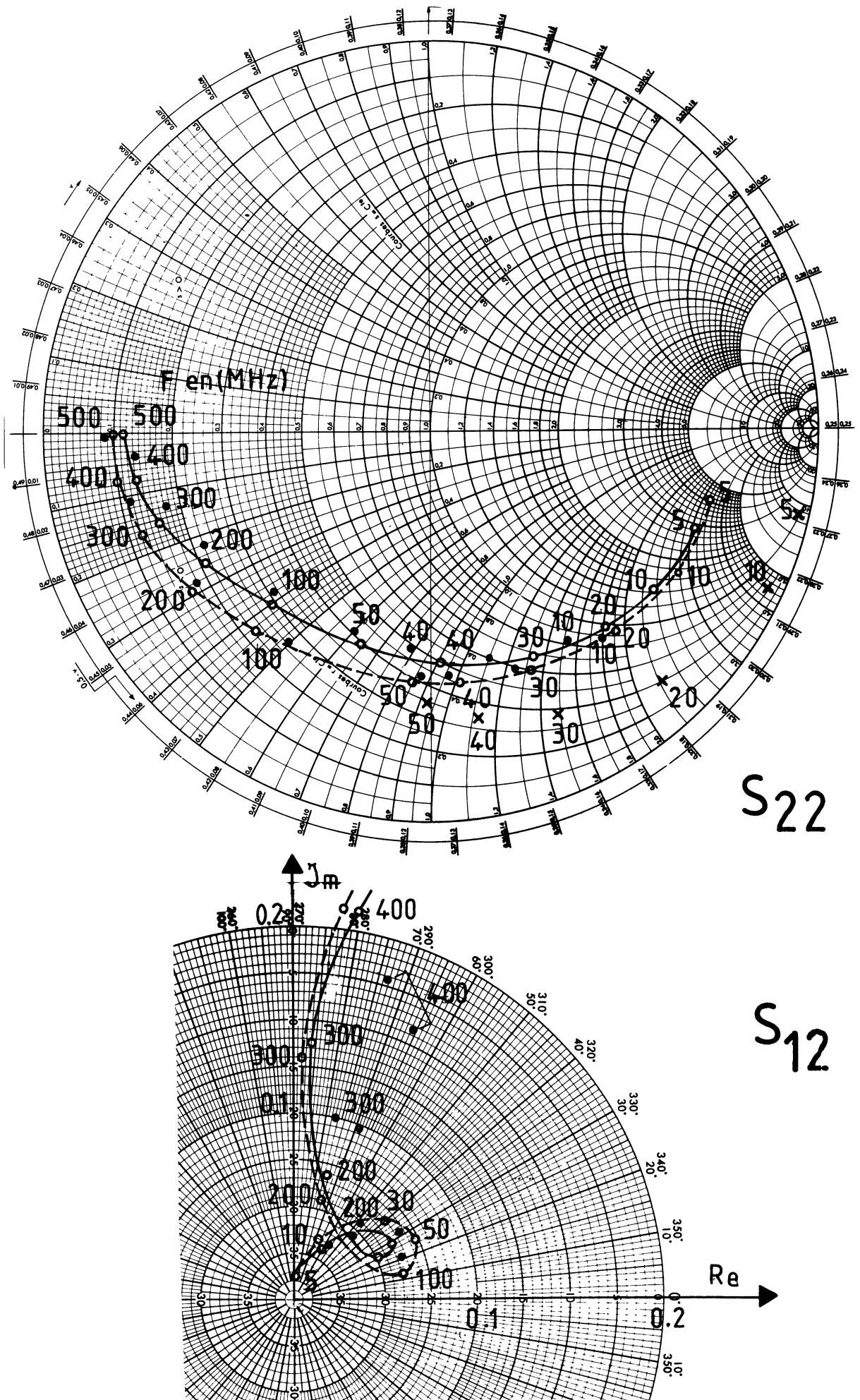FIG. 5. — Computing method for dynamic parameters determination.

FIG. 6. — Variations of the S_{ij} parameters as a function of the frequency ($V_D = 10$ V) (—O— theoretical values, high level $I_D > I_{DL}$; - - -O- - - theoretical values, $I_D = 100$ mA ; x theoretical values neglecting the saturation resistance effects (S_{22}); ● experimental values).

elements are : C_{gd} drain-overlap capacitance, C_{GS} source-overlap capacitance, C_{DS} transition-capacitance of the drain diode, R_{DS} resistance of the N⁻ region, LG, LD, LS access inductances. From the intrinsic factors y_{ij} and from the stray elements, we get the overall equivalent circuit shown in figure 4.

4.3 THEORY-EXPERIMENT COMPARISONS. — A numerical program enables us to compute (Fig. 5) : (i) the drain current, (ii) the intrinsic y_{ij} factors, (iii) the overall S_{ij} parameters. In order to check the validity of the model the scattering S_{ij} parameters were measured and computed. The input data have been determined as follows :

Element	Determined by	Value
$\mu_0 \cdot \dfrac{Z}{L} \cdot C_{0x}$	Low level output conductance	0.20 A/V²
ZLC_{0x}	Junction depth (L) or input capacitance measurements	30 pF $< ZLC_{0x} < 40$ pF
LE_0	Transconductance variations in saturation	5.0 V
ψ	Low level output conductance	10.0 V
V_T	Current in ohmic range	1.1 V
C_{GD}	Calculated or deduced of Im (y_{12}) [8]	5 pF $< C_{GD} < 6$ pF
C_{DS}	Calculated or deduced of Im (y_{22}) [8] at $V_D = 0 \rightarrow C_{DS} = \alpha$	105 pF $< \alpha < 115$ pF
R_{DS}, C_{GS}	Calculated (doping, geometry...)	$R_{DS} = 2\,\Omega$, $C_{GS} = 4$ pF
L_S, L_G, L_D	Calculated (bonding wire)	$L_G = L_S = 2$ nH ; $L_D \simeq 0$ nH

The calculated values are obtained by classical relationships including the area, length, doping, thickness or drain-voltage effects. From the comparisons between the experimental results (Fig. 6) and the computed parameters, it appears : (i) in VHF range the model simulates with a good accuracy the experimental characteristics (ii) in HF range, the observed discrepancies (S_{22}) must be attributed to the saturation-resistance (channel shortening) effects. From a general point of view it must be noticed that (i) for gate bias voltage higher than the critical value ($V_G > LE_0$), all parameters (S_{ij}, Y_{ij}, MUG) are independent of the gate voltage (ii) the power gain-transition frequencies ($MUG = 0$ dB) are very low, located in the range 500-800 MHz (Fig. 7, curves 1, 2).

This last property must be attributed to the parasitic element (drain-capacitance C_{DS} associated with the N⁻ region-R_{DS} resistance) shunting the output-drain, source-electrodes. An evaluation of the limit of the performances by using an optimal configuration of the drain diode (including voltage handling capability from reference [9]) shows that the theoretical-frequential limit for this kind of device can not be higher than 2 GHz (Fig. 7, curves 3, 4).

5. **Conclusion.** — The above methods are for establishing the models of V-MOS transistor. The essential differences from classical MOST are associated with the saturation of the scattering velocity : linearity of the transfer characteristic, dynamic parameters independent of the gate voltage. The intrinsic properties linked to the short channel effects are highly affected by the drain diode configuration and the evaluation of the useful range for optimized struc-
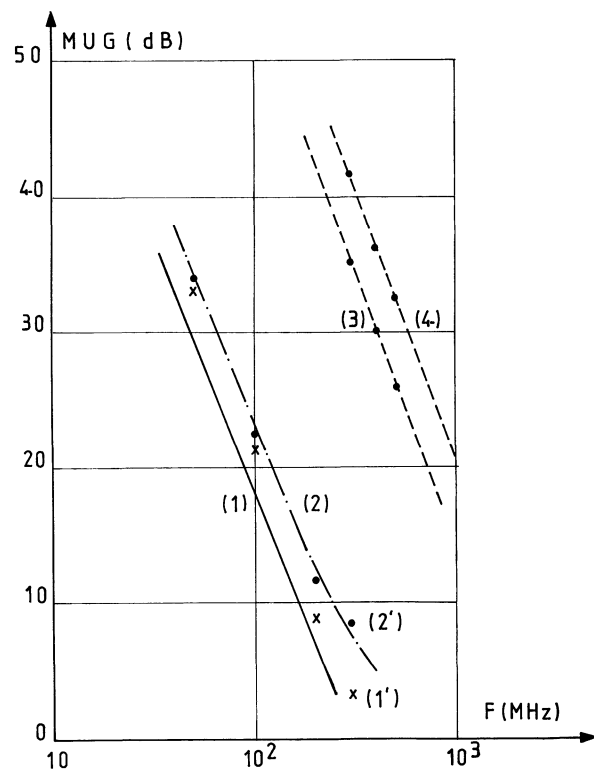

FIG. 7. — Maximum unilateral gain as a function of the frequency : —— (1) theoretical values, low level ($I_D = 100$ mA) ; —.—.—.— (2) theoretical values, high level ; x (1'), ● (2') experimental value ; - - ● - (3) and - - ● - (4) theoretical-limit value (low and high level).

ture will be restricted to UHF. It must be noted that these models have been used for a CAD of broadband linear amplifiers (1 MHz-150 MHz).

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