CMOS 1 MICRON ISOLATION TECHNOLOGY USING INTERFACE SEALING BY PLASMA NITRIDATION : PLASMA SILO

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P. DELPECH, B. VUILLERMOZ, M. BERENGUER, A.STRABONI and T. TERNISIEN

CNET Centre National d'Etudes des Télécommunications, Chemin du Vieux Chêne, BP 98, F-38243 Meylan Cedex, France

RESUME - Nous avons évalué l'apport de la technique d'isolation par SILO PLASMA dans une filière CMOS 1 µm par comparaison à un isolement par LOCOS classique. Le SILO PLASMA permet de réduire de 0.4 µm les pertes liées au LOCOS, ainsi que l'effet de canal étroit, tout en conservant les principales caractéristiques électriques de cette technique (courant sous le seuil, intégrité de l'oxyde grille, etc,)

ABSTRACT - The improvement of a 1 µm CMOS process using PLASMA SILO as an isolation technique has been evaluated by comparison with a classical LOCOS. The PLASMA SILO provides a reduction of 0.4 µm in the channel width loss, and a gain on the narrow channel effect. The other electrical characteristics are maintained (subthreshold characteristics, gate oxide integrity, etc,)

INTRODUCTION

For submicron design rules, new approaches have to be proposed for better control of lateral isolation. In order to avoid LOCOS limitations (i.e. Bird's Beak and lateral diffusion of channel stop implant) SILO has already been proposed [1]. In this paper we report an evaluation of the PLASMA SILO technique in a 1 micron CMOS process. This isolation technique uses a plasma sealed interface with few modifications in the standard LOCOS procedure; this constitutes a significant advantage for a rapid introduction into an industrial technology.

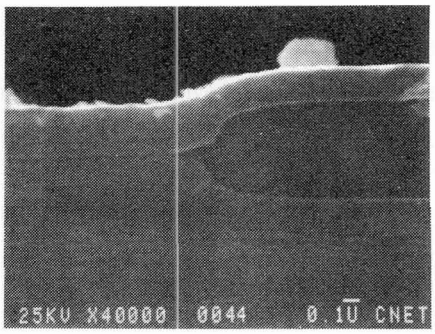
Application of plasma nitridation to the SILO [2] presents the main advantage to realise a very effective and reproducible barrier against lateral oxidation, by avoiding native oxide present between Silicon and deposited Si_3N_4. In addition, it is possible with this technique to grow the field oxide at a lower temperature, which reduces the dopant diffusion while keeping a short Bird's Beak value.

EXPERIMENTAL PROCEDURE

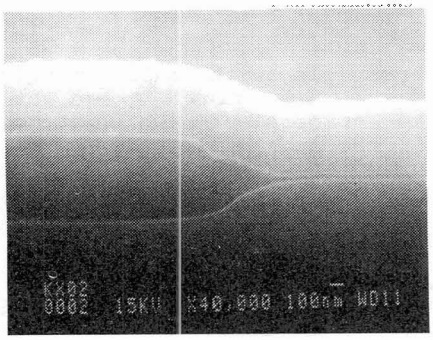
The sealing nitridation is achieved in a 13.56 MHz plasma with external capacitive coupling. The set up allows batch treatment and is now available as a production machine [3]. 4 to 5 nm thick Silicon Nitride is grown at 950°C in an ammonia flow at a pressure of 3.E-2 mBar(hPa) during 6 hours with a power of 800 W. These very thin layers were able to resist the severe oxidizing conditions (steam at 980°C) used to grow a 400 nm oxide on bare (100) Silicon. In the SILO process, the standard pad oxide (25 nm) / Si_3N_4 (90 nm) LOCOS mask is used over the sealing film, except that the thermal pad oxide is replaced by an LPCVD oxide.

RESULTS AND DISCUSSION

The Figure 1 shows the morphology of the resulting field oxides (700 nm) after steam oxidation at 980°C for the PLASMA SILO (a) and at 1050°C (reduced Bird's Beak) for the conventionnel LOCOS (b). The bird's beak length to oxide thickness ratio (L_{BB} / Tox) is 0.45 for the former as compared to 0.70 for the latter, as measured before mask removing.



a) PLASMA SILO BEFORE MASK REMOVING



b) STANDARD LOCOS AFTER MASK REMOVING

FIG. 1. SEM MICROGRAPHS OF BIRD'S BEAK EXTENSION

We have compared electrical characteristics of devices fabricated with both PLASMA SILO and optimised LOCOS (Field oxide LOCOS: 700 nm).
The main result is the reduction in the loss of channel width DELTAW = W_{mask} - W_{eff} by 0.4 µm, from 1.1 for optimised LOCOS to 0.7 µm for PLASMA SILO, with slight variation between N and P type (channel stop implanted NMOS side only).
The narrow channel effect is substantially reduced as seen in Fig 2, mainly due to the decrease in DELTAW. Thus, a transistor with a 0.5 µm effective width (1.2 µm designed width) is well controlled.

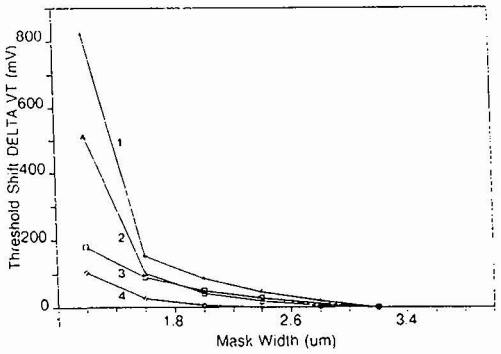


FIG. 2. NARROW CHANNEL EFFECT COMPARISON SILO/LOCOS
SILO PMOS (1) SILO NMOS (2)
LOCOS PMOS (3) LOCOS NMOS (4)

A statistical analysis performed over 400 devices, shows (Figure 3) that the narrow channel effect is very weak, even for an effective width as low as 0.2 µm.

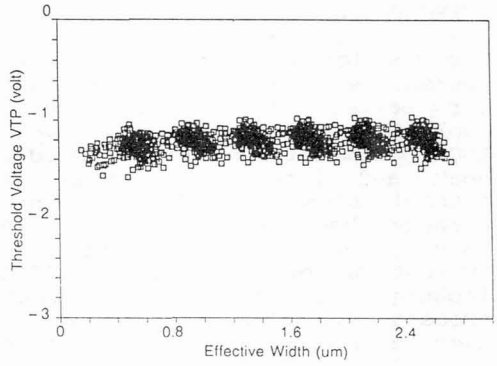


FIG. 3. NARROW CHANNEL EFFECT SILO PMOS

The subthreshold characteristics as measured on P-channel transistors , with L=1.6 µm and W between 3.2 and 1.2 µm are shown in Figure 4 for SILO and LOCOS respectively at Vd=-7 Volt. These curves show similar characteristics and in particular, no additional leakage current for the SILO process. The same behaviour is found for N-channel transistors.

Moreover, no kink appears showing the absence of parasitic sidewall transistors.

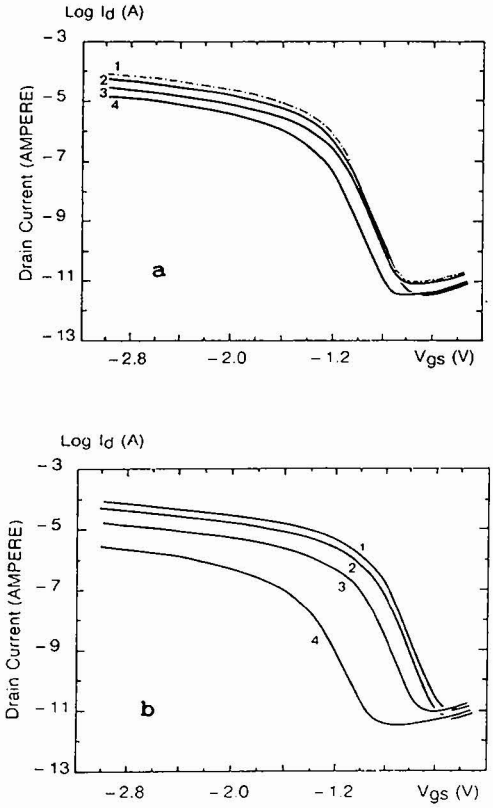


FIG. 4. SUBTHRESHOLD CHARACTERISTICS OF PMOS TRANSISTORS a) SILO b) LOCOS, VD=-7 VOLT L=1.6 µM, W=3.2 µM (CURVE 1), W=2.4 µM (CURVE 2), W=1.6 µM (CURVE 3), W=1.2 µM (CURVE 4)

Junction leakage measurements were performed on diodes which exhibit different area(A)/perimeter(P) ratios : finger-type diodes with A=2.6E-4 cm^2 and P=1.7 cm, and rectangular-type diodes with A=6.8E-4 cm^2 and P=0.1 cm. The values of the perimeter leakage current at ± 5 V are reported in Table I. For the SILO process, an insignificant increase in the leakage value can be noticed.

TABLE I. PERIMETER LEAKAGE CURRENT I_R AT ±5 V FOR SILO AND LOCOS PROCESSES AND THE TWO TYPES OF DIODES N+/P AND P+/N

ISOLATION PROCESS	I_R (pA/cm) N+/P	P+/N
SILO	21.4	18.8
LOCOS	16.2	16.3

SEM observations on SIRTL etched samples oxidized at 980°C confirm the absence of crystalline defects at the boarder of the devices. This was, however, not the case on samples oxidized at 920°C, i.e.below the viscous flow transition temperature.
The SILO technique allows the same field threshold voltage $|V_{TF}|$ as the LOCOS, for N and P type, from 17 V for a 2.4 µm isolation spacing to 13 V for 1.2 µm spacing. The Id(Vg) characteristics of a field transistor are shown in Fig.5 for Vd=1 et 5 V. The leakage current is less than 1 pA/µm for both types of field transistors.

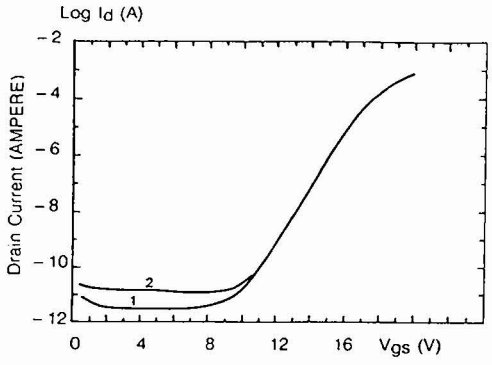


FIG. 5. SUBTHRESHOLD CHARACTERISTICS OF A NMOS FIELD TRANSISTOR VD=1 V (1) AND 5 V (2)(W=1000,L=2 µM)

The effect of PLASMA SILO on the thin oxide gate integrity (25 nm) has been evaluated on capacitors with polycide gate. The defect density is not affected by such a technology, indicating that the mask has been efficiently removed.

CONCLUSION

We have presented an evaluation of the PLASMA SILO isolation which provides a significant gain in both the width loss and the narrow channel effect by comparison with the classical LOCOS, while the main electrical characteristics are preserved. Due to its simplicity (no additional masking level) this technology seems promising for submicrometer processes .

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[2] B.Vuillermoz, A.Straboni, R.Pantel, E.C.S. Meet., Toronto, Abstract 248, 1985
[3] French patent N° 83 18299