



**HAL**  
open science

## Fully Digital Test Solution for a Set of ADCs and DACs embedded in a SiP or SoC

Vincent Kerzérho, Philippe Cauvet, Serge Bernard, Florence Azaïs, Mariane Comte, Michel Renovell

► **To cite this version:**

Vincent Kerzérho, Philippe Cauvet, Serge Bernard, Florence Azaïs, Mariane Comte, et al.. Fully Digital Test Solution for a Set of ADCs and DACs embedded in a SiP or SoC. IET Computers & Digital Techniques, 2007, 1 (3), pp.146-153. 10.1049/iet-cdt:20060136 . lirmm-00195172

**HAL Id: lirmm-00195172**

**<https://hal-lirmm.ccsd.cnrs.fr/lirmm-00195172>**

Submitted on 10 Dec 2007

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Fully Digital Test Solution for a set of ADC's and DAC's embedded in a SiP or SoC

V. Kerzérho<sup>1,2</sup>, P. Cauvet<sup>2</sup>, S. Bernard<sup>1</sup>, F. Azais<sup>1</sup>, M. Comte<sup>1</sup> and M. Renovell<sup>1</sup>

<sup>1</sup>LIRMM, University of Montpellier / CNRS – 161 rue Ada, Montpellier, 34392 France

<sup>2</sup>Philips France Semiconducteurs, 2 Rue de la Girafe B.P. 5120, Caen Cedex 5, 14079 France  
{vincent.kerzerho, philippe.cauvet}@philips.com ; {bernard, azais, comte, renovell}@lirmm.fr

## Abstract

The trend towards highly integrated electronic devices leads to the growth of the System-in-Package (SiP) and System-on-Chip (SoC) technologies, where data converters play a major role in the interface between the real analogue world and the digital processing. Testing these converters with accuracy and at a low cost represents a big challenge, because the observability and controllability of these blocks is reduced and the test operation requires a lot of time and expensive analogue instruments. The purpose of this paper is to present a new Design-for-Test (DFT) technique called “Analogue Network of Converters”. This technique aims at testing a set of Analogue-to-Digital Converters (ADC) and Digital-to-Analogue Converters (DAC) in a fully digital setup (using a low cost digital tester). The proposed method relies on a novel processing of the harmonic distortion generated by the converters and requires an extremely simple additional circuitry and interconnects.

## 1. Introduction

The market pressure for data and telecommunication applications is now driving the need for integrating very different analogue or mixed-signal blocks into a single System-in-Package (SiP) or System-on-Chip (SoC). Figure 1 gives a picture of such a complex mixed-signal system integrated into a single package. The integration of many different functions into a single package offers several clear benefits, but also implies very significant test challenges. As an illustration of these difficulties, examples are usually reported where the test of the analogue blocks in the system may represent up to 90% of the whole test effort while these analogue blocks only represent 10% of the whole chip area.

When testing analogue blocks, the main difficulty comes from the performance requirements of the test instruments. Indeed, analogue testing is made of a long sequence of parameter characterization that is performed using very expensive instruments able to accurately measure analogue signals. In addition to these required expensive instruments, we should note that controllability and observability of deeply embedded analogue blocks are much reduced and the possibility of external testing may be limited. Also, as signals become faster and systems are operated at higher speeds, external testing becomes more susceptible to disturbances such as noise, crosstalk, etc.).

To overcome these problems, several authors have proposed different BIST techniques where signals are internally generated and/or analysed [1-7]. Another possible and less expensive solution consists in using DFT techniques to internally transform the analogue signals into digital ones that are made controllable and observable from the chip I/Os [3,8,9]. As a result, only digital signals are externally handled by cheap “digital” test equipment (Low Cost Tester).

In current systems, it is to mention that converters (ADC's and DAC's) are the main components of any mixed-signal chip. Nowadays, many ADC's and DAC's may be implemented in a complex SoC or SiP. For instance, Figure 1 proposes a microphotography of the PNX8327 device for set-top box applications where 2 ADC's and 7 DAC's are embedded on the same SiP [10]. Testing this whole set of converters is a very complex task requiring a long test time because of the above mentioned problems of accessibility, signal integrity, accuracy of converter parameter measurements.

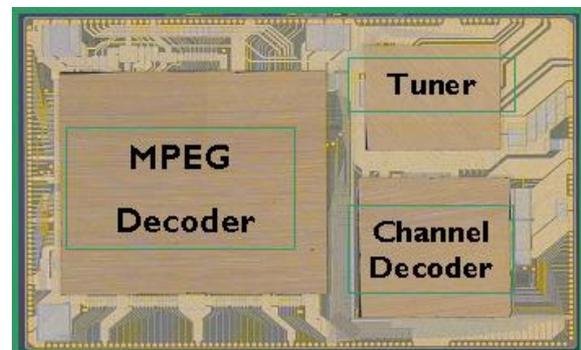


Figure 1: SiP for set-top box applications

In this context, an original DFT technique called “Analogue Network of Converters” (ANC) is proposed to test the whole set of embedded ADC's and DAC's. An extremely small circuitry is required to apply a fully digital test approach to the System-in-Package/System-on-Chip.

Following a brief reminder of the basic test techniques for converters, section 2 introduces the fundamental principle of the ANC technique, and the first step of the method. In section 3, the test of the set of  $n$  DAC's and  $m$  ADC's is made equivalent to a system of equations where the converter characteristics are the unknowns. An example of generalization of the method and an estimation of the test time reduction are shown in section 4. In section 5, the proposed ANC technique is validated through simulations and measurements. Finally, section 6 gives some

concluding remarks, and a summary of the expected further works.

## 2. ANC Fundamental Principle

As often mentioned, analogue testing is classically oriented to performance characterization of a function under test. Performance characterization is obtained through a number of static and dynamic parameter estimations.

### 2.1. ADC and DAC testing

Real-life converters are affected by errors, usually classified in two types [9][11][12]:

- Stochastic errors: noise, aperture uncertainty (jitter), and coupling between analogue and digital part.
- Deterministic errors: non-linearities, distortion.

Several parameters are defined in order to characterize and test ADC's and DAC's. Various methods are now used to accurately test the signal-to-noise ratio in a noisy environment, but distortion remains a domain where only a limited number of advanced solutions have been proposed so far. A crucial deterministic parameter is the Integral Non Linearity (INL). For most of the application domains, two of the key dynamic parameters are:

- Total Harmonic Distortion (THD),
- Spurious Free Dynamic Range (SFDR),

The above set of dynamic parameters is derived [13] or computed [9] from the harmonic values appearing in the spectrum of the output signal.

A very common way to estimate the dynamic parameters of a given converter relies on spectral analysis, i.e. to apply a 1-tone sine wave signal to the converter input and compute the FFT of the output signal. The obtained harmonic values are then used to compute the dynamic parameters. Figure 2 shows a typical spectrum of a 12bits ADC driven by a sine wave at frequency  $F_0=4.43\text{MHz}$

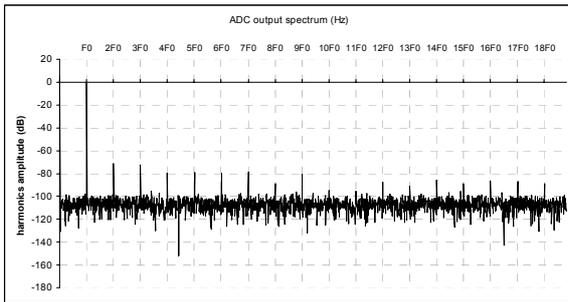


Figure 2: Spectrum of a converter output signal

The fundamental bin is at frequency  $F_0$ , the frequency of the input sine wave. All the values of the spectrum are normalized to this fundamental one. The converter errors induce harmonic frequencies, which enter in the computation of the converter parameters. Note that even non-linearities may be derived from these harmonic values as demonstrated in [13,14].

Considering for instance the test of a single ADC using efficient instruments, it has been demonstrated

[13] that the output signal can be represented by (1). This equation includes an ideal sampled sine wave  $x(n)$  and the sum of all the harmonic values introduced by the converter errors.

$$s(n) = x(n) + \sum_{k \geq 0} H_k^{\text{converter}} \cos(k(\theta_n + \theta_0)) \quad (1)$$

In equation (1),  $n$  is the sample index,  $\theta_0$  the initial phase shift and  $H_k^{\text{converter}}$  the amplitude of the  $k^{\text{th}}$  harmonic and  $\theta_n$  is the nominal sampling phase

$$\theta_n = 2\pi \left( \frac{P}{M} \right) n \quad (2)$$

Given the above comments, it clearly appears that accurate measurement of the set of harmonic values  $H_k^{\text{converter}}$  of the output signal is a crucial point for any converter testing technique. The above equation may also apply to the test of a single DAC, because the analogue output signal is converted into a digital sample set in the commonly used testers.

### 2.2. Analogue Network of Converters

Considering a complex system with several ADC's and DAC's, the objective of this paper is to measure the harmonic values  $H_k^{\text{converter}}$  of each converter output signal using a fully digital way. To be fully digital from an outside chip perspective, a very simple circuitry is added to the system:

- to realize the analogue sum of any combination of DAC outputs,
- to connect the resulting sum to any combination of ADC inputs.

This ANC is presented by figure 3. A simple OPAMP-based analogue adder can be used to implement the proposed DFT. The multiplexer control signal  $I_i$  ensures the connection of the corresponding DAC $_i$ . In the same way, the multiplexer control signal  $O_j$  connects the corresponding ADC $_j$ .

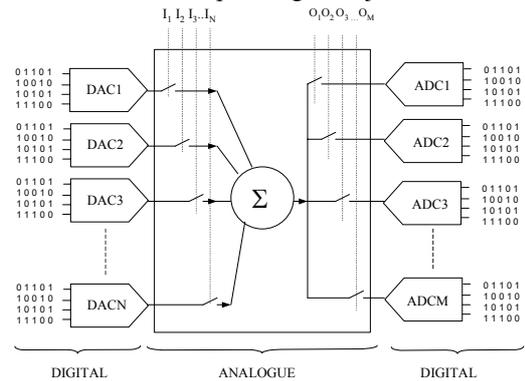


Figure 3: The ANC DFT technique

We define  $C(n,m)$  as the configuration where  $n$  DAC's and  $m$  ADC's are connected. Using configuration  $C(1,1)$ , the spectrum of the output signal can be computed and we can extract the values of the harmonics  $H_k^{C(1,1)}$ . But in this case, the output signal includes the errors of DAC1 and the errors of ADC1. In other words, the spectrum includes the harmonic contribution of DAC1 and the harmonic contribution of

ADC1. So, thanks to the linearity of the system, we can write the following equation:

$$\sum H_k^{\text{measure}} = \sum H_k^m = \sum (H_k^{\text{DAC1}} + H_k^{\text{ADC1}}) \quad (3)$$

In this equation, we assume that the harmonic amplitudes created by the DAC are negligible with respect to the fundamental amplitude of the signal. Thus, we can consider the signal driving the ADC as a single tone signal. This working hypothesis will be verified in the validation phase described in section 4.

Thanks to equation (3), we obtain a relation between the harmonic contributions of the different converters. Indeed, the left member of equation (3) is made of known values, the spectral bins at the output of the ADC, whereas the right member represents the unknowns.

This example establishes the relationship between one configuration and its resulting equation, which leads to the fundamental idea of the ANC DFT technique. By using different configurations  $C(n,m)$ , we are able to obtain a set of different equations. So, with an adequate set of configurations (i.e; system of equations), we expect to be able to fully determine the set of unknowns, i.e. the individual harmonic contribution of each converter.

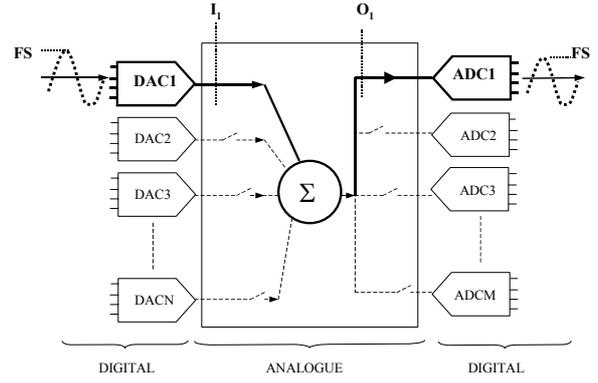
The ANC DFT technique creates a duality between the configurations and the equations giving the estimation of the harmonic contributions of each converter. The next section explores the space of possible configurations to obtain such a set of equations.

### 3. First step: applying ANC to a basic configuration

The ANC principle consists in using different converter interconnections. Adequate test configurations have to be found in order to discriminate the influence of each converter on the final response. In practice, the test parameters that can be easily controlled are only the phase and the amplitude of the digital stimulus. In this section, two configurations, using DAC1 DAC2 and ADC1, are studied in order to discriminate their harmonic contributions.

#### 3.1. Configuration C(1,1) at full scale

The first configuration considered is made up of a single DAC and a single ADC (Figure 4).



**Figure 4: C(1,1) test configuration**

According to the harmonic contribution model (3), the influence of the two data converters on the sampled signal can be expressed by:

$$s(n) = x(n) + \sum_{k \geq 0} (H_{\text{dac}k}^{\text{FS}} + H_{\text{adc}k}^{\text{FS}}) \cos(k(\theta_n + \theta_0)) \quad (4)$$

where  $H_{\text{dac}k}^{\text{FS}}$  and  $H_{\text{adc}k}^{\text{FS}}$  are respectively the  $k^{\text{th}}$  harmonic contribution of the DAC and the ADC for an input signal reaching the converter full scale. Notice that, in this study, we consider that all the converters have the same dynamic range.

If we only consider the three converters DAC1, DAC2 and ADC1, we generate two test setups. In a first step, a sine wave is sourced from DAC1 to ADC1, with amplitude covering the converter full-scale. The expression of  $H_k^{m,a}$ , the amplitude of the  $k^{\text{th}}$  harmonic measured on the ADC output is given by:

$$H_k^{m,a} = H_{\text{dac}k}^{\text{FS}} + H_{\text{adc}k}^{\text{FS}} \quad (5)$$

In the second step, the test path goes through DAC2 and ADC1. The amplitude of the test signal still reaches the full scale of the converters. Therefore, we obtain a second equation given by (6), where  $H_k^{m,b}$  is the amplitude of the  $k^{\text{th}}$  harmonic measured on the ADC output.

$$H_k^{m,b} = H_{\text{dac}2k}^{\text{FS}} + H_{\text{adc}k}^{\text{FS}} \quad (6)$$

At this point, we have three unknown parameters ( $H_{\text{dac}k}^{\text{FS}}, H_{\text{dac}2k}^{\text{FS}}, H_{\text{adc}k}^{\text{FS}}$ ) and only two equations (5 and 6) from two acquisitions.

One could think to play with the amplitude and phase of the input signal to establish new equations. Unfortunately, variations of these test setup parameters give no additional independent information to discriminate the influence of each converter on the final response. Indeed, the input signal phase has no influence on the converter harmonic contribution and even if the input signal amplitude  $A_{\text{in}}$  modifies the converter harmonic contribution ( $H_{\text{dac}k}^{A_{\text{in}}} \neq H_{\text{dac}k}^{\text{FS}}$  if  $A_{\text{in}} \neq \text{FS}$ ), each new acquisition would give a new equation but also two new unknown parameters ( $H_{\text{dac}k}^{A_{\text{in}}}, H_{\text{adc}k}^{A_{\text{in}}}$ ).

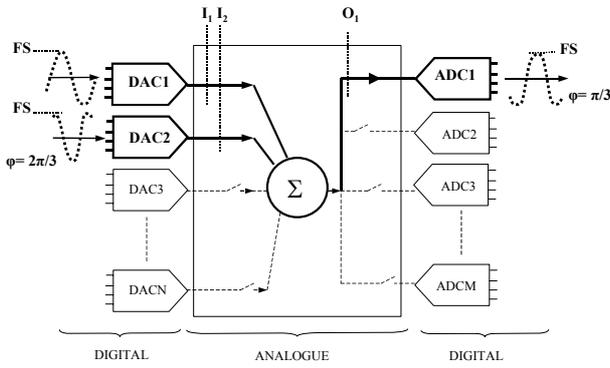
To avoid this problem, the two DAC's outputs are added to establish a new configuration. This new configuration is called C(2,1) and is described in the next section.

### 3.2. Configuration C(2,1) at full scale

The second hardware configuration is made up of two DAC's and one ADC. The input signal of the ADC is the sum of the two DAC output signals. A C(2,1) test configuration has already been described in [15]. But in this case, the objective is to test only the ADC, and DAC's must have higher resolution than the ADC.

Unfortunately, considering three converters with the same resolutions, the sum of two full-scale signals from DAC1 and DAC2 with no relative phase shift is twice the converter full scale and would saturate the ADC.

The solution to overcome this problem is to introduce a relative phase shift of  $2\pi/3$  between the two input signals (Figure 5)



**Figure 5: Test setup to obtain the third equation.**

The sum of the two DAC outputs is a full-scale signal; this property is mathematically explained by (7)

$$\cos\left(x + \frac{2\pi}{3}\right) + \cos(x) = 2 \cos\left(x + \frac{\pi}{3}\right) \cos\left(\frac{\pi}{3}\right) = \cos\left(x + \frac{\pi}{3}\right) \quad (7)$$

As a consequence we obtain (11), the third equation,

$$H_k^{m,c} = Hdac1_k^{FS} + Hdac2_k^{FS} \cos(k2\pi/3) + Hdad1_k^{FS} \cos(k\pi/3) \quad (8)$$

where  $H_k^{m,c}$  is the amplitude of the  $k^{\text{th}}$  harmonic measured on the ADC output. So finally, we obtain the following equation system for each  $k^{\text{th}}$  harmonic contribution:

$$\begin{cases} H_k^{m,a} = Hdac1_k^{FS} + Hdad1_k^{FS} \\ H_k^{m,b} = Hdac2_k^{FS} + Hdad1_k^{FS} \\ H_k^{m,c} = Hdac1_k^{FS} + Hdac2_k^{FS} \cos(k2\pi/3) + Hdad1_k^{FS} \cos(k\pi/3) \end{cases}$$

This system would enable the discrimination of the harmonic contribution of every converter if the three equations were independent. This condition is not verified for harmonic components that are of a prime order and greater than three. Indeed for these harmonics, the third equation is a linear combination of the two other equations.

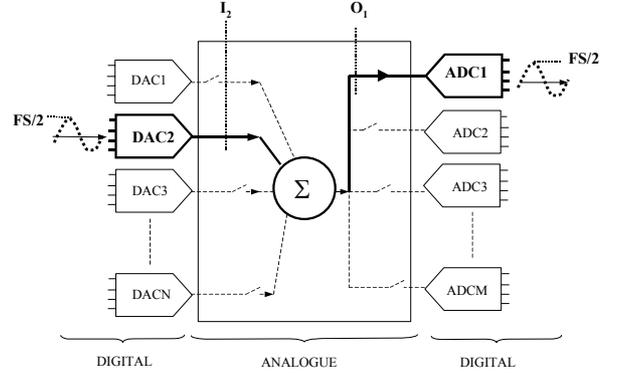
We have observed a similar limitation whatever the relative phase shift introduced between the two input signals. So, this 3-equation system permits to discriminate the 4 first harmonics, but is not sufficient to calculate the THD or the SFDR. To go further and discriminate more harmonics, it is necessary to vary the input signal amplitude, as subsequently described.

### 3.3. Configuration C(1,1) at 1/2 full scale

The second parameter we can control is the input signal amplitude. As previously explained, harmonic contribution depends on the stimulus amplitude ( $Hdac1_k^{A_{in}} \neq Hdac1_k^{FS}$  if  $A_{in} \neq FS$ ) and no trivial relationship exists between these different harmonic contributions. Consequently, the use of different amplitudes induces additional unknown parameters. Nevertheless, it also introduces new test setup possibilities that can be exploited to get additional independent useful information.

Practically, we have looked for a system of equations that allows the discrimination of the three converter harmonic contributions,  $Hdac1_k^{FS}$ ,  $Hdac2_k^{FS}$ ,  $Hdad1_k^{FS}$  using test stimuli with amplitude at full-scale and amplitude at 1/2 full-scale.

The new third equation is the result of a test at 1/2 full scale through DAC2 and ADC1, as illustrated in Figure 6.



**Figure 6: Test setup to obtain the third independent equation**

The measured harmonics are the sum of DAC2 and ADC1 harmonic contributions for an input signal at 1/2 full-scale.

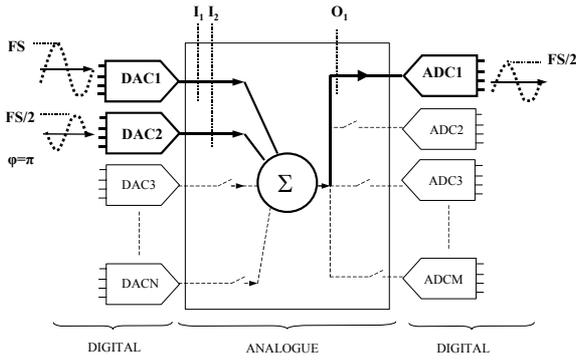
$$H_k^{m,c} = Hdac2_k^{FS/2} + Hdad1_k^{FS/2} \quad (9)$$

Thanks to this test, we add two new unknowns. In order to keep the same number of unknowns and increase the number of equations, it is possible to associate DAC1 at full-scale as described in the next section.

### 3.4. Configuration C(2,1) at 1/2 full scale

1/2 full-scaled input signal has introduced two unknown parameters,  $Hdac2_k^{FS/2}$  and  $Hdad1_k^{FS/2}$ . Three Independent equations have already been established, (5) (6) and (9), so we need two additional independent equations. C(2,1) configuration with both amplitude and phase variation, is used to establish these two equations. The 4<sup>th</sup> test setup involves a full-scale input signal on DAC1 and a 1/2 full-scale input signal on DAC2 with a  $\pi$  phase shift (Figure 7). The resulting signal at the ADC input is a sine wave at 1/2 full-scale:

$$\cos(x) + \frac{\cos(x + \pi)}{2} = \cos(x) - \frac{\cos(x)}{2} = \frac{\cos(x)}{2} \quad (10)$$



**Figure 7: Test setup to obtain the 4th independent equation**

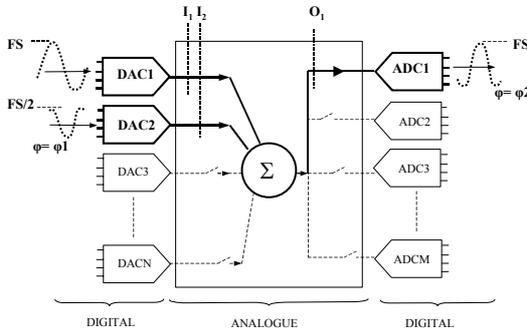
The resulting equation is the sum of the harmonic contribution at full-scale of DAC1, the harmonic contribution at  $\frac{1}{2}$  full scale of DAC2 balanced by the phase shift and the harmonic contribution at  $\frac{1}{2}$  full scale of ADC1.

$$H_k^{m,d} = Hdac1_k^{FS} + Hdac2_k^{FS/2} \cos(k\pi) + Hadc1_k^{FS/2} \quad (11)$$

The 5<sup>th</sup> and ultimately required test is very similar to the previous one (Figure 8). The input amplitudes are the same but they are relatively phase shifted of  $\varphi_1$ . The resulting signal at ADC input is now a sine wave at full-scale with a phase shift of  $\varphi_2$ .

$$\cos(x) + \frac{\cos(x + \varphi_1)}{2} = \cos(x + \varphi_2) \quad (12)$$

$$\text{with } \varphi_1 = \pi - 2\arccos\left(\frac{1}{4}\right), \varphi_2 = \pi - \arccos\left(\frac{1}{4}\right) \quad (13)$$



**Figure 8: Test setup to obtain the 5th independent equation**

The 5<sup>th</sup> equation then corresponds to the sum of the harmonic contributions balanced by their phase shift:

$$H_k^{m,e} = Hdac1_k^{FS} + Hdac2_k^{FS/2} \cos(k\varphi_1) + Hadc1_k^{FS} \cos(k\varphi_2) \quad (14)$$

In summary, the proposed test strategy is composed of five successive tests. Each test consists in an acquisition and a spectral analysis (with Fast Fourier Transform) to evaluate harmonic bins. We obtain a 5-equation system for each harmonic bin:

$$\begin{cases} H_k^{m,a} = Hdac1_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,b} = Hdac2_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,c} = Hdac2_k^{FS/2} + Hadc1_k^{FS/2} \\ H_k^{m,d} = Hdac1_k^{FS} + Hdac2_k^{FS/2} \cos(k\pi) + Hadc1_k^{FS/2} \\ H_k^{m,e} = Hdac1_k^{FS} + Hdac2_k^{FS/2} \cos(k\varphi_1) + Hadc1_k^{FS} \cos(k\varphi_2) \end{cases}$$

This system of independent equations is sufficient to calculate the value of the required harmonic contributions ( $Hdac1_k^{FS}, Hdac2_k^{FS}, Hadc1_k^{FS}$ ). It allows thus a fully independent characterization of the three converters of the C(2,1) configuration in terms of harmonic contributions.

#### 4. Second step: generalization of the method and test time reduction

The first step consists in using C(2,1) and C(1,1) configurations to characterize the three first converters (DAC1, DAC2 and ADC1). Five consecutive tests are necessary in order to characterize these three converters.

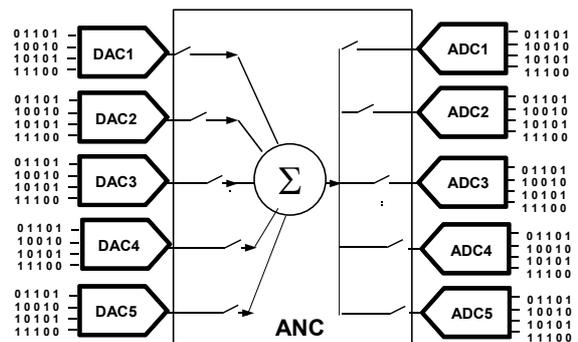
The generalization of the method is based on two ideas.

At first, by using an already characterized converter, we can characterize an additional one with only one test. For instance, DAC1 can be used to characterize the harmonic contribution of an uncharacterized ADCi using one digital stimulus at full-scale to obtain the following additional equations:

$$H_k^{m,j} = Hdac1_k^{FS} + Hadc_i^{FS} \quad (15)$$

The second idea is to do some parallel tests, during the first step in order to anticipate the measurements that would permit to apply the first idea. Indeed the first step needs five consecutive tests using C(1,1) and C(2,1) configurations, during a C(1,1) test, there is a DAC which is not used. Consequently, this DAC may be used to achieve the test described by equation 15. The results of this test will help characterize the unknown ADCi once the first step will be finished and DAC1 characterized. The parallel testing is possible, because only digital tester channels are required.

For instance, let's consider the ANC presented by figure 9. This is a set of 5 DAC's and 5 ADC's interconnected. The network of interconnections would be defined, considering the tests that should be done.



**Figure 9: ANC made of 5 DAC's and 5 ADC's**

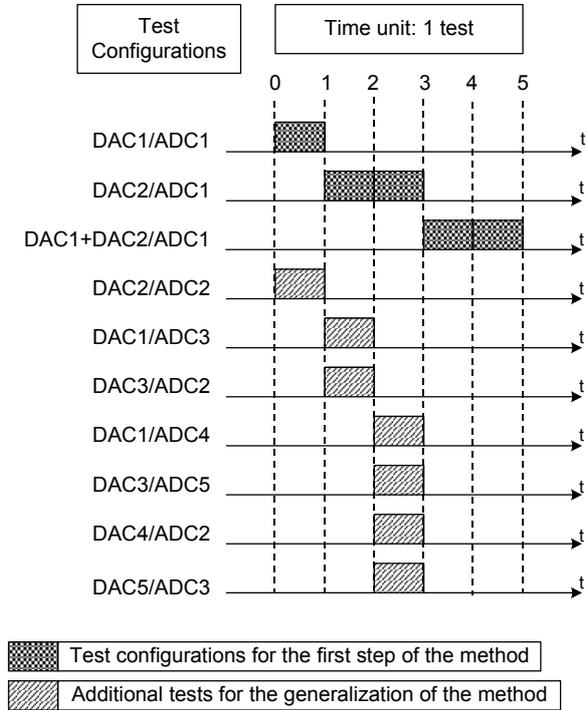
Figure 10 gives a temporal description of the test configurations that would be used in order to test this set of 10 converters. There are two kinds of tests:

- Test configurations for the first step of the method, used to characterize DAC1, DAC2 and ADC1.
- Additional tests for the generalization of the method in order to test the seven other converters.

The time unit is one test. One test is equal to the time required to test one converter with a classical approach. We assume that this time is equivalent to the time for a C(1,1) or C(2,1) test. The total test time is equal to five because five consecutive tests are needed for the first step.

In the first time slot, two tests are performed simultaneously. The test configurations are DAC1/ADC1 and DAC2/ADC2. The results of the DAC1/ADC1 are exploited in the estimation of DAC1, DAC2, and ADC1 parameters, while the results of DAC2/ADC2 will help characterize ADC2, when DAC2 parameters are known.

In the second time slot, three tests are done using DAC2/ADC1, DAC1/ADC3 and DAC3/ADC2 configurations. The first test is part of the process for estimating DAC1, DAC2, and ADC1, and the two additional tests permit to characterize ADC3 and DAC3. The remaining parameters are similarly computed in the subsequent time slots.



**Figure 10: Temporal description of the test configuration for the generalization of the method**

At the end of the process, for a test time of five, the distortion of ten converters can be computed. In the

first step DAC1 DAC2 and ADC1 are tested. Only one test per converter is required to additionally test DAC3..5 and ADC2..5 using parallel testing.

Obviously this generalization of the first step is an example of a possible process that can be elaborated in order to reduce the test time. The generalization depends on the number of converters to test, their specifications and the number of digital pins available on the tester. As a consequence a generalization should be elaborated for each case.

But it appears clearly that using this test methodology helps reduce the test time of a set of converters embedded in a SiP or SoC.

## 5. Validation

A number of experiments based on simulation have been conducted to validate the first step of the proposed approach. The converter model used for simulation is first introduced, then the simulation setup is defined, and finally simulation results are presented. The performance of the proposed test strategy is discussed in terms of estimation error on the harmonic components and on the dynamic parameters.

### 5.1. Data converter model

In order to simulate the test strategy, we need to establish a model that takes into account the effects of the converter non-idealities. Three main sources of errors will be considered, i.e. the sampling jitter of the converter, the non-linearities of its transfer function and the thermal noise.

Let us consider  $r(n)$  an input sine wave passing through an ideal converter and affected by the jitter,  $J_t$ , and the thermal noise,  $N_{th}$ .

$$r(n) = 2^N \left( \frac{V_0}{V_{FS}} \right) \cos(\theta_n + J_t + \theta_0) + 2^N \left( \frac{V_{DC}}{V_{FS}} \right) + N_{th} \quad (17)$$

where  $N$  and  $V_{FS}$  respectively represent the number of bits and the full-scale voltage of the converter,  $V_0$  and  $V_{DC}$  respectively correspond to the amplitude and the DC component of the input sine-wave, and  $\theta_0$  and  $\theta_n$  are respectively the initial and nominal sampling phase of the signal.  $J_t = 2\pi f_0 \delta_t$ , with  $f_0$  the frequency of the input signal and  $\delta_t$  a centred Gaussian noise. The thermal noise is usually modelled by a centred Gaussian noise.

The second significant source of errors that has to be considered is the non-linearity of the converter transfer function. A common approach to analytically model the converter INL is based on polynomial approximation [4] [14] [16]. However, such modeling tends to smooth the sharp transitions usually encountered for actual INL. In order to alleviate this drawback, we choose an approach that consists in using “true” INL curves extracted from measurements on real data converters. Consequently, let us consider  $s(n)$  the signal deteriorated by the two types of errors:

$$s(n) = [ r(n) + INL([r(n)]) ] \quad (18)$$

where  $INL(x)$  is a non-linearity curve measured through histogram testing of a real converter. This non-linearity curve is indexed by the rounded signal including the sampling jitter effect  $[r(n)]$ . The complete equation is rounded to model the quantization effect.

Equation (18) models the deterioration of a sine-wave signal passing through a converter affected by sampling jitter, transfer function non-linearities and thermal noise. This equation has been used for the simulations described in the following sections.

## 5.2. Simulation setup

In order to validate the proposed test strategy, we have conducted a number of simulations considering data converters of the same resolution and sampling frequency. The objective is to compare the values of the harmonic components evaluated using the proposed strategy to the ones obtained using a classical stand-alone test.

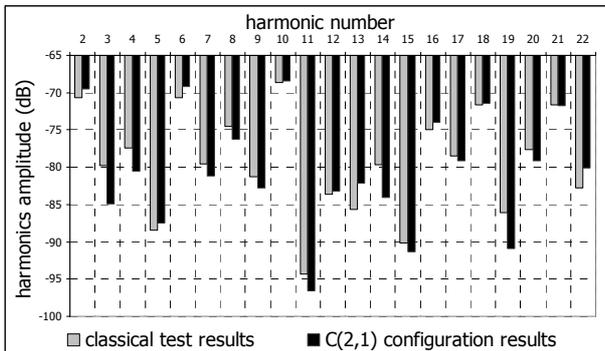
In an initial phase, we performed measurements on real data converters to extract INL curves. Practically, these INL curves were determined by performing a histogram test on 15 different PHILIPS 12-bits ADC TDA9910. Using equation (18), we could therefore model 15 different converters. Subsequently, two sets of simulation were run:

At first, we considered each data converter in a stand-alone configuration to get reference values.

Then, we considered five different C(2,1) configurations, with three different converters each time. For each C(2,1) configuration, we simulated the test algorithm described in section 3.2.

## 5.3. Results and discussion

As an example, Figure 9 presents the results obtained for one converter. The amplitude of the harmonic components evaluated using the C(2,1) configuration (grey bins) are compared to the amplitude of the harmonic components computed using the classical stand-alone test configuration (black bins).



**Figure 11: Estimation of the first 20 harmonics of one converter vs. reference values**

The maximum estimation error, observed on the amplitude of the first 20 harmonic components, is about 5dB. However, it is worth noting that this error is observed for a harmonic component of very small amplitude ( $\approx -85$ dB). Considering only the major harmonic components with amplitude higher than -

75dB, the observed estimation error remains below 2dB. These results show the efficiency of the proposed strategy that permits an accurate evaluation of the converter harmonic components.

Similar simulations have been performed for the complete set of 15 different converters. Results are summarized in Table 1 that reports the maximum estimation error observed on the amplitude of the first 20 harmonic components for the different converters. Results have been classified in three ranges according to the amplitude of the harmonics.

**Table 1: Maximum estimation errors vs. the amplitude range of the harmonic components (dB)**

Converter #	Maximum Error for Ranges of Wanted Amplitudes (dB)		
	$h > -75$ dB	$-75$ dB $>h > -85$ dB	$-85$ dB $>h$
Converter #1	0.28	-7.99	-16.04
#2	-0.64	7.58	-19.23
#3	0.36	7.62	3.55
#4	-0.26	6.1	-8.49
#5	-0.25	0.91	11.60
#6	-0.33	-4.89	5.73
#7	0.24	-3.73	-18.16
#8	-0.39	2.10	-22.31
#9	0.25	8.00	6.58
#10	3.50	1.03	3.78
#11	-0.10	-2.10	-2.96
#12	-0.29	-1.02	22.9
#13	-0.37	-1.2	4.59
#14	0.14	3.17	14.20
#15	-0.45	-4.84	5.42

Analyzing these results of Table 1, it can be seen that the higher the amplitude of the harmonic component, the better the estimation. On the complete set of 15 converters, the maximum estimation error remains below 3.5dB for harmonic components with amplitude higher than -75dB, 8.00dB for harmonic components with amplitude between -75dB and -85dB, and 22.31dB for harmonic components with amplitude smaller than -85dB. Despite of few significant estimation errors, the estimated values are still in the amplitude range of the wanted harmonics. This is a satisfactory result, taking into account that the purpose of the test is to distinguish converters that exhibit poor performances, i.e. converters that present harmonic components with high amplitude (typically higher than 75dB for a 12-bit converter).

To further validate the efficiency of the proposed strategy, we have evaluated two classical dynamic parameters, namely the Total Harmonic Distortion (THD) and the Spurious-Free Dynamic Range (SFDR), for the 15 different converters. These parameters are evaluated from the spectral distribution. Results are summarized in Table 2, which reports the THD/SFDR values computed using the stand-alone configuration and the THD/SFDR values computed using the C(2,1) configuration, and the corresponding estimation error

**Table 2: THD and SFDR estimation error**

Converter Number	Wanted THD (dB)	THD estimation (dB)	THD error (dB)	Wanted SFDR (dB)	SFDR estimation (dB)	SFDR error (dB)
#1	-59.1	-59.0	0.4	68.8	69.3	-0.5
#2	-58.0	-57.9	-0.1	69.3	69.9	-0.6
#3	-58.2	-58.2	0	67.9	67.5	0.4
#4	-64.3	-63.9	-0.4	69.4	68.9	0.5
#5	-66.7	-66.9	0.2	70.9	71.1	-0.2
#6	-61.7	-58.8	-2.9	63.4	64.2	-0.8
#7	-48.1	-48.1	0	67.1	66.3	0.8
#8	-62.7	-62.2	-0.5	65.4	64.7	0.7
#9	-60.7	-60.9	0.2	64.9	65.5	-0.6
#10	-59.7	-59.7	0	62.2	62.2	0
#11	-61.5	-61.8	0.3	64.0	65.1	-1.1
#12	-61.6	-61.4	-0.2	62.8	62.8	0
#13	-70.4	-69.6	-0.8	71.1	67.4	3.7
#14	-55.5	-55.6	0.1	65.0	65.0	0
#15	-64.0	-63.6	-0.4	68.6	68.4	0.2

Analyzing these results, it can be seen that the proposed strategy enables a very accurate measurement of both these dynamic parameters, with an estimation error that remains below 3.7dB for the 15 different converters considered in the experiment. Note that such a low estimation error actually corresponds to the accuracy range that we can expect for the measurement of these parameters taking into account fluctuations in the test environment. Indeed, the reference values computed here with the stand-alone configuration are obtained considering ideal test instruments. However in a real environment, the repeatability of the measurements is impacted by unavoidable fluctuations in the test instrumentation. As a result, it is very classical to observe dispersion in the range of 5 to 10% when measuring the THD and SFDR parameters in a real environment.

## 6. Conclusion

The "Analogue Network of Converters" (ANC) represents a real breakthrough in the techniques for testing the harmonic distortion of embedded converters. The proposed method solves the problem of using very expensive mixed-signal instruments, thanks to a fully digital process.

Another benefit of the method relies on test time reduction. We have demonstrated that the generalization of the method to several converters leads to a significant reduction of the time required for both acquisition and data processing. Moreover, we build the basis of a BIST solution, based on an at-speed functional and parametric approach.

This method is in line with the test strategy applied to the SiP, electronic complex devices with embedded data converters, overcoming the observability and controllability issues.

Many experiments will follow this study, in order to validate the method on various converter architectures, and to check its robustness against some test parameters, such as signal amplitudes, or resolution.

## Acknowledgement:

This work has been carried out under frame of the European MEDEA+ Project: "Nanotest".

## References

- [1] M.Toner, G.Roberts, "A BIST scheme for an SNR test of a sigma-delta ADC", *Proc International Test Conf.*, 17-21 Oct. 1993 Page(s):805 - 814.
- [2] M.Toner, G.Roberts, "A BIST Technique for a Frequency Response and Intermodulation Distortion Test of a Sigma-Delta ADC", *Proc 12th IEEE VLSI Test Symp.*, 25-28 April 1994 Page(s):60 - 65.
- [3] M.J.Ohletz, "Hybrid Built In Self Test (HBIST) for Mixed Analog/Digital Integrated Circuits", *Proc. European Test Conference*, 1991, pp.307-16
- [4] S.K.Sunter, N.Nagi, "A simplified polynomial-fitting algorithm for DAC and ADC BIST" *Proc. IEEE International Test Conference*, pp.389-395, 1997.
- [5] F.Azais, S.Bernard, Y.Bertrand, M.Renovell, "Towards an ADC BIST scheme using the histogram test technique" *European Test Workshop, 2000*. Proceedings. IEEE 23-26 May 2000 Page(s):53 - 58
- [6] F.Azais, S.Bernard, Y.Bertrand, M.Renovell, "Implementation of a linear histogram BIST for ADC's" *Design, Automation and Test in Europe, 2001*. Conference and Exhibition 2001. Proceedings 13-16 March 2001 Page(s):590 - 595
- [7] K.Arabi, B.Kaminska, J.Rzeszut, "A New Built-In Self Test Approach For Digital-to-Analog and Analog-to-Digital Converters", *Proc. of ICCAD*, 1994.
- [8] N.Nagi, A.Chatterjee, J.Abraham "A Signature Analyzer for Analog and Mixed-Signal Circuits", *Proc. ICCD, 1994* pp284-287
- [9] M. Mahoney, "DSP-Based Testing of Analog and Mixed-Signal Circuits", *IEEE Computer Society Press*, ISBN 0-8186-0785-8, 1987.
- [10] Datasheet of PNX8327, [http://www.semiconductors.philips.com/applications/video\\_broadcast/stb/stb210\\_sat/index.html](http://www.semiconductors.philips.com/applications/video_broadcast/stb/stb210_sat/index.html)
- [11] C.Taillefer, G.W.Roberts "Reducing Measurement Uncertainty in a DSP-Based Mixed-Signal Test Environment without Increasing Test Time", *Proceedings. International Test Conf 2004* Page(s):953 - 962
- [12] J.A. Mielke, Frequency domain testing of ADC's *Design & Test of Computers*, IEEE Volume 13, Issue 1, Spring 1996 Page(s):64 - 69
- [13] J-M. Janik, "Estimation of A/D Converter Nonlinearities from complex Spectrum", *Proc. International Workshop on ADC Modeling and Testing*, pp.8-10. September 2003.
- [14] F. Xu, "A New Approach for the Nonlinearity Test of ADC's/DAC's and its application for BIST", *Proc. IEEE European Test Workshop*, pp 34-39, 1999
- [15] H. Jiang, D. Chen and R.L. Geiger "Dither Incorporated Deterministic Dynamic Element Matching for High Resolution ADC Test Using Extremely Low Resolution DAC's" *Circuits and Systems, 2005. ISCAS 2005*. IEEE International Symposium on 23-26 May 2005 Page(s):4285 - 4288 Vol. 5
- [16] F. Adamo, F. Attivissimo, N. Giaquinto, and M. Savino, "FFT Test of A/D Converters to Determine the Integral Nonlinearity", *IEEE Trans. Instrum. Meas.*, vol. 51, no. 5, pp. 1050-1054, Oct. 2002