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Large area silicon epitaxy using pulsed DC magnetron sputtering deposition

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Abstract:

Pulsed DC magnetron sputtering is used for deposition of large area crystalline (200 mm) silicon 100nm thin films. p doped Si substrates are flashed (T_s = 900 °C) under high vacuum (5 10^{-6} Pa) for removing native oxide and restoring surface crystallinity. Subsequent boron doped Si homoepitaxy is obtained at substrate temperature below 500°C for pulse frequency of 150 kHz.

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Introduction

Large area deposition of hydrogen free crystalline silicon is highly desirable for many applications in micro and macroelectronics such as silicon on insulator substrates, solar cells … Even though low temperature epitaxy of crystalline silicon is well addressed [1-3], a recent study by Reinig et al [4] has shown that simple pulsed DC magnetron sputtering allows growth of epitaxial films of intrinsic silicon on chemically prepared silicon wafers. Combined DC-RF (100MHz) magnetron sputtering has also been carried out to obtain silicon epitaxy on silicon [5]. The preparation of the substrate, regarding the crystal structure and purity of the outer surface, is a critical step of the starting conditions of the epitaxial growth. The other critical parameter is the ion flux impinging the substrate during deposition. Previous studies [4] reporting on pulsed magnetron sputtering deposition have shown that wet RCA cleaning procedures are suitable for further epitaxy. Nevertheless, for a fully integrated epitaxy system, a vacuum cleaning procedure is highly desirable, so the cleaning and deposition steps can be realized in the same chamber. Moreover, for compatibility with other deposition steps, highly uniform large area silicon epitaxy on 200 mm wafer is also required, while previous studies were only carried out on small samples of a few cm^2. The present article reports on the successful attempt to deposit boron-doped silicon epitaxy by pulsed DC magnetron sputtering on 200mm wafers with a in-situ low temperature (900°C) rapid thermal annealing (RTA) cleaning of the substrate. Thus, this study provides a new way towards a full ultra high vacuum large area silicon epitaxy system, including wafer cleaning. Moreover, the thermal budget of such a process is far less than a usual CVD processes. This process also has the added benefit of being environmentally friendly, using only argon gas instead of the dangerous/or toxic gases/liquids used in thermal CVD and RCA cleaning processes.

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2. Experimental

Samples were prepared in a plasma deposition reactor (MHS-Equipment) by pulsed-dc magnetron sputtering (50 W, -200 V) in pure Ar atmosphere from a boron doped (0.1 Ω.cm, [B] = 5. $10^{17}cm^{-3}$) Si-target. The sputtering pressure is 0.5 Pa and the target to substrate distance is 90 mm. The base pressure of the load-lock vacuum system is in the range of 1-2 10^{-6}Pa. The pulsed DC plasma was ignited using a pulse frequency of 150 kHz at a fixed duty cycle 60% on. As substrates, boron-doped (19 Ω.cm, [B] = 7. $10^{14}cm^{-3}$) 200 mm monocrystalline Si-wafers with a (100) surface orientation, were used. The Si substrates were cleaned (native oxide removal) using low temperature (900°C, 30 seconds) RTA in a UHV closed connected chamber (MHS-Equipment) before deposition. Samples were transferred under UHV to the deposition chamber for the deposition step and the samples were electrically grounded. The deposition temperature is controlled up to 500°C with a temperature regulator (UHV Design Ltd.).

Raman-spectrometry (Horiba-Jobin-Yvon LabRam HR, 325 nm line of He-Cd probe laser), UV-Visible spectroscopic Ellipsometry (Horiba-Jobin-Yvon UVISEL) and Transmission Electron Microscopy (Philips CM30) were employed to obtain a complete set of characterisations of the crystalline structure of the films. Doping depth profiling was analyzed using CAMECA SIMS ion probe IMS6F.

3. Results

Si deposition was performed at substrate temperature of 450°C with Argon flow of 250 sccm. This led to a growth rate of 3nm/min. Silicon epi-layer of 100 nm where deposited with a film thickness uniformity below <2% for 200 mm diameter wafers. Moreover, when the magnetron target was tilted by 30° with respect to the horizontal plane, the thickness uniformity was reduced below 1%.

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Figure 1 displays a TEM micrograph showing the very good crystalline arrangement of the deposited silicon layer. This was possible only after the 900°C RTP annealing step, which allowed for a good crystalline and defect-free starting surface. It should be noted that the deposition is not followed by an additional annealing step; the deposited layer is observed directly after processing. While some interface defects are observed between substrate an layer, there is still continuity of the crystalline structure from bulk to the epilayer.

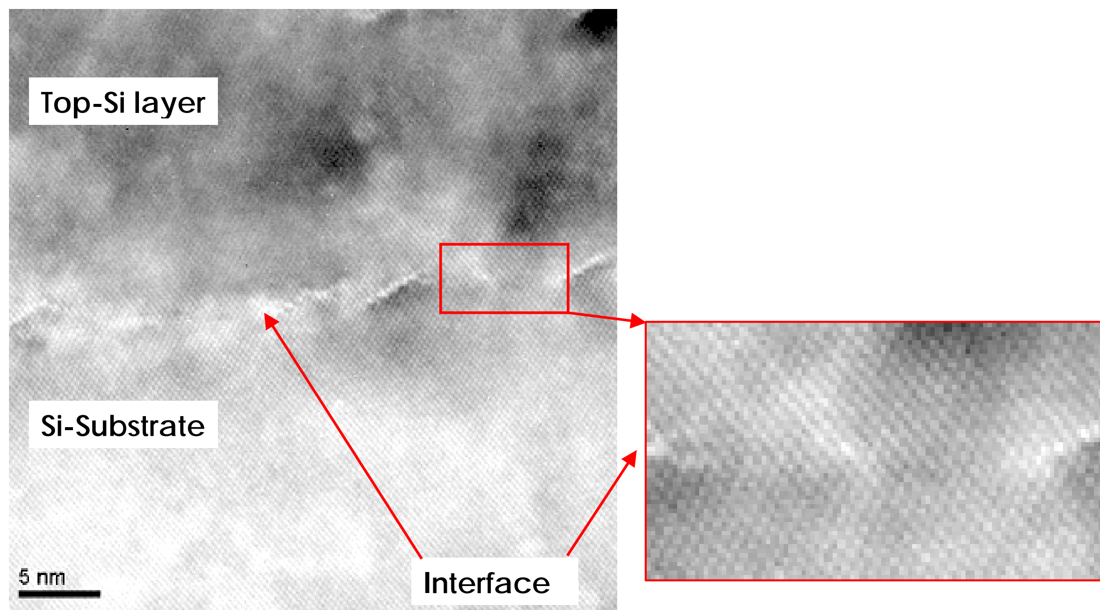

Figure 1: TEM micrograph of silicon layer without post - annealing.

When an additional annealing step (850°C, 2 min) is performed after the deposition, the interface quality is further increased (Figure 2) and results in an ideal continuity between the Si-substrate and the deposited Si-layer.

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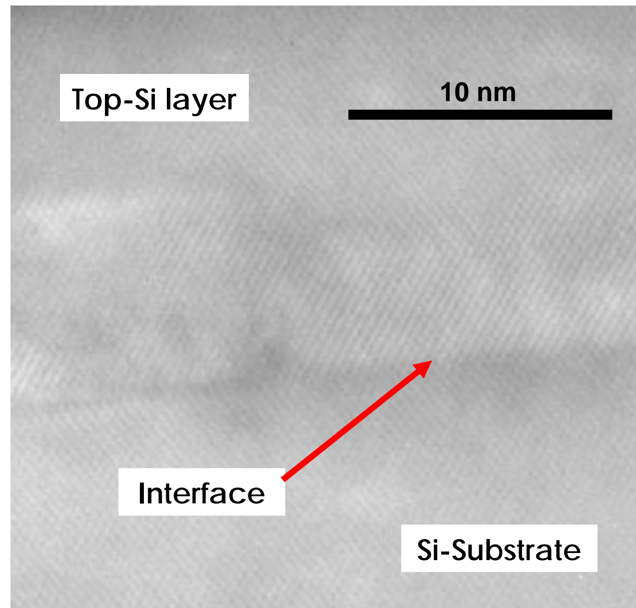

Figure 2: TEM micrograph of the silicon layer after annealing at 850°C for 2 min

It should be pointed out that the present silicon epitaxy is obtained using a doped target, which was not in previous works [4, 5]. This capability is of great interest for SOI applications, where doped layer may require additional doping diffusion steps.

Because TEM observations are very localised, determination of the structure on a larger scale was obtained by using Raman Spectroscopy which is a highly sensitive probe of long range order and is thus well suited for analysing crystalline state. This was conducted at different locations on the wafer. Figure 3 displays Raman spectra of the bare substrate and the Si layer. The Si TO Raman peak has the same position and the same width for both Si bulk and layer, indicating the large scale order of the layer. The He-Cd laser wavelength (325 nm) allows only probing of the layer without any contribution from the substrate.

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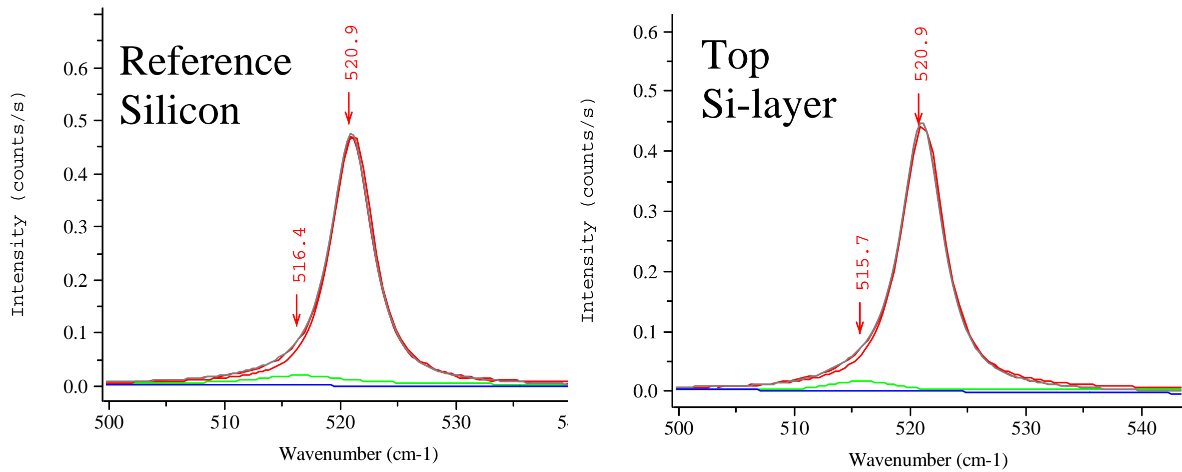

Figure 3: Raman spectra of the bare silicon and the top Si-layer

Spectroscopic ellipsometry was used to control the crystalline homogeneity at various location of the surface using an automated scanning of the wafer area (314 cm^2) with 30 randomly analysed zones (0.2 cm^2). All the analyzed zones were shown to be crystalline. As revealed by Figure 4 where typical (n, k) plots of the Si bare substrate and of the top Si-layer are displayed, no difference between the crystalline state of the substrate and the Si deposited layer is observed.

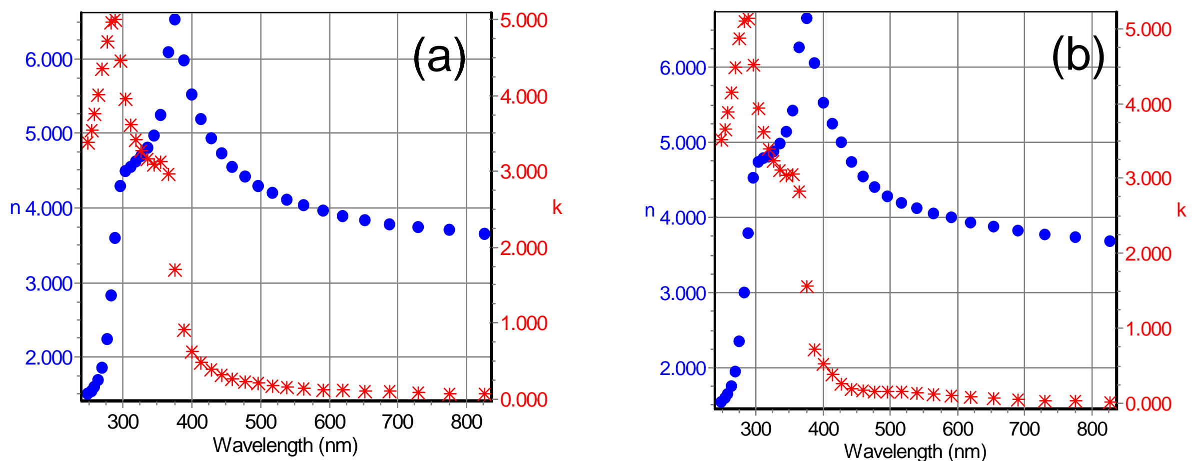

Figure 4: Typical (n,k) plots as function of incident light wavelength.
(a) Si bare substrate (b) Si epitaxial layer. Symbols (●) are for n and (∗) for k

The deposition experiment were carried out over a period of 12 months, both before and after maintenance was conducted on the systems, including opening the deposition chamber to

ambient air. No shift of the silicon film crystallinity was noted, showing a high reproducibilty and reliability of the proposed process.

As mentioned above the Si target is boron-doped for allowing the direct growth of a Si doped epi-layer. The successfully grown layers were analyzed by SIMS for highlighting the boron depth profile in the deposited silicon layer. Figure 5 shows the boron profiles (after annealing at 900°C) at the center and at the edge of the Si epilayer. Because the doping level in the sputtering target is higher than in the substrate, this difference is also observable in the Si layer. The boron depth profile displays a peak close to the Si-Si interface. This could be due to the target preparation which induces target surface heating and some boron segregation or also It is residual B on the Si substrate after cleaning, perhaps due to B incorporated in the native oxide as for MBE [6]. Moreover, for a controllable boron doping, a two target system, intrinsic and boron doped silicon could be easily implemented.

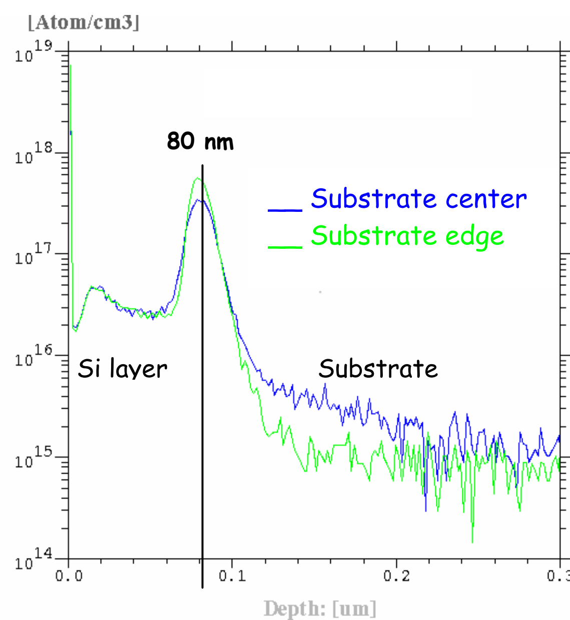

Figure 5: Boron depth profile in the deposited crystalline silicon at wafer center and edge

4. Conclusion

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High quality, large area (200mm), boron-doped silicon layer epitaxy is obtained using pulsed DC magnetron sputtering. It is shown that the initial substrate cleaning by low temperature RTA is very efficient in preparing a non-oxidized, defect free, crystalline surface. The Si-Si interface, probed by TEM, shows very good crystalline continuity despite the boron doping. Raman spectroscopy and spectroscopic ellipsometry show a very good crystalline homogeneity. The boron concentration is continuously distributed within the deposited layer. However there is an increase in concentration near the layer/substrate interface that is not fully understood.

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