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THERMAL MODELLING OF MULTI-FINGER ALGAN/GAN HEMT's

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ABSTRACT

AlGaN/GaN high electron mobility transistors (HEMTs) are very promising for high power applications at microwave frequencies. The heterostructures are usually grown on SiC or sapphire substrates. Sapphire substrates are relatively cheap, but their low thermal conductivity is a major disadvantage. To improve the thermal performance, a hybrid integration of the HEMT onto an AlN carrier substrate is proposed. In this study we compare two different hybrid integration schemes for multi-finger HEMTs: a flip-chip integration and an integration where the sapphire substrate is removed by laser lift-off. The two structured are compared using finite element analysis. After experimental validation of the modelling, both structures are thermally optimized.

1. INTRODUCTION

As GaN devices operate at exceptionally high power density, self-heating is a crucial issue, which needs to be addressed specifically. Output power density has climbed up to typically 12W/mm. For comparison, a typical GaAs MMIC is capable of delivering about 0.75W/mm. The rapid increase in power density since the beginning of the development of GaN amplifier is to be found in the use of SiC substrates instead of sapphire, and the development of passivation. Indeed, although GaN possess outstanding physical properties and has been demonstrated promising prototypes, the lack of a suitable low-cost and low-mismatch substrate remains a "bottleneck" for the development of high-power devices. The most widely used substrate compounds are by now, sapphire and SiC [3]. As the thermal conductivity of SiC is far larger than the one of sapphire (4 W/cm°C compared to 0.45 W/cm°C for sapphire), the best power performance is indeed recorded on SiC substrate. At high power, self-heating of the device occurs and reduces the ability of the nitride devices grown on sapphire to withstand high power/high temperature conditions. However, regarding the cost of SiC substrates, which are
ten times more expensive than sapphire, it indeed still makes sense to look for solutions of thermal management for devices grown on sapphire.

2. STRUCTURE OF THE TRANSISTOR

For this study, epitaxial layers for GaN HEMTs are grown by MOVPE (Metal-Organic Vapor Phase Epitaxy) on sapphire substrates [1]. Multi-finger HEMTs are processed using a standard processing scheme: mesa etch, ohmic contacts, contact metal, gate metal (1.5 mm gate length) and passivation. Figure 1 shows the AlGaN/GaN HEMT layout. The dimensions of the layout are given in Table 1. The device layout investigated consists of 6 gate fingers each with a gate length of 0.25 µm and a gate width of 100 µm, which yields a total gate width of 0.6 mm. A 100 µm pitch separates the gate fingers. The source fingers are connected with plated gold air bridges. The airgap underneath the bridge structure is 2 µm. Drain fingers and pads are also gold plated (0.15µm thick).

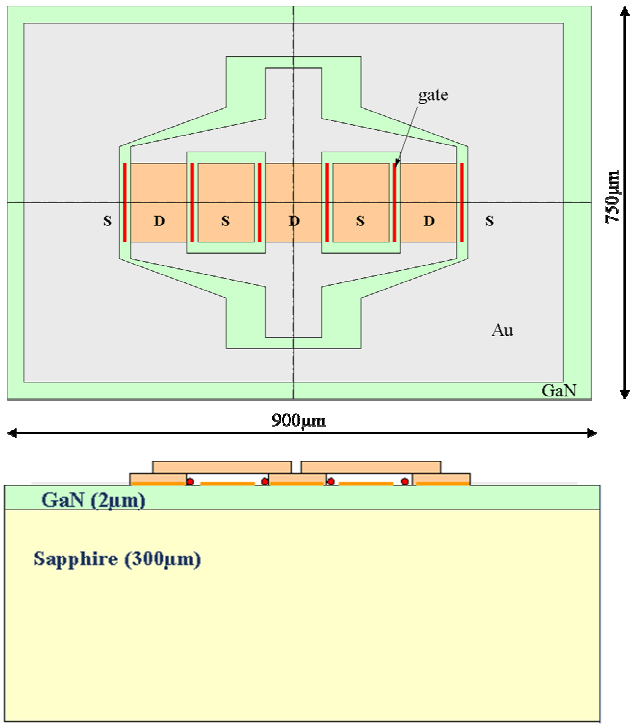

Figure 1: Schematic diagram of the transistor layout. (a) Top view. (b) Cross section

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3. MODEL FOR THERMAL ANALYSIS

A fully three dimensional finite element model is build to study the thermal behaviour of the different integration structures using the commercial software code MSC-MARC. In the simulations the entire conduction channel region where the heat is generated (Fig. 2) is taken as the heat source[2]. The heat generation is assumed to be uniform in this channel region. The channel length is 5µm and the width for one finger is 100µm. For a heat dissipation of 3W/mm gate width for the 6 fingers, this amounts to a total heat dissipation of 1.8W. Table 1 gives the thermal conductivity of the materials used in the simulations [3,4,5]. For GaN and sapphire the temperature dependency of the thermal conductivity is taken into account.

Table 1: Conductivity and thickness of the materials used in the simulations

Material	Thermal conductivity [W/m-K]	Thickness [µm]
GaN	$130*(T/300K)^{-1.4}$	2
Sapphire	45*(T/300K)	300
Au	310	0.15
AlN	180	300
SU-8	0.25	5
Solder	50	25
SiO_2	1	0.15

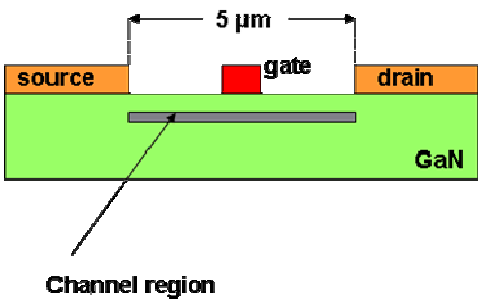

Figure 2: Channel region of the transistor where the heat is generated

The thermal behaviour of the device will be examined for three different integration structures:

1. the device is mounted on an AlN substrate
2. the device is flip assembled on the AlN substrate
3. the device is bonded using SU-8 on the AlN substrate and the sapphire substrate is removed using a laser lift off technique.

3.1. Transistor mounted on AlN substrate

Figure 4 displays the calculated temperature profile in the GaN layer along the transverse direction. The calculated peak temperature is 104 °C with input power of 1.8 W and 25°C base temperature on the bottom surface of the device. A detail view of the temperature distribution is shown in Fig. 3. As seen in Fig. 4 the temperature decreases sharply at location away from the channel region.

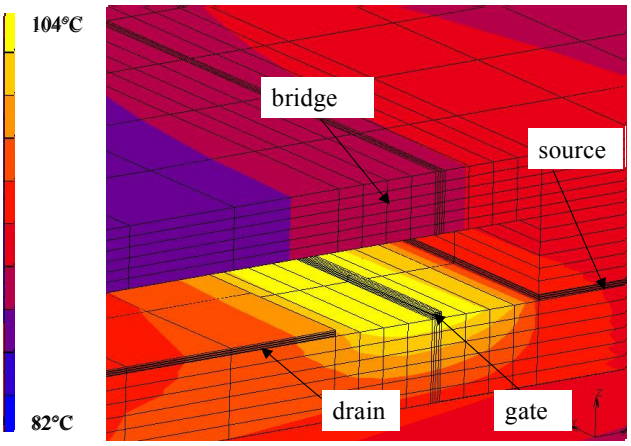

Figure 3: Detail view of the temperature distribution in the vicinity of the gate. The power density in the channel region is 3W/mm and the base temperature of the substrate is 25°C.

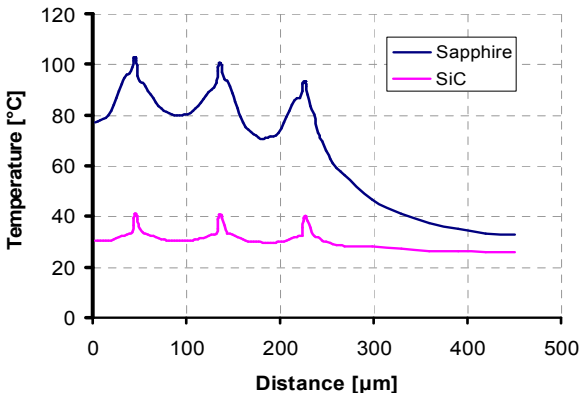

Figure 4:Temperature profile in the GaN-layer of a 6-finger HEMT device on a sapphire and SiC substrate for a power input of 3W/mm and a base temperature of 25°C at the bottom tof the device.

Since the thermal conductivity of the materials is temperature dependent, the relation between the power input and the peak temperature is non-linear. This can be seen in Fig. 5. The demonstrated devices have a power density of 3W/mm. In the future this power density will have to increase up to 15W/mm. From Fig. 5 it can be seen that other integration techniques need to be used to reduce the maximum temperature in the GaN.

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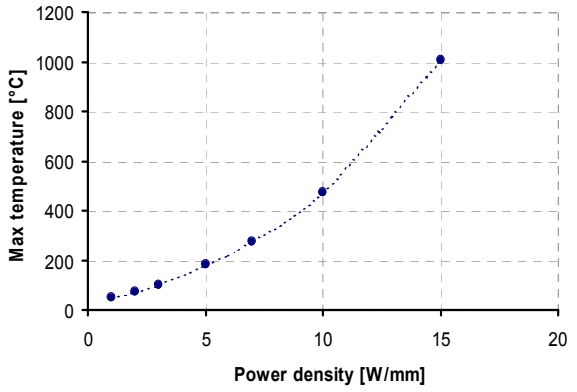

Figure 5: Evolution of the maximum temperature in the GaN layer as a function of the power density in the channel region.

3.2. Flip chip structure

For the flip-chip integration, an electroplated Cu airbridge, with (or without) BCB underfill, is deposited to connect the isolated source areas. In the final step the complete devices (including air-bridge) are diced and bonded onto the AlN carrier using Sn-bumps. The diameter of the bumps is 75µm and the heigth is 75µm. The position of the solder flip chip connections is illustrated on Figure 6.

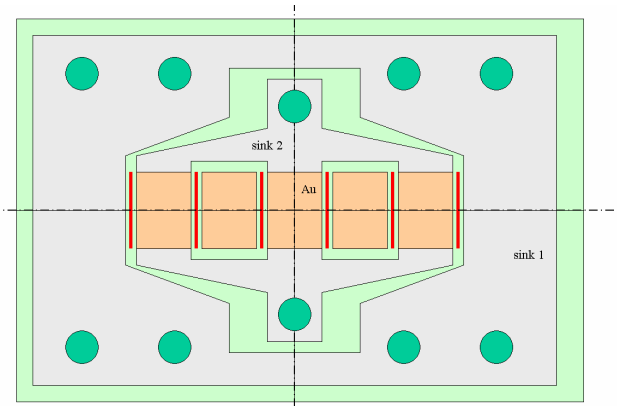

Figure 6: Position of the solder balls on the device.

Figure 7 shows the temperature distribution in the GaN layer of the HEMT. From the thermal simulations, we found that the placement of the bumps is very important in order to get an optimal thermal performance. The dissipated power of the HEMT can only be removed via the solder bumps. By placing bumps closer to the active area, the maximal device temperature will drop significantly. Other improvements made are the placement of extra bumps on the sources and drains. In this case the air bridge has to be replaced by a metal layer on the substrate side to provide the connections. The results of the modifications on the maximum temperature can be seen in Figure 8.

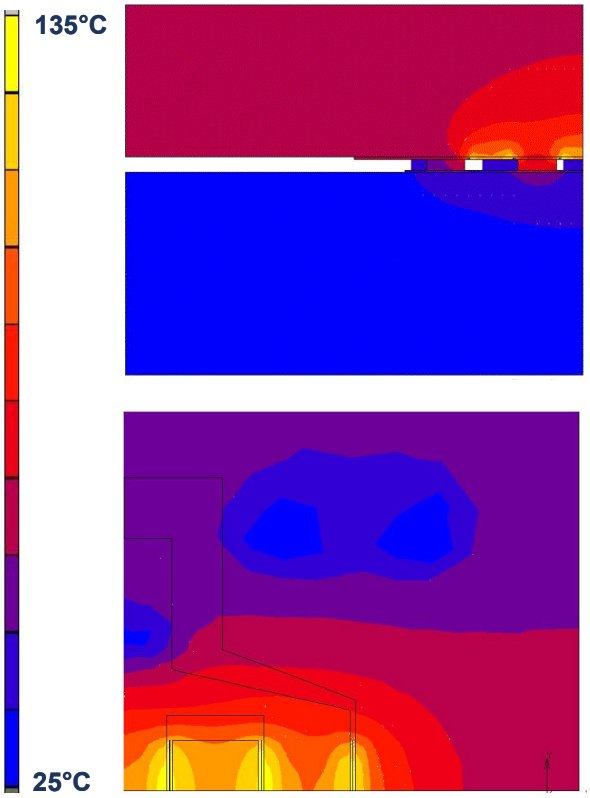

Figure 7: Temperature distribution in the flip chip assembled device. The input power density is 3W/mm. (a)Vertical cross section (b) Temperature distribution in GaN layer.

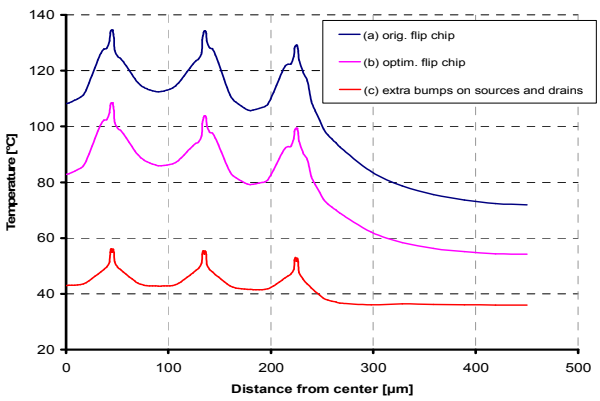

Figure 8: Temperature profile along the center axis in the GaN layer:
(a) for the original position of the solder balls (Fig. 6) ;
(b) for an optimised postion of the solderballs;
(c) also solderballs placed on the source and drain pads.

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3.3. Laser lift off structure

For the third integration scheme, no airbridges are made on the front side of the wafer. Here the devices are diced and bonded using SU-8 onto the AlN carrier. Then, the sapphire substrate is removed using laser lift-off, followed by a Cl2-etch to provide electrical contacts at the backside of the HEMT. Finally a Cu-layer is electroplated to establish an airbridge-like connection at the backside of the HEMT. The connections to the source pad are made through Cu vias through the GaN layer. Figure 9 illustrates the different steps in the processing.

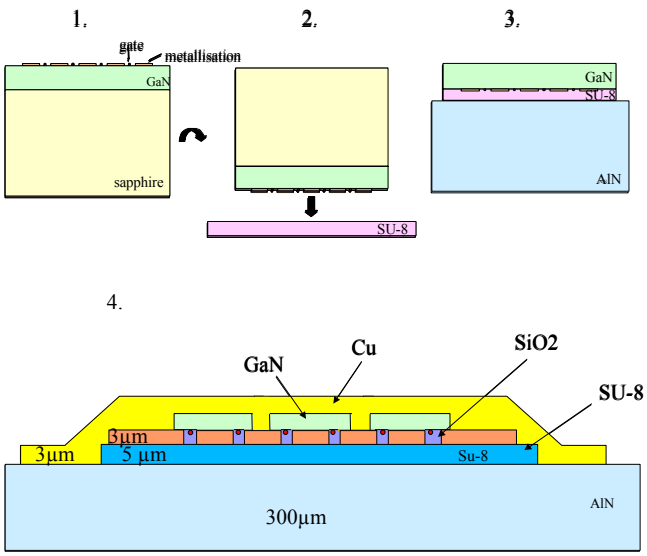

Figure 9: Steps in the processing of the laser lift off structure.

In case of a flip-chip configuration, the dissipated power of the HEMT can only be removed via the solder bumps; whereas for the laser lift-off configuration multiple thermal leakage pads are present, close the heat generating zone. Therefore this structure is more interesting than the flip chip structure. However the temperatures reached in this structure are a much higher than in the other structures for the same input power densities. The temperature distribution in the GaN layer is shown in Figure 10. Here the thermal bottleneck is the very poor thermal conductivity of the glue layer; only 0.25 W/m-K. Moreover an optimisation of the thermal performance of the laser lift-off configuration is still possible: one can e.g. consider to deposit cooling layers at the frontside and/or backside of the HEMT, or to reduce the thermal resistance of the glue layer. This can be done by decreasing the thickness of the layer or by increasing the equivalent thermal conductivity of the glue (adding metal particles or thermal vias).

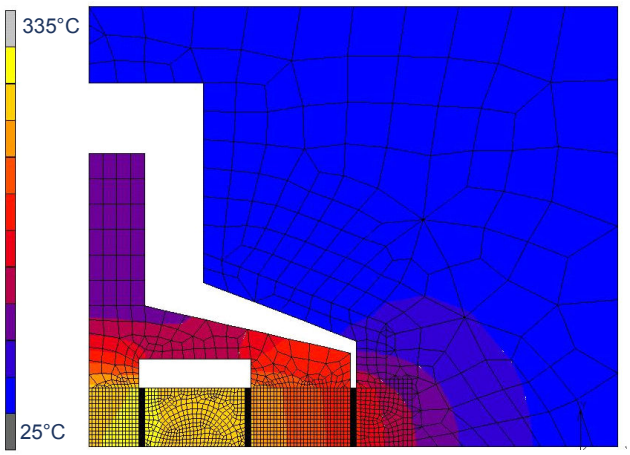

Figure 10: Temperature distribution in the GaN layer in the laser lift off structure. The input power density is 3W/mm and the base temperature at the bottom of the AlN substrate is 25°C.

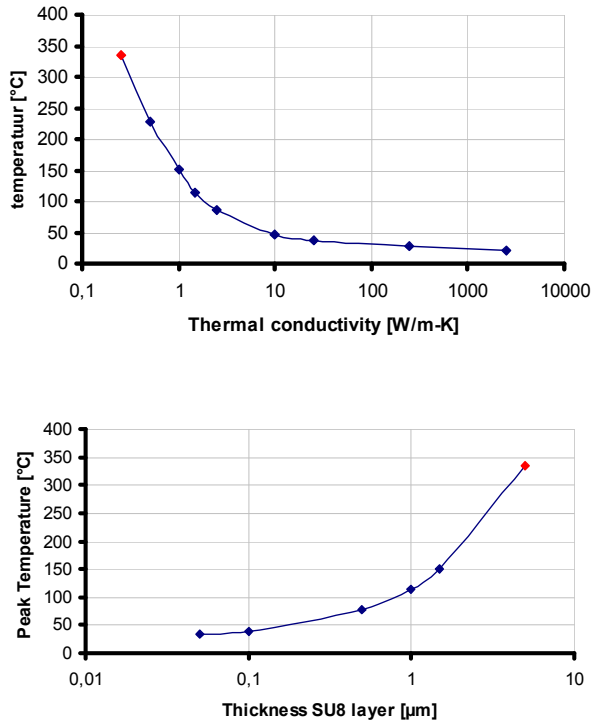

Figure 11: Influence of the thickness and the thermal conductivity of the SU-8 glue layer on the maximum temperature in the GaN layer.

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3.4. Thermal measurements of the

The temperature of the active devices is experimentally measured for all the structures presented here by the group of Dr. Kuball at University Bristol. The measurements are performed using Raman spectroscopy [6]. All the devices are measured at different power levels. The results of these measurements are first used to gain information about the material properties and the dimension of the channel region. Later the results of the measurements are used to validate the simulations.

5. CONCLUSIONS

In this paper the temperature distribution in an AlGaN/GaN high electron mobility transistor (HEMT) is calculated using a three dimensional finite element model. Three different integration schemes for the transistor are compared and optimised:

1. directly mounted on a AlN carrier;
2. flip chip assembled on a AlN carrier;
3. laser lift off substrate removal.

The laser lift off substrate removal structure shows the most promise for higher power densities if the thermal resistance of the glue layer can be optimised.

The results of the simulations are compared to Raman spectroscopy measurements, of the active devices.

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