Theoretical investigation of thermal feedback effects in low-power circuits

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THEORETICAL INVESTIGATION OF THERMAL FEEDBACK EFFECTS IN LOW-POWER CIRCUITS

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ABSTRACT

The paper presents electro-thermal simulation methodology and its application to a simple LDO regulator circuit. Presented simulation results show that thermal feedback can affect, not only high power circuits, but also relatively low power high resolution circuits such as LDO regulators or A/D converters. Potential benefits of electro-thermal simulator (SISSI) are shown by applying thermal feedback to improve low frequency figures of merits of a simple LDO regulator.

1. INTRODUCTION

Increasing speed and component density of different integrated circuits cause higher power dissipation per unit area, consequently higher and higher temperature on the chip surface. These effects may result in immediate reliability degradation or different functional problems. The importance of the electro-thermal simulation, thermal characterization and investigation of temperature distribution of the semiconductor structure are well understood today.

The temperature-aware design has great challenges. There are several different techniques to achieve proper device matching, and additionally an acceptable temperature gradient on the chip surface. By using basic matching techniques several thermal feedback effects (e.g. the offset voltage changes of differential input stages) can be largely avoided.

For these reasons proper dissipation map has to be determined simultaneously during the simulations, in order to get more appropriate results about the near-real operation of the investigated circuits. The simulated temperature gradient map on an LDO circuit using a pre-defined layout arrangement can be seen in Figure 1. The main heater element is a relatively large pass-transistor divided to several smaller parallel sections. The temperature sensitive elements are the current mirror and the differential input stage.

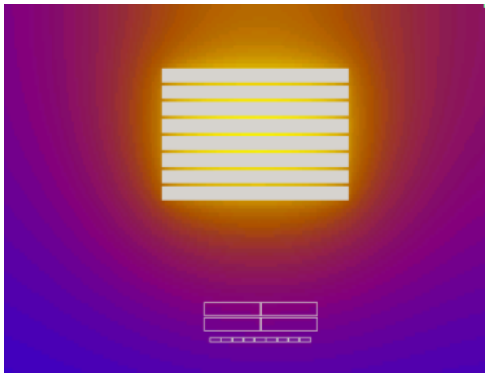

Figure 1 – Simulated temperature gradient on the LDO chip surface

2. APPLIED METHODOLOGY

There are two methods for solving electro-thermal problems. Most of the publications present the transistor level simulation by using SPICE or similar circuit simulators and an additional thermal simulator, which is usually a FEM program (e.g. ANSYS). These simulators are connected in an iteration loop where one simulator uses the updated results of the other simulator in the iterative process. The method is called the relaxation method [1]. This method has an advantage in the implementation. It takes advantage of existing electrical and thermal simulators without the need to modify them. The drawback of this method is that the iterative loop is not optimal. Only weak thermal coupling and slow changes can be investigated.

In our study we used electro-thermal simulator called SISSI (Simulator for Integrated Structures by Simultaneous Iteration), which applies another method for solving electro-thermal problems [2]. This tool uses simultaneous iteration method for solving electro-thermal problems [3]. The main advantage is that iterative solution takes place simultaneously for the thermal and electrical networks. Therefore fast changes, fast transients and strong thermal coupling can be simulated and investigated. The only drawback is the relatively more complex implementation.

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In SISSI, the thermal network is represented as an electrical network. The electrical "only" network consists of different thermally dependent electrical devices, which include thermal nodes beside the electrical nodes. The models of different devices have several parameters, which are influenced by the temperature, generated by self-dissipation of the active elements on the chip-surface itself during normal operation.

For example, one of the temperature depended parameter is the current of an ideal diode characteristics influenced by the thermal voltage $U_T = kT/q$.

If we add an additional node to the device model, of which voltage represents the actual temperature of the device and its current, means the heat current of this node could be the common point for the two networks. This thermal node represents the connection between the electrical and thermal network represented by its electrical model network (Fig. 2). Therefore the ideal diode characteristics depend on the device temperature T, which is moreover proportional to the 'voltage' value of the thermal node.

For these reasons device model with additional thermal nodes (electro-thermal device model) and simulator tool, which can handle and calculate with this device models, are needed to generate joint solution of the electrical and thermal parts of the investigated structure. This means, that the spice device model routines had to be rewritten, retaining the original electrical only model as much as possible.

Additionally, the thermal behavior of the chip and package structures is needed to allow them to be linked with the electrical solution algorithm. They should also be compact enough to provide a reasonably fast solution. The thermal model appears in the form of an electrical circuit, where electrical resistances and capacitances model the thermal resistances and capacitances, current models the heat flow and the voltage values represent the temperatures [4].

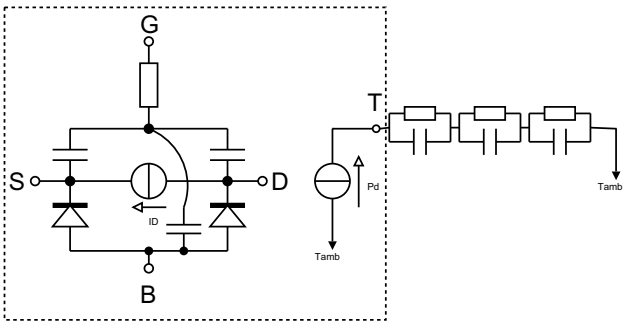

Figure 2 – The electro-thermal MOS model

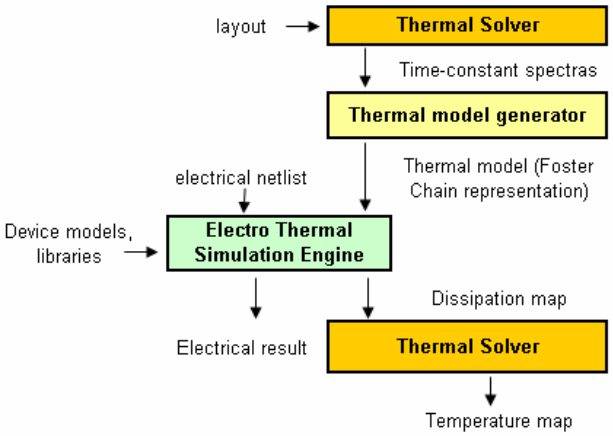

Figure 3 – Electro-thermal simulation steps

First of all, the network model, which represents the thermal properties of the structure, has to be generated. The first possibility is building a lumped RC model for the thermal structure, using the finite difference method and to solve the *electrical circuit* and the *electrical model of the thermal structure* together. The appropriate modeling of the thermal part requires a very fine discretization, which means a very high number of nodes in the model network. Therefore – because of the increased solving time – the best way is to build *compact models* of the thermal subsystem. The Network Identification by Deconvolution (NID) method was used to generate the exact compact model of the thermal network [5].

Accordingly the representation of the dynamic thermal behavior of the chip and package thermal system by an N×N matrix of Foster RC chains were determined, where N is the number of the coupling thermal nodes. For each thermal node the discretized time constant spectrum were calculated by thermal simulation, and from these spectrums, the correspondent foster equivalent chains were obtained.

3. THE INVESTIGATED CIRCUIT AND STRUCTURE

In the past importance of thermal feedback has been mainly liked to relatively high power circuits such as high current regulators, high power amplifiers [6][7] or SOI structures [8]. In these circuits thermal feedback has normally been considered an unwanted phenomenon, of which effects should be minimized if possible.

With availability of advanced circuit simulators that take thermal effects into account, such as SISSI, these interactions can however be also benefited from. One possibility is to improve low frequency accuracy of amplifiers or LDO regulators by applying small amount

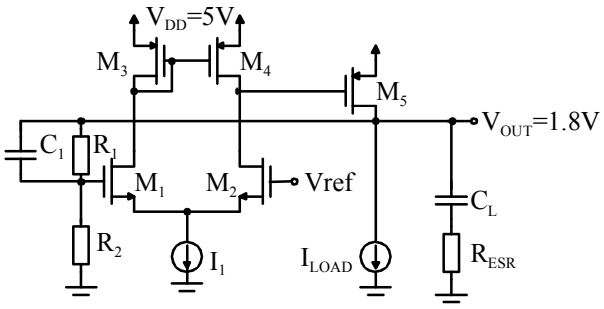

Figure 4 – Schematic of a simple LDO regulator

of positive thermal feedback to the investigated circuit. A very simple example of such circuit is the amplifier of Fig. 4. connected as linear regulator.

In absence of thermal interactions systematic offset of Fig. 4. is zero only when the current mirror M3-M4 has unity current transfer characteristics. Because V_{DS} of M4 affects the current mirror mirroring-ratio, this offset can be zero only with one output current level. In regulators, this output voltage dependency on output current is characterized by a term load regulation. Usual solution to this problem is to increase DC gain of the regulator, but an alternative solution takes advantage of positive thermal feedback.

By placing the input transistor M1 and/or the current mirror transistor M4 of Fig. 4. closer to the dissipating pass transistor M5, see Figs 1. and 4., we can create a small amount of positive thermal feedback that opposes changes in output voltage at high current levels. If M2 is placed closer to the dissipating device we can see opposite effect as shown later in section 4.

Because thermal gradients depend on distance in an exponential fashion, the actual power level (chip temperature) is less important than placement of transistors on different isotherms. The actual distance from the dissipating element simply sets the power level at which the thermal interactions start to have effect on a chip's performance.

4. RESULTS

A simple LDO regulator of Fig. 4. was simulated using SISSI with and without thermal interactions. Regulator was biased from 5V supply and had an output voltage of 1.8V. The used DIL package model consisted of silicon, solder compound and ceramic layers. Only input stage transistors were placed on different isotherms. Resulting systematic offset as a function of load current is shown in Fig. 5.

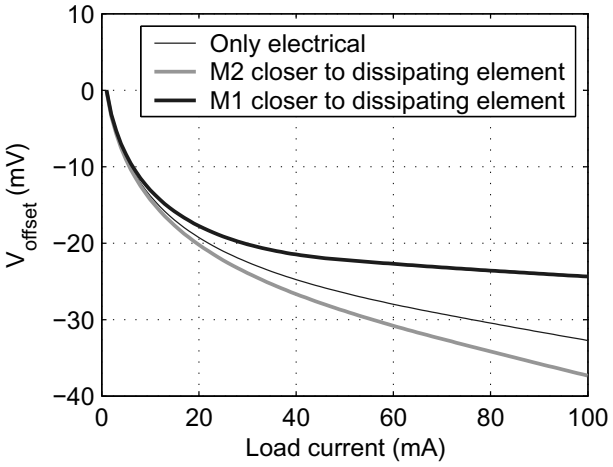

Figure 5 – Systematic offset as a function of load current

Clearly visible from the figure is that the proper placing of input stage transistors (M1 closer to the dissipating device) can significantly improve the DC performance of a simple regulator.

Response of the simulated circuit to a 50mA load current step is shown in Fig. 6. From the figure it can be seen that the positive thermal feedback affects also transient response. However as long as the system is well compensated and the bandwidth of the electrical network is much faster than the bandwidth of the thermally active transistors, applied positive feedback causes minor problems.

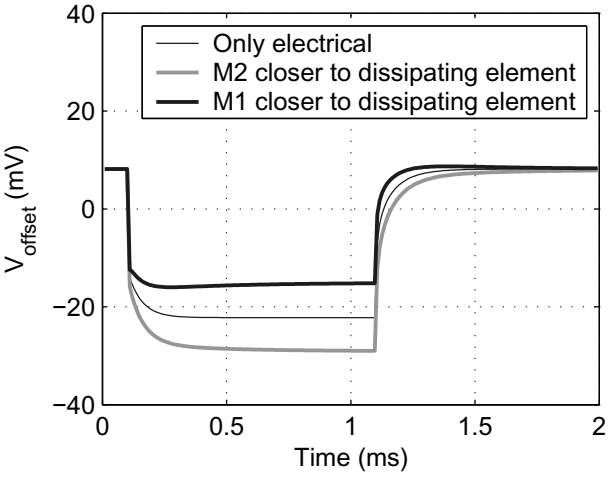

Figure 6 – Output voltage response to 50mA load current step

5. SUMMARY

This paper demonstrated how the electro–thermal simulator can be used in circuit design to optimize chip layout. Simulations of a simple LDO regulator demonstrated how proper application of positive thermal feedback could be used to significantly improve low frequency performance of LDO regulators.

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