3D ASSEMBLY TECHNOLOGY FOR HYBRID INTEGRATION OF HETEROGENOUS DEVICES

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3D ASSEMBLY TECHNOLOGY FOR HYBRID INTEGRATION OF HETEROGENOUS DEVICES

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ABSTRACT

For heterogeneous chip technologies (Power/Signal, Electronics/MEMS, CMOS/III-V´s, ...) the three dimensional integration of hybrid assembled chips is a viable approach to overcome the issues encountered here. Especially when the interconnects become very dense (high I/O´s) or signal voltages from chip to chip are vastly different, a non-ohmic contact via capacitive coupling can be a solution to overcome this issue.

Submicron accuracies in the z-direction and low-micron accuracies in x/y are required to fulfill the needs of such a capacitive contact for 8x8µm^2 sized pad arrays. The authors have successfully developed a chip, the interconnect scheme and the assembly process that allows the capacitive coupling of high I/O chips for electronic, MEMS and heterogeneous hybrid devices. The 3D Chip Stack was afterwards assembled on a test PCB with through via wirebonding. Envisioned concept shows the use of backside contacts e.g. PWR/GND/CLK for the top chip to be realized by integrated through via chip manufacturing as used in MEMS/MOEMS technology

1. INTRODUCTION

3D Integration is becoming an important technology for future system implementation. A number of solutions for vertical interconnection has been proposed, particularly concerning wireless inter-chip connections. Contact-less communication is a strategic technology for the realization of high-performance vertical links: without an ohmic connection between the two chips, ESD protections could be omitted, reducing parasitics and improving overall performance.
The main strategies described so far are:

- Interconnections based on inductive coupling [1], [2]
- ohmic coupling [3]
- and capacitive coupling [4], [5], [6], [7]

The former approach presents good performance and a great advantage in terms of packaging: chips are stacked and aligned face-up, avoiding more critical manipulations. With current controlled communication, the transmission power can be tuned in order to deal with assembly issues. On the other hand, the capacitive approach optimizes interconnection performance and area if a high-precision face-to-face assembly is available. This communication approach is the one adopted in this work, allowing a bandwidth density enhancement of calculated 6.35Mbps/µm^2 to 14Mbps/µm^2, while reducing the needed power by one order of magnitude [8]. Combining chip design and high precision assembly technology, these features are achievable.

Furthermore, with this hybrid assembly approach, complex MEMS devices can be realized by merging the electronic functionality of a read-out chip with a wafer level protected [9] MEMS functionality. Here, either capacitive coupling or ohmic coupling are favorites.

The envisioned capacitive coupling using 3D assembly technology is sketched in [Figure 1]

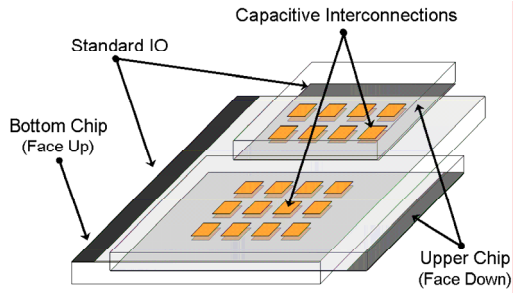

Figure 1: Schematic of capacitively coupled massively parallel chip-to-chip interconnects

where chips are stacked face-to-face in a two level structure. Electrodes, in the upper metal layer of each device, realize the capacitive coupling necessary for communication.

This work describes a capacitive 3D assembly using 0.13µm CMOS implementation, the assembly process and measurement results of such a massive parallel interface concept.

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In order to achieve such a massive parallelism, contact pitches and respective pad sizes must be small. Essentially, to minimize crosstalk between two adjacent chip contacts and to maximize the coupling efficiency, the gap between the contacts should be as small as possible, preferably close to zero.
Finally, the 3D chip assembly is mounted in a prototyping technology to a test board for easy contacting to a motherboard connected to an external test apparatus

2. REALIZATION OF CHIP-CHIP INTERCONNECT

The chips were obtained from a 300mm multi project wafer manufactured in a 0.13um CMOS technology. The chips have arrays of capacitive contacts from 8, 15 and 25µm in size, with respective double contact pitches. To facilitate the semi automated alignment process, alignment marks were also structured to the final metal layer.
Initially, the chips had a 0.7µm thick passivation layer, that in later trials was omitted in the area of the capacitive pads.
For bonding, obviously both chips needed to have a symmetric arrangement of the contact pads. [Figure 2] shows the overlay image of the CAD file and its mirror, depicting the final assembly situation. In the overlapped area, the contact pads are positioned above each other. The non-symmetry of the chip allows now to contact the AlSi1% bond pads from the smaller sides of the IC, face up for the bottom chip, face down for the top chip.

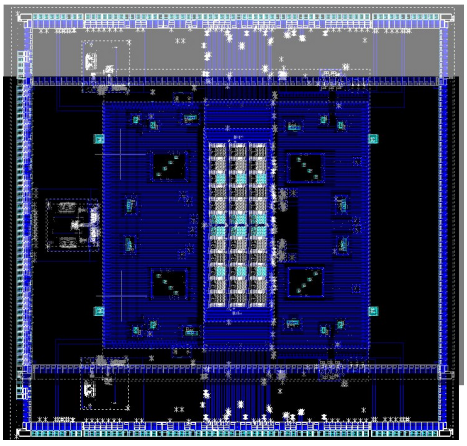

Figure 2: Overlay image of mirrored CAD design

Bonding was performed using a FC150 flip chip bonder manufactured by Karl Suss. The system allows a nominal accuracy of 0.5µm in x and y. Z-axis control is not in the same level of precision therefore other means of gap control were conceptualized. Thus, the process was designed to be self limiting in z-direction by using viscosity induced gap limitation of an adhesive dielectric

For a given precise applied pressure to two parallel plates, the flow resistance of a fluid with viscosity η (i.e. the displacement of a given volume) in a small gap increases according to equation [Eq. 1], thereby allowing a good control of the final gap in the range ~1µm. This depicts that there is a relation of the flow rate dV/dt, giving a correlation to D^4 in order to decrease the gap size while increasing the applied pressure p:

$$\frac{dV}{dt} \sim \frac{D^4}{\eta} p$$

Eq. 1: Viscous flow in a gap /10/; D: gapsize, η: viscosity, p: applied pressure

For a high precision in z-axis, it is paramount to have

- clean, particle free chips
- an adhesive with excellent reproducibility in viscosity
- fast cure, zero-outgassing adhesive material

Material selection needed also to take into account that a subsequent process step involves a 120°C wirebonding process. For the prototoype assemblies, material selection did not need to take e.g. multiple soldering processes into account. A Loctite 4204 acrylate adhesivewas selected to suit these needs. In first realizations, silicon monitor chips were assembled to optimize the required bond pressure to a value of 5kgf over the chip area of 5,1x4,3mm^2. With this approach, the prototype chips were assembled.
Prior to bonding, the chips were immersed in IPA, then in distilled water. Clean nitrogen was used to remove any particles and the fluid, leaving only an absorption layer of H_2O required to catalyze the bonding process.
As for the assembly of the prototype chips, we aligned first the alignment marks to achieve a ~5µm accuracy. Then, magnification was increased, focusing on individual pads of 5µm size and iteratively optimizing the alignment by shifting the movable substrate table in x/y and theta to the final accuracy target of ~1µm.

After alignment was finished, a precise volume of the acrylate adhesive was dispensed on the bond area. Due to expected tolerances in the dispensing process, the initial chip design took under- and over-dispensing into account. While under-dispensed volume would likely result in a non-critical reduction of bonded area, not affecting the capacitive coupling, over-dispensing too much might result in the contamination of the bond pads. In order to minimize this, a 100µm wide overflow area was designed into the chip. Thus, volume variations of up to 100% could be tolerated [Figure 3]

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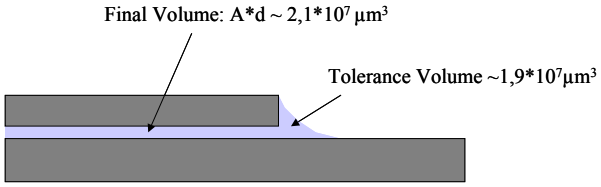

Figure 3: Tolerated volume variation

Figure 4 shows an image of an assembled 3D Chip to Chip stack and the SEM close-up to the bonded interface, showing also the bond pads of one of the chips

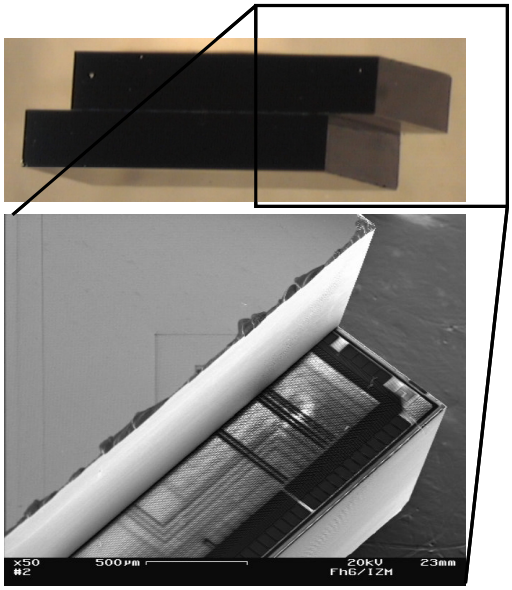

Figure 4: Chip-Chip Assembly

Cross sections of the resulting assemblies showed, that distances in z-direction of 0,7…1,4µm can be achieved. Lateral x/y accuracy in the range of 1µm were reproducibly shown [both: see Figure 5]. A grid of the passivation topography was helpful to determine this, as preparation of such minimal structures are difficult.

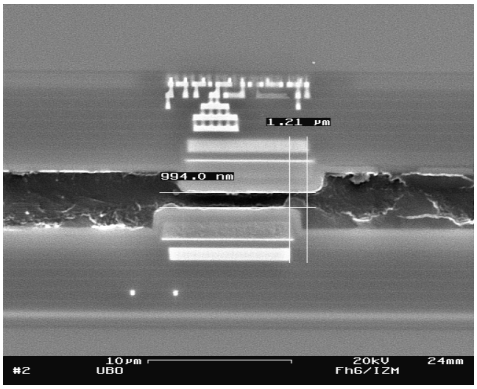

Figure 5: cross section of aligned structure

3. REALIZATION OF CHIP-PCB INTERCONNECT

With the prototype chips, bond pads were present on both sides of the chip. Thus, a non conventional approach to interconnect both sides had to be found. The bonding concept is given in [Figure 6]. To achieve this, a special PCB design with a milled-out trench had to be realized [Figure 7].

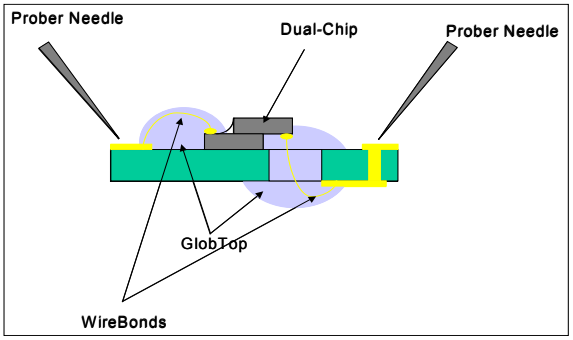

Figure 6: Concept of wirebond assembly of 3D Chip-Chip Stack, indicating prober needles for preliminary testing

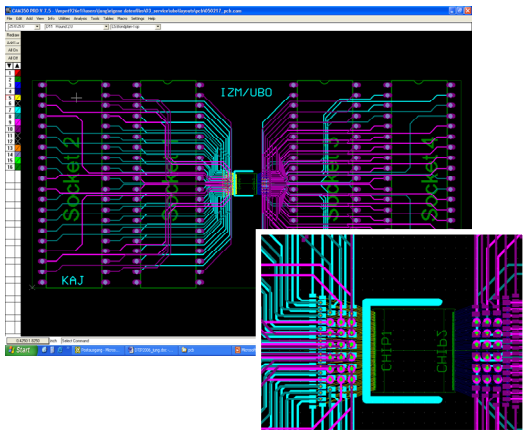

Figure 7: PCB design and close up of chip attach area

The high number of I/O´s required a four layer multilayer substrate with 100µm lines/spaces design and a final metallization of bondable Ni-Au. As the pads were closely spaced, Al wedge-wedge bonding was selected as optimum bond technology.
Firstly, the chips were die-attached to the substrate using an epoxy adhesive. Then the first (bottom) chip was bonded in a conventional fashion and then protected by a partial glob top encapsulation to prevent wire sweep during the final glob topping [Figure 8].

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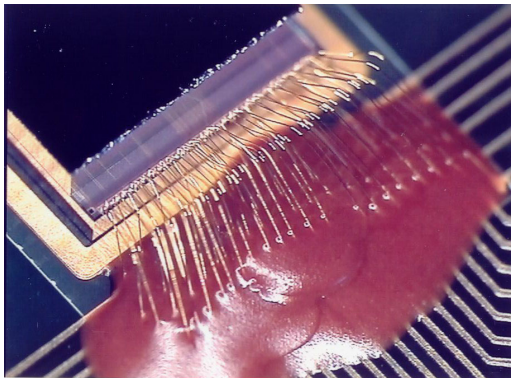

Figure 8: Bottom Chip wirebond and part-encapsulation

Secondly, the PCB was turned upside down in a holder with a cavity and the top chip was bonded through the milled cavity. Prior to final glob top encapsulation, the wirebonds were part-encapsulated to prevent any void entrapment in the ~1mm thick cavity [Figure 9]. Adhesive assembly of a polymer lid was identified as alternative to glob topping.

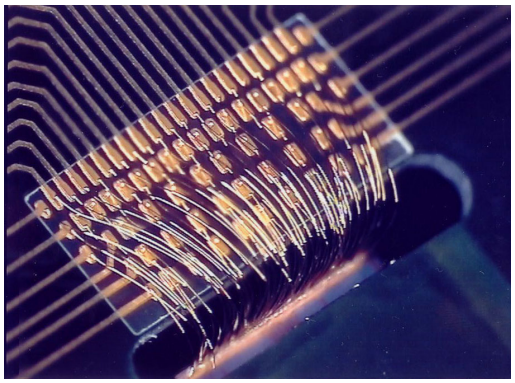

Figure 9: Wirebonds through the milled trench of PCB

4. MEASUREMENT RESULTS

On these PCBs multi pin connectors were assembled by soldering technique to fit onto a generic test bench. Here, measurements were done to identify the performance of the 3D chip/chip stacks.

The observed power consumption for a signal transmission was seen to be similar for the different bond pad sizes 8µm, 15µm and 25µm, increasing from about 30µW @ 10 MHz to about 110µW at 1GHz [see Figure 10].

Analyzing the wave forms of transmitted and received signals, the received signal provides good discrimination against the signal threshold, thereby indicating that the signal has been successfully transmitted over the capacitively coupled pads [Figure 11].

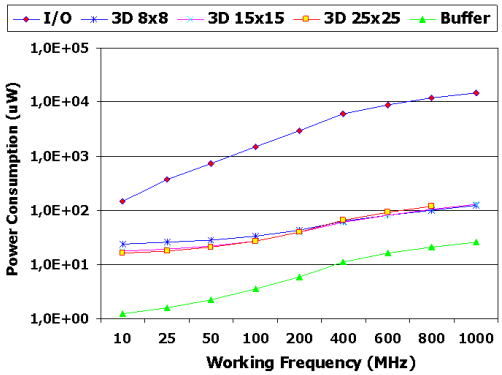

Figure 10: Power Consumption of transmitted signal according to capacitive pad size

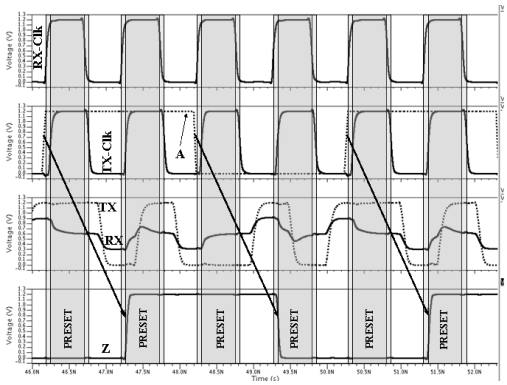

Figure 11: Transmitted signal wave form between transmission (TX) and reception (RX)

5. OUTLOOK

As a result from the first prototypes, three major advancements are identified for further progress:

1) passivation-less chips with internal copper interconnects
2) Low temperature plasma assisted silicon direct bonding [11] of the chips to minimize the gap even lower
3) Through-vias to the backside of the chip to provide power and clock directly [12], omitting the need for a trenched PCB

Especially the latter will enable a manufacturing capable solution to this innovative 3D chip/chip stacking using capacitively coupled interconnects, as the dice can be directly mounted to the "receiving" chips while still being non-singulated on their wafer and allowing conventional wirebonding in standard packages to take place at minimum extra effort.

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6. CONCLUSION

A high precision 3D assembly technique was employed to realize prototypes of capacitively coupled interconnects for future ultra wide band chip-to-chip interconnects.
Adhesive bonding was used to achieve ~1µm alignment in x/y and z direction. Interconnect of the chip stack to a PCB was performed through a milled trench of a multilayer interposer substrate, connecting this to a testbench via multipin connectors. Measurement results demonstrate the feasibility of the coupling concept and its advantages with respect to power handling and signal delay time.
The demonstrated technology lends itself for hetero system integration of electronic, MEMS and bio-systems, as high data transmission rates without the need for ohmic contacts were demonstrated together with a technology suitable for volume component-to-wafer assembly. Adhesive or adhesive-less techniques can be selected for the mechanical high precision mounting of the respective hetero-components.

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