On the Extraction of PiN Diode Design Parameters for Validation of Integrated Power Converter Design

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***Abstract*—Design of integrated power systems requires prototype-less approaches. Accurate simulations are necessary for analysis and verification purposes. Simulation relies on component models and associated parameters. The paper focuses on a step-by-step extraction procedure for the design parameters of a one-dimensional finite-element-method (FEM) model of the PiN diode. The design parameters are also available for diverse physics-based analytical models. The PiN diode remains a complex device to model particularly during switching transients. The paper demonstrates that a simple FEM model may be considered unknowingly of the device exact technology. Heterogeneous simulation is illustrated. The state-of-art of parameter extraction methods is briefly recalled. The proposed procedure is detailed. The diode model and extracted parameters are systematically validated from electro-thermal point-of-view. Validity domains are discussed.**

***Index Terms*—Finite-element-method (FEM), PiN diode.**

I. Introduction

In [1], are detailed some issues related to the integration of power electronic systems. The design issue is discussed and authors propose a tentative design flow [2]. Hybrid technologies and moreover monolithic technologies call for prototype-less design. Particularly integrated power systems render practical measurements difficult if not impossible. Then the design flow of such integrated systems becomes the key to success. This design flow includes several steps from functional design to physical verification and validation. This last step should provide accurate estimation of the system behavior as measurements provide todays with system prototypes. The simulation accuracy depends on the accuracy and the validity of the various components models. Particularly the semiconductor device model validity depends on the model equations but also on the model parameters. These parameters should be extracted accurately for the model to represent physical devices. Most models are based on physical approach, hence they depend on the device design parameters. An important step is thus related to the extraction of device design parameters. This latter issue has not been extensively discussed in literature though it is as important as the model equations themselves. The paper details a systematic procedure to extract the main design parameters of a PiN diode. The PiN diode remains a difficult device to model, particularly during switching transients.

The extraction of a design parameter can be performed directly from an electrical characteristic or from a more elaborate method. The threshold gate voltage of a MOSFET transistor is extracted easily from a I_{DS}-V_{GS} static curve for example. Unfortunately this technique is not possible for any device design parameter. It is more convenient to extract design parameters from an optimization process based on adequate experimental data. Such an extraction procedure requires at least five actions as introduced in [3]

1) choice of a device model and a related simulator;
2) definition of a circuit model similar to experimental setup;
3) production of experimental data and collection of other input data;
4) definition of a quality criterion, namely a cost function;
5) adoption of an optimization procedure;
6) validation of the optimal parameter set.

The optimization procedure takes the experimental and simulation data, computes the cost function and tunes the design parameter set to minimize the cost function. When the optimum is obtained, the simulation results are quite comparable to experimental data, and an optimal design parameter set is available. The three first steps as defined here above are now briefly recalled for the sake of place.

A. PiN Diode Model

Many PiN diode models are reported in literature. [4] or [5] classifies models developed until 1998. Other models are reported in [6] and [7]. Particularly models reported in [6] are declared accurate but they include parameters difficult to extract from author point of view. In [8] it is shown that the standard Spice model is not convenient to represent a PiN diode. The Spice model does not consider the high-injection phenomenon that takes place in the diode epitaxial base for example. As reported in [4] many models include the high-level injection phenomenon as [9], [10] which are the initiative developments for the Saber diode model [11]. Literature also reports equivalent circuit model of the lumped-charge model in the diode base [7], [12]. However this technique to produce Spice compatible models offers no advantage over state-space models [13], [14].

As indicated here above, the parameter extraction process is necessary for the accurate system simulation which will be carried out during the final verification phase inside an integrated system design flow. Probably finite-element method (FEM) modeling should be considered for this verification

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phase, within an heterogeneous simulation scheme. A circuit representation is sufficient for several parts of the system like will be shown for the circuit parasitic components. FEM models suit complicated components like power semiconductor components or magnetic devices. A FEM model is considered here for the PiN diode. Unfortunately the technological architecture of the semiconductor device is generally not available, and the paper demonstrates that a simplified and quite arbitrary technological architecture may be considered. However the reader may object immediately that FEM modeling enables complex technological representation for the PiN diode. First of all the paper focuses on a design parameter extraction method. For the sake of clearness, a simple generic doping profile is adopted for the diode but the essential design parameters of any doping profile are considered. Moreover FEM models are not the only ones suitable for the verification phase inside an integrated system design flow. Several physics-based analytical models may be considered. These models require the design parameters considered in the paper. Finally the diode technological architecture is not available to end-users. A visual inspection of bare dies gives only access to the estimation of the device area. The main difference between diodes of diverse manufacturers are on the doping profile. The proposed generic doping profile is unique while many options are considered by manufacturers to optimize the doping profile of their devices. From modeling point of view there is a trade-off between the level of complexity of the doping profile, the number of design parameters to extract and the gain in model accuracy. This trade-off and limitations of the presented approach are discussed in the last section.

The arbitrary 1-D technological architecture in Fig. 1 is considered for the PiN diode. This architecture is very simple as a uniform base is considered. The P^+ and N^+ regions have secondary effects on the diode transient behavior except at very high current level where the lateral regions control the carrier injection [15]. The N^+ region is involved during hard diode turn-offs. So the P^+ and N^+ region parameters are not identified in a first approach. The following values are set arbitrarily $X_{jP} = 16\ \mu$m, $P^+ = 10^{20}$ cm^{-3}, $X_{jN} = 45\ \mu$m and $N^+ = 10^{20}$ cm^{-3}. These values are of the same order as those of commercial device technologies. The parameter extraction procedure addresses the diode base width, W_D (μm), the diode base doping concentration, N_D (cm^{-3}), the ambipolar life-time in the diode base, τ (s), and the device effective area, A (mm^2).

The architecture in Fig. 1 is entered using the graphical tool MDraw by ISE [16]. An automatic meshing tool produces the necessary data for the FEM simulator Dessis [17]. The input file contains no numerical values for the above mentioned design parameters. These values are entered while performing the parameter extraction procedure. Similar results may be obtained using other FEM softwares like [18].

Dessis software supports heterogeneous simulation. The circuit considered experimentally and for simulation includes numerous components. All of them are simulated as equivalent circuit models except the PiN diode.

B. Circuit Model

The experimental circuit is pictured in Fig. 2. A MOSFET transistor/diode switching cell is implemented. The diode package is inserted at the end of a simplistic bus-bar. Varying

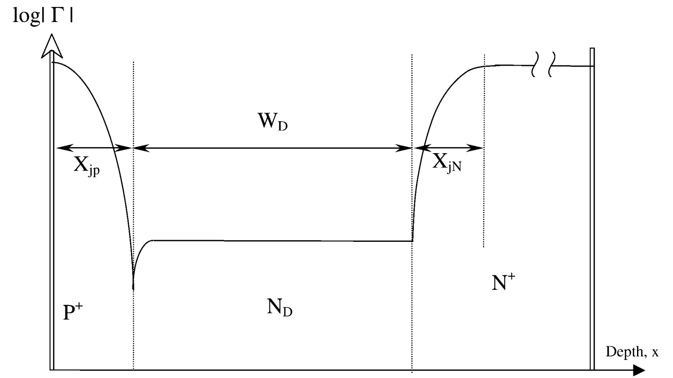

Fig. 1. Simplified 1-D architecture for the PiN diode.

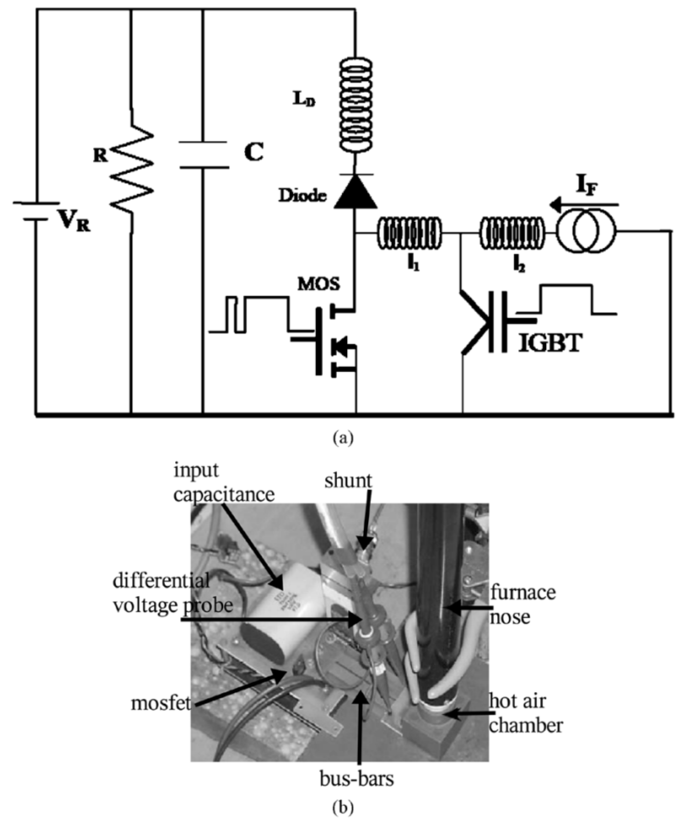

Fig. 2. Experimental circuit for the diode design parameter extraction. (a) Schematic. (b) Picture (IGBT transistor not included).

the length of the bus-bar changes the value of the wiring parasitic inductance, L_D. A current shunt is inserted in series with the diode. The shunt is a TMS Research device 0.025 Ω/1.2 GHz [19] or an experimental current sensor [20]. This shunt imposes a reference voltage at the high potential of the V_R source. Two voltage probes, Tektronix P6139A [21], [22], are connected in a differential manner to the diode. The differential setup features a 400-MHz bandwidth. A hot air furnace is used to control the temperature of the diode under test.

The switching cell main operating conditions are the forward current, I_F, and the reverse voltage, V_R. These conditions are imposed by a current and a voltage source respectively. It is required to extract the diode design parameters at a controlled temperature from experiment point of view. Hence it is necessary to limit diode self-heating by using a low recurrence

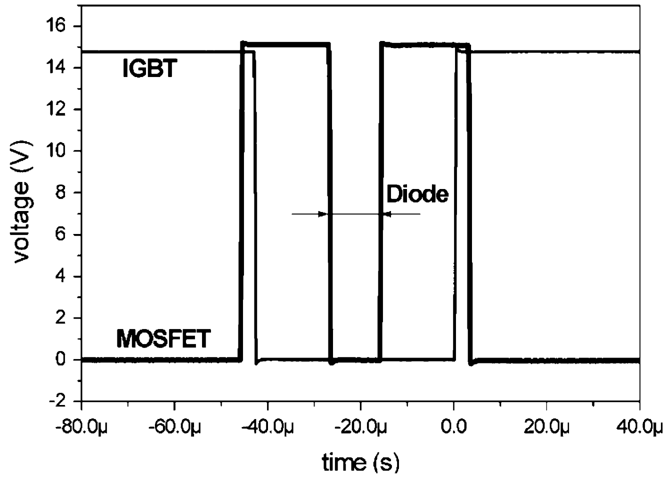

Fig. 3. Experimental control signal for the transistors in the circuit in Fig. 2(a).

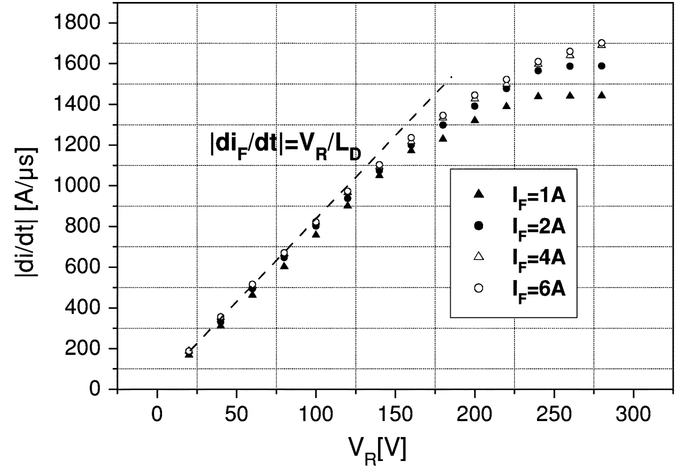

Fig. 4. Experimental diode current slope during turn-off in the experimental circuit.

operation. An IGBT transistor (MUP304) is added [Fig. 2(a)] that shorts the current source most of the time (Fig. 3). The IGBT transistor is turned-off only several tens of microseconds every hundreds of milliseconds. The MOSFET transistor is turned-on just before the IGBT transistor is turned-off. Then it operates a diode turn-on and turn-off, before the IGBT transistor is turned-on. The inductor, l_2, is a small wide-bandwidth air inductor that insures a constant current during the switching cell operation. A similar inductor of smaller value, l_1, disconnects the IGBT from the switching cell during transients of the switching cell, when the IGBT is in the off state.

From simulation point of view, the IGBT transistor is not necessary as it does not influence the switching cell behavior inside the experimental circuit. The MOSFET model is based on the classical Spice Level-3 Mosfet model, available in major circuit simulators. The model parameters for the IRF740 device are also available in major circuit simulators.

The experimental data are captured during the diode reverse recovery as detailed here after.

Textbooks [23], [24] detail that the diode current slope is approximated by $di/dt = -V_R/L_D$ at beginning of reverse recovery, inside a switching cell circuit where a unique wiring parasitic inductance is considered. Unfortunately experiment contradicts this assumption with the circuit in Fig. 2(a). Fig. 4 pictures the diode current slope during turn-off versus the reverse voltage, V_R and for several values of I_F. Obviously Fig. 4 shows that the $di/dt = -V_R/L_D$ approximation is not valid when V_R increases. The same discrepancy appears with respect to I_F. A model of the wiring parasitics is required. Of course during the validation phase of a power system, a complete model of the wiring parasitics would be necessarily available. Fig. 4 demonstrates the necessity of a pertinent wiring parasitic model to achieve accurate simulation at semiconductor level.

A wiring parasitic model of the experimental circuit is obtained using the commercial software InCA [25]. The PEEC method [26], [27] is applied to the printed circuit board in Fig. 5(a) and an inductance matrix is obtained. In Fig. 5(b) inductors, $l_{\rm dio1}$ and $l_{\rm dio2}$, account for the diode package internal wiring inductors. The shunt internal parasitic inductor, $l_{\rm sh}$, is non measurable and no coupling has been considered with other inductors. For numerical purpose, $l_{\rm sh}$ is set to 1 pH during

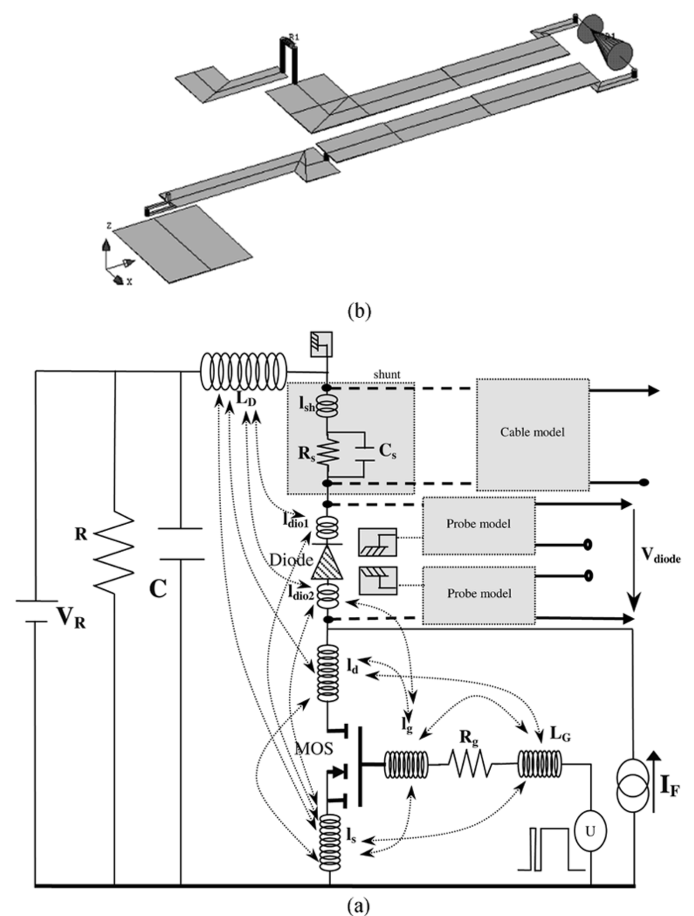

Fig. 5. Circuit model including a parasitic wiring model and probe models. (a) Printed circuit board. (b) Parasitic wiring model and probes location.

simulation. An inductance matrix is computed for each bus-bar used to support the diode.

Probe models are also considered to produce simulation results as closed as possible to experiment. These probe models have been detailed in [28]. The probe models represent the input impedance, the delay and the distortions introduced by the probes. Effects of these probe models are illustrated in following sections.

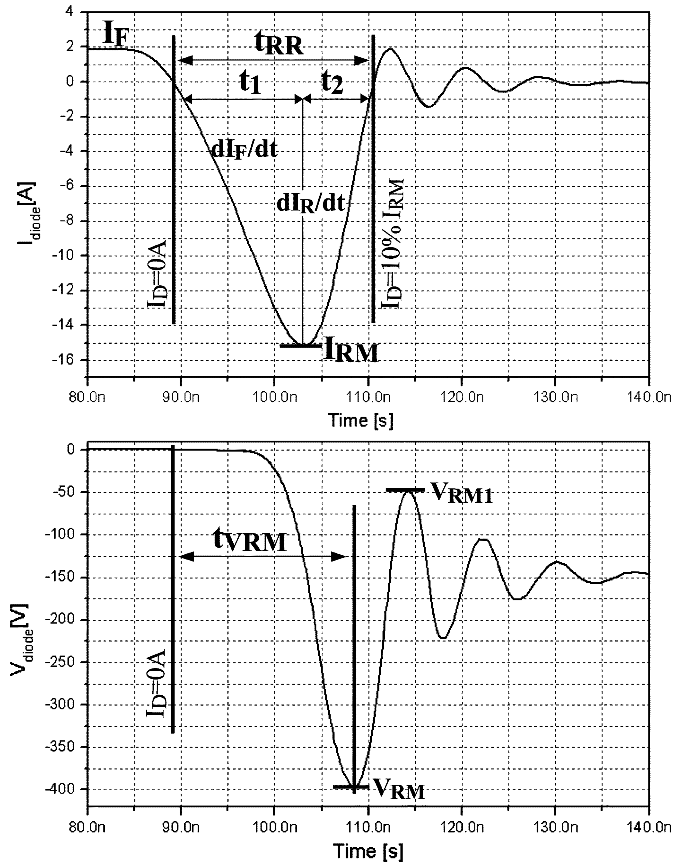

Fig. 6. Definition of main diode turn-off switching parameters based on current and voltage waveforms.

C. Experimental Data

Fig. 6 depicts a diode turn-off. Oscillations appear at the end of the turn-off. This part of the diode turn-off is difficult to model. It requires a very accurate description of the diode, an accurate description of the circuit wiring and a satisfying representation of the probes. Particularly the voltage probe input capacitance interacts with the diode under test, as pictured in Fig. 10. Experiment and simulation differ in terms of oscillation amplitude and phase. On a general basis it is not suitable to use directly waveforms to confront simulation and experimental results within the design parameter extraction method. If waveforms seem correct after the parameter extraction, it is not the case at the beginning of the procedure. It is then preferable to characterize the turn-off waveforms by so-called switching parameters (see Fig. 6). These switching parameters are extracted both from simulation and experimental results, and used for the extraction procedure. Additional data will come from manufacturer data sheets as current and voltage ratings.

The previous sections have recalled the three first actions involved in design parameter extraction. Next section details a step-by-step extraction procedure. Then the validity of extracted design parameters is discussed from electro-thermal point of view. Several simplifications have been considered so far. The validation section then discusses the possible limitations of the extraction procedure from simulation point of view.

II. Step-by-Step Extraction Procedure

Probably ICCAP [29] is the most popular system to extract model parameters in Microelectronics. ICCAP uses static I–V characteristics and C–V curves. Small biasing conditions are involved. Unfortunately these operating conditions are not sufficient to stimulate physical phenomena like high-level injection inside the PiN diode. I–V and C–V curves are not significantly influenced by the important phenomena involved inside the diode during hard switching like dynamic avalanche [30], [31], or Kirk effect [32] like in a bipolar transistor collector. Dynamic avalanche is referred to as a cause of diode failure [33], hence the necessity to render the experimental data sensitive to this latter phenomenon. Finally I–V characteristics are related to the ambipolar lifetime in the diode epitaxial layer only through the device voltage drop. This quantity reveals insufficient to estimate the ambipolar lifetime in a satisfying manner. Then the switching parameters as defined in Fig. 6 are preferred as input data.

A global optimization procedure is detailed in [34] to extract the diode design parameters: the diode base width, W_D, the diode base doping concentration, N_D, the ambipolar life-time in the diode base, τ, and the device effective area, A. The procedure accepts switching parameters as input data. One reported limitation is the large CPU-cost due to random optimization techniques.

Other extraction techniques have been presented [35], [36]. They concern lumped-charge models where physical parameters are mixed with nonphysical quantities. The extraction procedures appear quite complicated and lead to a parameter set of limited accuracy. Moreover the validation has not been demonstrated from electro-thermal point-of-view.

More recently [37] reports a diode design parameter extraction for the model in [14]. It is a step-by-step procedure for the parameters W_D, N_D, τ and A, that uses essentially data sheet results. The effective area, A, is extracted from the normal rating forward current, I_F and the maximal current density, J. The ambipolar lifetime, τ, is extracted from the current I_F and the reverse recovery charge, Q_{RR} by $\tau = Q_{RR}/I_F$. The drift region width, W_D, is extracted from the breakdown voltage, V_{BR}, assuming an arbitrary doping concentration $N_D = 10^{14}$ cm^{-3} and an arbitrary relation between V_{BR} and W_D. Then a refinement of the parameter values is performed using one inductive load turn-off at room temperature. First the inductance value is obtained from experimental data with the relation $di/dt = -V_R/L_D$. The value L_D is fed into the circuit model. Second the ambipolar lifetime is refined using I_F and Q_{RR} experimental values until experimental and simulation current waveforms match. Third the voltage waveform is used to correct the values of W_D and N_D. The procedure detailed in [37] is closed to the procedure presented here but suffers some limitations. It is shown in introduction that one inductance is not sufficient to represent the wiring parasitic components of the experimental circuit. The ambipolar lifetime is not the only design parameter to influence I_F and Q_{RR}. The voltage waveform depends also on the ambipolar lifetime and the effective area. Finally the limited refinement of the design parameters leads to a design parameter set that enables accurate simulation results only in the vicinity of the considered experimental conditions. The authors

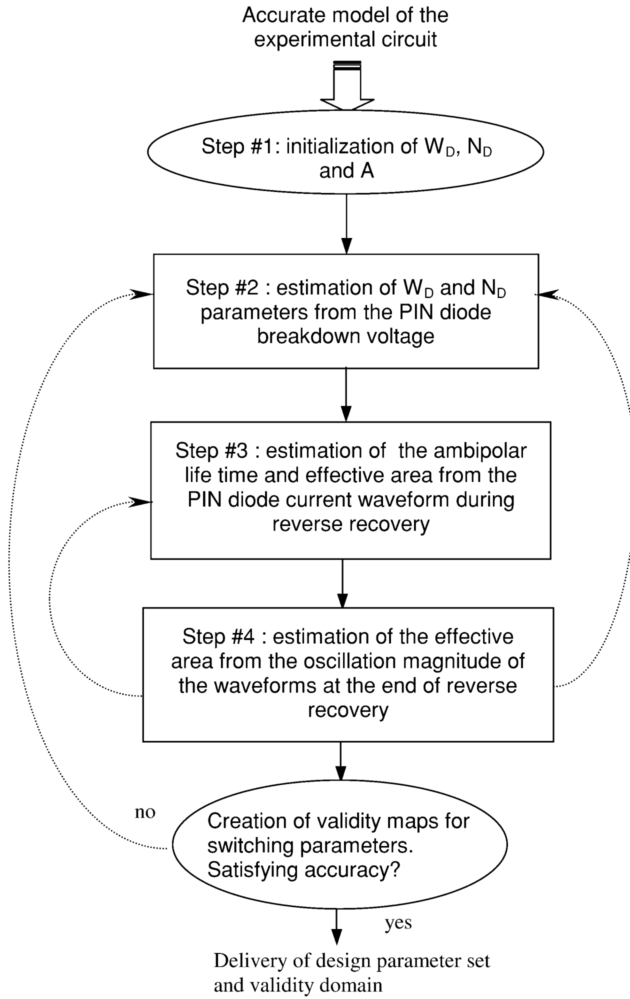

Fig. 7. Extraction procedure algorithm.

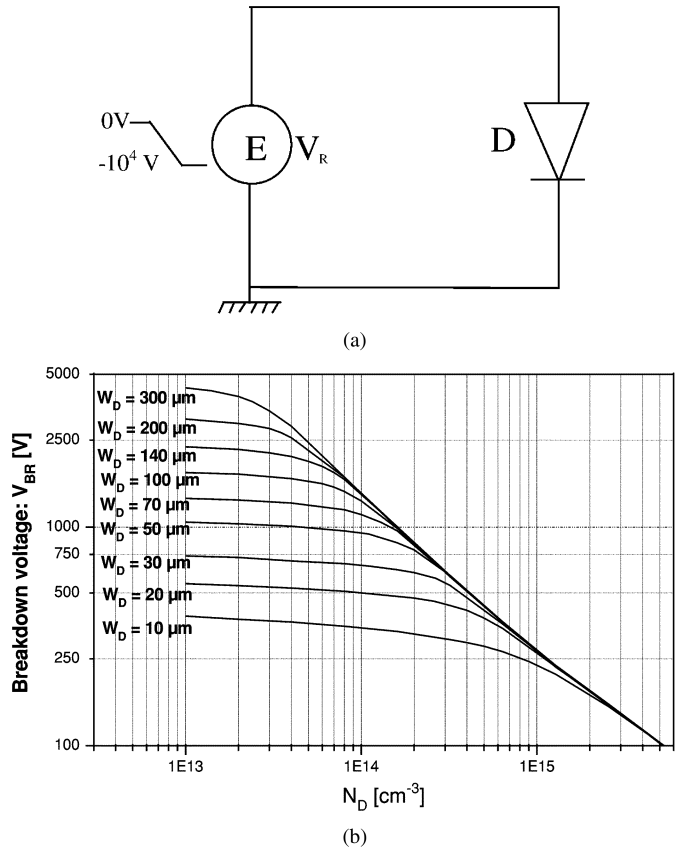

Fig. 8. (a) Simulation circuit for breakdown voltage estimation. (b) Estimated breakdown voltage using the 1-D model in Fig. 1.

detail here a step-by-step procedure which is significantly more rigorous but more expensive from CPU point-of-view. The validity of the design parameter set will be demonstrated using validity maps built on numerous diode turn-off waveforms.

Few parameters are extracted in a quite independent manner at each steps (Fig. 7). The quality of the parameter extraction may be checked at each step instead of final stage like in a global extraction procedure. Step #1 gives initial values to the diode base width, W_D, the diode base doping concentration, N_D, and the effective area, A. Step #2 refines the estimation of W_D and N_D. Step #3 gives an estimation of the ambipolar lifetime in the diode base layer, τ. Step #4 refines the estimation of the affective area, A. The "ambipolar lifetime" step is repeated after step #4 as τ depends on A. The parameters W_D and N_D are also refined again after step #4. The different steps are detailed now.

A. Step #1: Initial Values of W_d, N_d and A

It is not easy to have simultaneously a fast device with a high breakdown voltage and a low forward voltage drop. Consequently device engineers use trade-offs to satisfy the physical constraints that occur in the diode low-doped epitaxial layer. Under reverse-bias operation a space-charge region (SRC) develops in the diode drift region [38], [39]. The electric field shape is either triangular if the SRC extension remains within the epitaxial layer boundaries, or trapezoidal if the SRC tends to extend over the drift region width. When the electric field reaches a critical value, the breakdown phenomenon occurs due to impact ionization. The related voltage is called the breakdown voltage, $V_{\rm BR}$. It is considered here that the static breakdown voltage of the diode is determined mainly by the diode volume properties and not the edge terminations of the device. Edge terminations are generally optimized to approach this latter behavior [30].

The breakdown voltage is related to W_D and N_D in normally designed devices [40]. The diode model in Fig. 1 is simulated in the circuit in Fig. 8 for various values of W_D and N_D. Other parameters are set arbitrarily: $A = 1$ mm$^2, \tau = 100$ ns, $X_{jP} = 1$ μm and $X_{jN} = 45$ μm. The breakdown voltage is estimated and plotted versus W_D and N_D [Fig. 8(b)]. Simulations are carried out using the quasistationary mode of Dessis-ISE as the diode reverse-bias operation is mainly governed by the Poisson law. A trade-off for low forward voltage drop and large breakdown voltage is to set W_D and N_D so that the breakdown voltage appears in the knee region of one curve in Fig. 8(b).

The procedure considers the typical value of the device voltage rating as the breakdown voltage in the diode data sheet, and select the W_D-curve that places the breakdown voltage value in its knee region. Initial values of W_D and N_D are obtained. In the case of a bare diode die, an estimation of W_D could be possible by visual inspection. However there is no relation between the die width and W_D a priori.

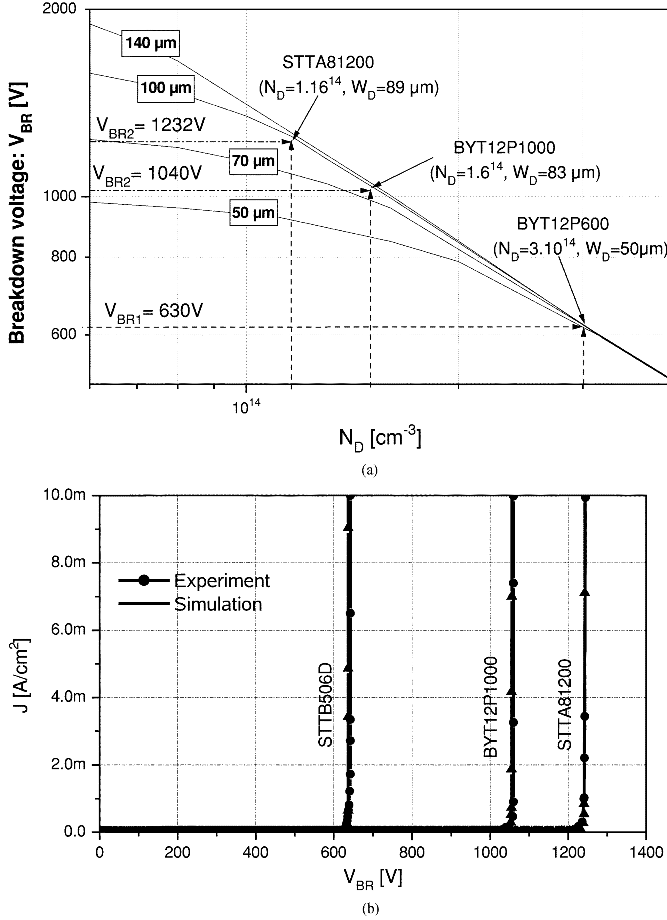

Fig. 9. Refinement of W_D and N_D based on reverse-bias I–V curve. (a) Refined values of W_D and N_D. (b) Simulated and experimental breakdown voltage for three commercial devices.

An initial value of A is obtained from the forward current rating, I_F, as indicated in the device data sheet. It is assumed a current density of 150 A/cm^2. A visual inspection of a bare diode die gives access to the contact surface, and this surface can be an initial value for A.

B. Step #2: First Refinement of W_D and N_D

The refinement is based on the reverse-bias static characteristic of the PiN diode. This I–V curve is obtained experimentally using a high-power curve tracer Tektronix 371 A. A pulse-mode and a single-sequence operation are used to limit self-heating effects. The simulation results are obtained using Dessis-ISE in quasistationary mode. Few try-and-change phases are required to obtain matching simulation and experimental curves. The procedure may be carried out manually using a dichotomic approach for example. The procedure may also be performed using optimization tools like Darwin in Model Center [41] or an Optimization Toolbox in MatLab [42]. Fig. 9 pictures results after step #2 for three commercial devices: STTA81200, BYT12P1000, and BYT12P600. These results confirm the hypothesis about the static breakdown voltage and its relation to the diode volume properties more than the device edge terminations.

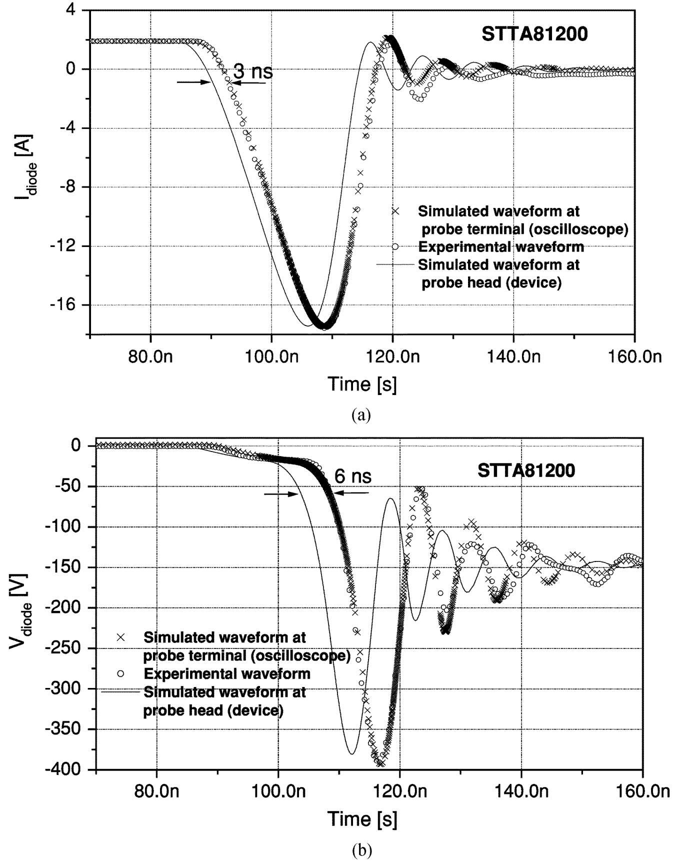

Fig. 10. Comparison of experimental and simulation waveforms with regard to probe effects. (a) Current waveforms. (b) Voltage waveforms.

TABLE I
OPTIMAL DESIGN PARAMETER SET FOR THREE COMMERCIAL DIODES

diodes	STTB506D	BYT12P1000	STTA81200
A (mm^2)	3,65	5	6
τ (ns)	260	258	208
N_D (cm^{-3})	3.10^{14}	1,5.10^{14}	1,16.10^{14}
W_D (μm)	50	83	89

TABLE II
COMPARISON OF SWITCHING PARAMETER VALUES FOR A STTB506D DIODE

	Simulation	Experiment
t_{RR} (ns)	24,3	24,5
I_{RM} (A)	-19,7	-19,5
V_{RM} (V)	-406	-415

C. Step #3: Estimation of τ and Refinement of W_D and N_D

A small forward voltage has the disadvantage of a great amount of stored carriers when the diode is highly forward biased, and high-level injection occurs in the diode base region [38]. This yields a low switching speed. Deep recombination centers are created (Au or Pt doping) in the epitaxial layer to reduce the ambipolar lifetime, τ, hence, improving the switching speed.

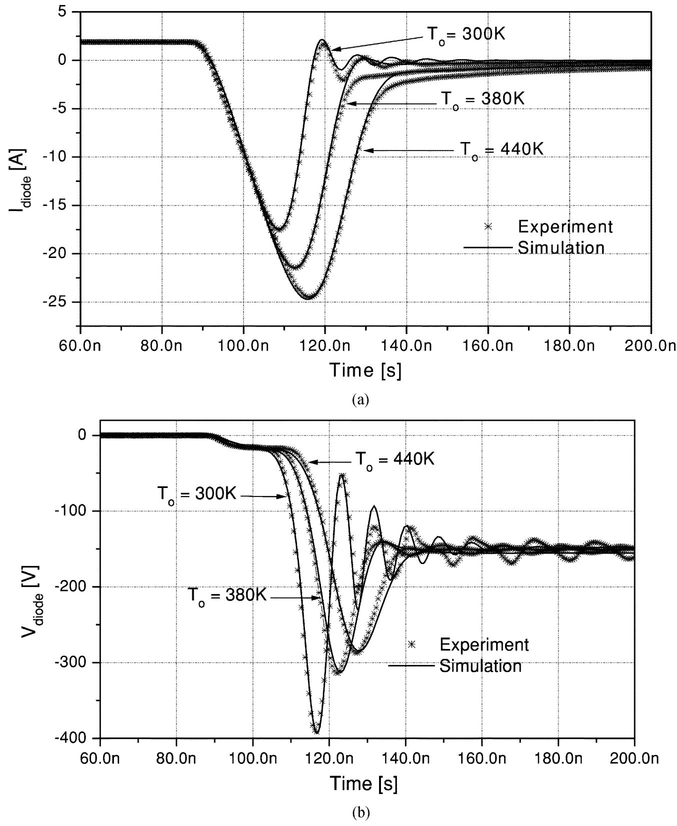

Fig. 11. Comparison of experimental and simulation results at various temperatures. (a) Current waveforms. (b) Voltage waveforms.

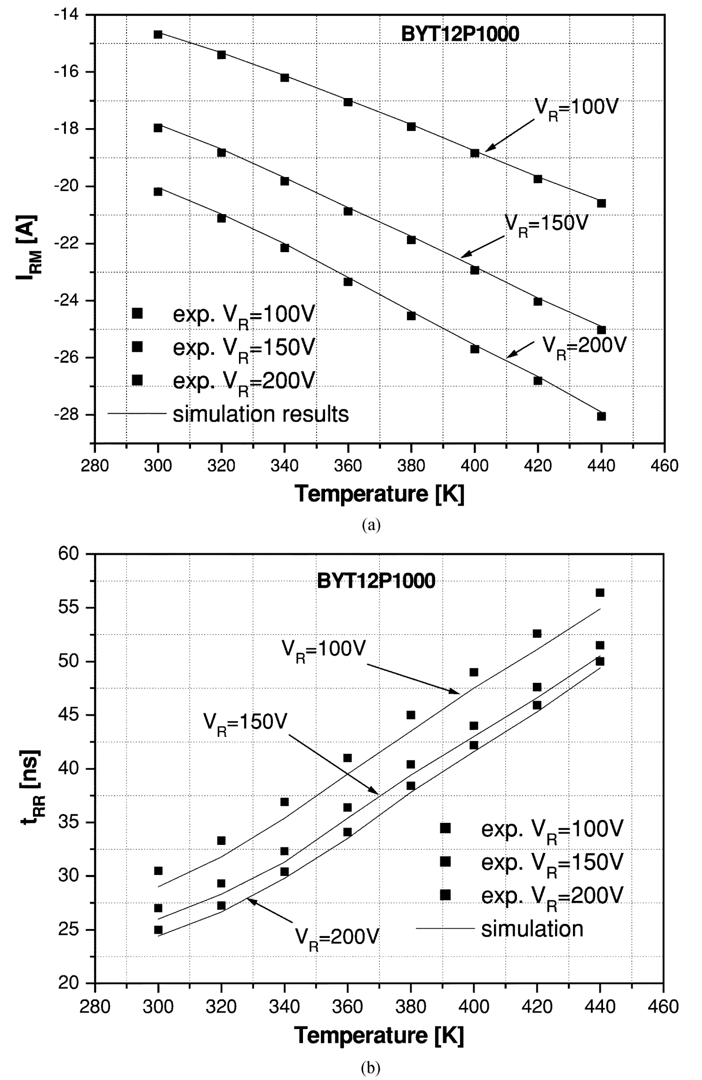

Fig. 12. Maps of switching parameters for the device BYT12P1000. (a) $I_{\rm RM}$. (b) $t_{\rm RR}$.

The ambipolar lifetime influences the recovery time, $t_{\rm RR}$ (Fig. 6) defined as $(t_1 + \mathrm{t}_2)$ where t_1 and t_2 characterize the time intervals of constant current slope, dI_F/dt and dI_R/dt, respectively. $I_{\rm RM}$ and $t_{\rm RR}$ define the recovery charge, $Q_{\rm RR}$. The recovery charge is then influenced by τ, A, W_D and N_D: i.e., the design parameters of the epitaxial layer. The value of τ is estimated by matching experimental and simulated values of t_1 and t_2. The effective area, A, is estimated in a subsequent step. So step #3 has to be repeated, and the values of W_D and N_D are also refined by the way. Step #1 is repeated for the sake of coherence in the latter parameter values.

The estimation of the ambipolar lifetime is not expensive from CPU-cost point-of-view as it only requires few loops. However the success of this step is related to the accuracy of estimation of t_1, t_2, and $I_{\rm RM}$. One cause of error is due to the current and voltage probe. As stated in introduction, probes interact with the device under test, create delays due to propagation in the cable, and worst of all, degrade the signal due to distortion in the probes and the cables. The overall accuracy of the extraction procedure requires the probe effects to be taken into account in simulation. The author experienced that probe models are easily introduced in simulation while it is more difficult to post-process experimental data [28].

Fig. 10 pictures a comparison of waveforms during the reverse recovery of the device STTA81200. The operating conditions are $I_F = 2$ A, $V_R = 150$ V, and $L_D \approx 77$ nH. An optimal design parameter set has been used in simulation. The simulation results give the estimation of current and voltage waveform at probe head (at device extremities) and at probe terminal (as displayed on the oscilloscope). It is obvious that the propagation delay is a cause of inaccuracy with regards to t_1 and t_2 for example. Fig. 10 shows a good agreement between simulation results including the probes and experimental results except at the end of turn-off (oscillations).

D. Step #4: Refinement of A

During an ultra-fast diode reverse recovery, when the maximal reverse voltage $V_{\rm RM}$ has been reached, the device behavior is determined by the interaction between its SCR and the external circuit. Indeed, at the end of the recovery process, the diode behaves as a nonlinear capacitance in series with circuit wiring parasitic components. This yields a damped oscillatory response of the voltage and current waveforms, with a fast decrease in the current [43]. Thus, the oscillation magnitude of the voltage waveform at the end of the recovery process depends on the effective value of the diode reverse-biased junction capacitance. Since this latter value is directly proportional to the PIN diode effective area [38], good agreement between experimental and simulated waveform oscillations at the end of the recovery process is obtained by tuning the device effective area, A. As indicated before, steps #3 and #1 have then to be repeated for the

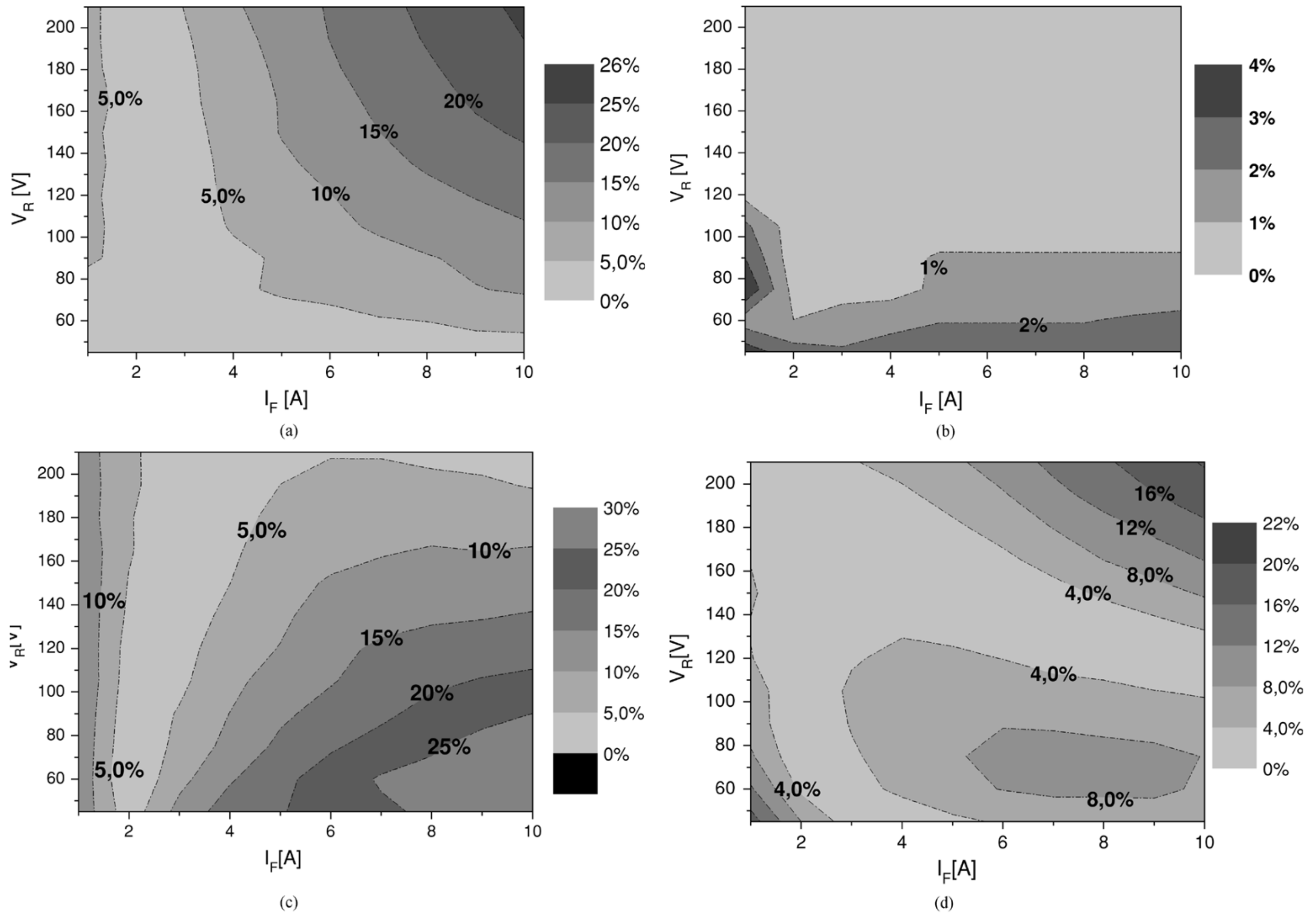

Fig. 13. Validity maps of switching parameters for the device BYT12P1000. (a) t_{RR}. (b) dI_F/dt. (c) I_{RM}. (d) V_{RM}.

sake of accuracy and consistency. It should be noted that the refinement of A is successful only if a correct model of the circuit wiring parasitics is available. Otherwise a part of discrepancies between simulation and experimental results are accounted for in the diode effective area and subsequently in the other design parameters.

The extraction procedure has been performed for numerous commercial diodes. Table I gives the extracted design parameter set for three devices. Around 20 simulations are required per device. Table II gives the experimental and simulated values of the switching parameters during a room temperature reverse recovery of a device STTB506D, with $I_F = 2$ A, $V_R = 200$ V, and $L_D \approx 35$ nH. Table II shows a good agreement between simulation and experiment. However the authors have the opinion that such results do not demonstrate the validity of the extracted design parameters.

A validity domain information should be preferred. Validity maps have been proposed in literature as comprehensive data about validity domain [44]. A validity map pictures the evolution of the error between experimental and simulated results about a switching parameter with respect to operating conditions. Validity maps are presented in next Section.

III. Validation

The extraction procedure for the device STTA81200 has been performed at room temperature (300 K). The experimental circuit in Fig. 2(b) is equipped with a thermal management unit TP041AH that controls the temperature of the diode under test. The diode reverse recovery is then operated at 380 K and 440 K, with $I_F = 2$ A, $V_R = 150$ V, and $L_D \approx 77$ nH. Experimental results are compared to simulation results. The 1-D model in Fig. 1 is used with the design parameters in Table I. From thermal simulation point-of-view, the diode is identified to a silicon die of negligible vertical thickness compared to other geometrical dimensions. Losses are assumed to be generated at the device top surface and to flow normally to the surface. A 1-D heat flow is considered. The die top surface ($x = 0$ in Fig. 1) is assumed to be thermally insulated. The bottom surface is a cooling boundary where temperature, T_0, is imposed by the hot air furnace. Convection and radiation are assumed negligible. The electro-thermal mode is selected in the FEM simulator Dessis. The Bennettwilson model [45] and the unified mobility model proposed by Klassen [46] are selected for the effective intrinsic density and the bulk mobility, respectively. Temperature dependence is considered for the Shockley–Read–Hall lifetimes [47]. The avalanche effects are also taken into account. The latter choices are adequate for the electro-thermal simulation of power devices. They are not discussed here as these issues are behind the scope of the paper. Fig. 11 pictures the comparison of results. An excellent agreement is found between experiment and simulation. A similar agreement has been noticed for many other commercial devices.

During the verification phase of a power system design, the engineer requires data to appreciate the simulation result accuracy. At device level, the engineer should appreciate the validity domain of a model including extracted parameters. Validity maps of switching parameters are good candidates to display validity domains. Reverse recovery of the device BYT12P1000 has been performed for various conditions of I_F, V_R and device temperature. Fig. 12(a) compares several simulation and experimental results about the switching parameter I_{RM}. There is a good agreement between experimental and simulation results. In Fig. 12(b), the agreement is not so good about the switching parameter t_{RR} for low reverse voltage, V_R. This moderate agreement is discussed here-after.

Fig. 13 pictures similar results but in terms of error between experiment and simulation results at room temperature. The dI_F/dt validity map indicates an error less than 4%. The validity map demonstrates the validity of the circuit wiring parasitic model (Fig. 5).

The t_{RR} map shows that the BYT12P1000 model offers a wide range of validity. The error exceeds 20% for I_F larger than 8 A and V_R larger than 160 V. This limitation is due mainly to the 1-D model in Fig. 1 since the circuit wiring model is satisfaying, and probe models have been taken into account. The V_{RM} and I_{RM} maps deserve the same comments.

The extraction procedure yields optimal design parameter values with regard to the experimental input data. Numerous results and diverse validity maps are satisfying so far. For a wide range of operating conditions, the 1-D model is then sufficient. As many physics-based analytical models of the PiN diode use the same parameter set, it is easy to extrapolate that these models will provide equivalent validity maps. The paper demonstrates that a generic 1-D diode model may be used for accurate electro-thermal simulation, providing an adequate design parameter extraction procedure. This generic model offers an efficient trade-off between accuracy, CPU-cost and ease of design parameter extraction.

However for large operating conditions, simulation results are affected by the model simplification. The P^+ and N^+ lateral regions are chosen arbitrarily in Fig. 1. At high current density, these regions may control the injection of carriers in the diode base region. The model may not estimate correctly the store charge in the diode. At circuit level, the values of I_{RM} and t_{RR} are not correct for example. One other major simplification is the diode epitaxial layer with constant doping level. In most devices, the drift region is made of one or more steps near the N^+ region [48]. This complex technology offers a better trade-off between switching speed, oscillatory reverse recovery, low forward voltage drop and breakdown voltage. Fig. 14(a) pictures an augmented doping profile model. One doping step is considered at the end of the epitaxial layer, and two additional design parameters have to be extracted at least. This doping profile is still generic as no manufacturing technology corresponds exactly to this model. Fig. 14(b) presents the optimal 1-D model for the device STTB506D. A local lifetime profile is associated to the doping profile. It is obvious that this doping profile is more complex than the generic model in Fig. 1, but it does not correspond either to the model in Fig. 14(b). This latter doping profile should enlarge the validity maps where the proposed generic doping profile suffers limitations. Particularly advanced doping profiles influence phenomena like Kirk effect or dynamic avalanche, occurring at both high voltage and high current. The authors have the opinion and the experience that a complex doping profile should be restricted to the cases when the diode technology is known. Otherwise the additional complexity in the parameter extraction method is not worth the small incremental accuracy.

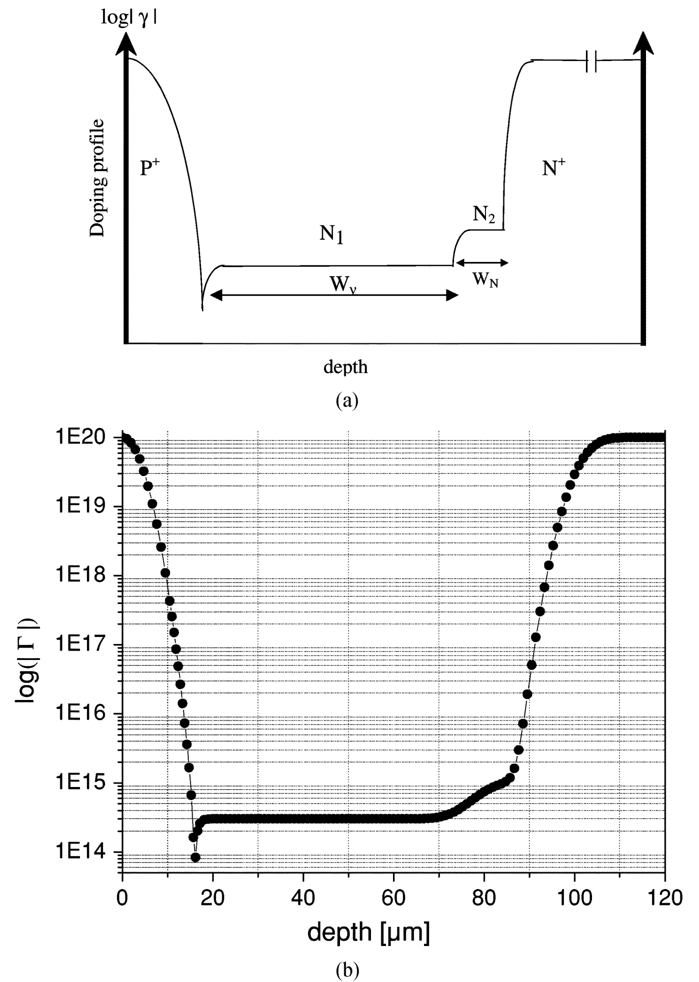

Fig. 14. Augmented doping profile model and optimal model for the device STTB506D. (a) "One-step" doping profile. (b) STTB506D.

Experiment concerns only few samples of a given commercial device. Extraction procedure may probably gives an other set of design parameters using other samples, i.e., not manufactured at the same time. The authors have not studied the statistical validity of estimated parameter sets.

IV. Conclusion

The paper details a novel method to more accurately assess diode design parameters. This job is necessary when a model must represent a specific device. Literature addresses largely model issues but scarcely parameter extraction issues. Optimal model parameters participates to simulation result accuracy. Accurate simulations are essential for prototype-less design of power integrated systems.

A simplified 1-D representation of the diode has been considered. The extraction procedure enables to obtain values for the major design parameters: W_D, N_D, τ, and A. The diode model associated to extracted parameters has been validated inside a switching cell circuit which corresponds to the classical operation of the diode.

Excellent simulation results with respect to experiment are obtained at moderate current level. The results demonstrate that a finite-element method approach is possible without the knowledge of the PiN diode technology. The paper illustrates also the advantage of heterogeneous simulation, including circuit and FEM device models.

An accurate model of the experimental circuit is considered including the wiring parasitic components and probe effects. Papers related to design parameter extraction do not pay sufficient attention to this issue. Then experimental results are compared to non pertinent simulation results. Errors due to negligence of mutual parasitic inductances and probes are translated to the device design parameters.

The extraction procedure leads to very accurate simulation. It paves the path to prototype-less design of power integrated systems. It enables the system analysis under extreme conditions like high temperature. It enables also to evaluate non available integrated systems like Silicon Carbide converters. Validity maps have been introduced to picture the validity domain of a model with associated design parameters.

Some improvements will be carried out with the automation of the design parameter extraction procedure. The procedure will also be improved taking into account secondary parameters like doping concentrations and widths of lateral regions.

REFERENCES

[1] F. Lee, J. V. Wyk, D. Boroyevitch, G. Lu, Z. Liang, and P. Barbosa, "Technology trends toward a system-in-a-module in power electronics," *IEEE CAS Mag.*, vol. 2, no. 4, pp. 4–22, 2002.
[2] J. Chen, Y. Wu, C. Gence, D. Boroyevitch, and J. Bohn, "Integrated electrical and thermal analysis of integrated power modules using iSIGHT," in *Proc. IEEE APES'01*, 2001, pp. 1002–1006.
[3] A. Bryant, P. Palmer, J. Hudgins, E. Santi, and X. Kang, "The use of a formal optimization procedure in automatic parameter extraction of power semiconductor devices," in *Proc. IEEE PESC'03*, vol. 2, 2003, pp. 822–827.
[4] R. Kraus and H. Mattausch, "Status and trends of power semiconductor device models for circuit simulation," *IEEE Trans. Power Electron.*, vol. 13, no. 3, pp. 452–466, May 1998.
[5] M. Cher and T. King-Jet, "Using power diode models for circuit simulations—A comprehensive review," *IEEE Trans. Ind. Electron.*, vol. 46, no. 3, pp. 637–645, Jun. 1999.
[6] P. Lauritzen, "Compact models for power semiconductor devices," Tech. Rep., Available: http://www.ee.washington.edu/research/pemodels/, 2000.
[7] P. Igic, P. Mawby, and M. Towers, "Physics-based dynamic electrothermal models of power bipolar devices (PiN diode and IGBT)," in *Proc. IEEE ISPSD'01*, 2001, pp. 381–384.
[8] N. Masmoudi, D. Mbairi, B. Allard, and H. Morel, "On the validity of the standard spice model of the diode for simulation in power electronics," *IEEE Trans. Ind. Electron.*, vol. 48, no. 4, pp. 864–867, Aug. 2001.
[9] C. Ma and P. Lauritzen, "A simple power diode model with forward and reverse recovery," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 342–346, Jul. 1993.
[10] C. Ma, P. Lauritzen, and J. Sigg, "Modeling of power diodes with the lumped-charge modeling technique," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 398–405, May 1997.
[11] H. Mantooth and J. Duliere, "A unified diode model for circuit simulation," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 342–346, Jul. 1993.
[12] A. Strollo, "A new SPICE model of power P-I-N diode based on asymptotic waveform evaluation," *IEEE Trans. Power Electron.*, vol. 9, no. 6, pp. 553–559, Nov. 1994.
[13] H. Morel, S. Gamal, and J. Chante, "A state-variable modeling of the power PiN diode using an explicit approximation of semiconductor device equations: A novel approach," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 112–120, Jan. 1994.
[14] P. Leturcq, M. Berraies, J. Laur, and P. Austin, "Full dynamic power bipolar device models for circuit simulation," in *Proc. IEEE PESC'98*, vol. 2, 1998, pp. 1695–1703.
[15] S. Bellone, G. Persiano, and A. Strollo, "A measurement method of the injection dependence of the conductivity mobility in silicon," *IEEE Electron Device Lett.*, vol. 16, no. 3, pp. 91–93, Mar. 1995.
[16] MDRAW-ISE Version 9: User's Guide Manual, ISE. (2003). [Online]. Available: http://www.ise.com
[17] Dessis-ISE Version 9: User's Guide Manual (2003). [Online]. Available: http://www.ise.com
[18] TMA, Inc., *Medici: User's Guide Manual*. Paolo Alto, CA: Technology Modeling Associates, 1999.
[19] Products Series SDN-414, T&M Research. (2001). [Online]. Available: http://www.tandmresearch.com
[20] F. Costa, E. Laboure, and C. Gautier, "Wide-bandwidth large ac current probe for power electronics and EMI measurements," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 502–511, Apr. 1997.
[21] P6139a Voltage Probe: Data Sheet, Tektronics. (2000). [Online]. Available: http://www.tek.com
[22] Application Note: The A-B-C's of Probes, Tektronics. (2003). [Online]. Available: http://www.tek.com
[23] N. Mohan, T. Undeland, and R. Robbins, *Power Electronics Converters, Applications and Design*, 2nd ed. New York: Wiley Interscience, 1995.
[24] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Berlin, Germany: Kluwer, 2001.
[25] *INCA: User's Guide Manual*, Cedrat, Grenoble, France, 1995.
[26] C. Hoer and C. Love, "Exact inductance equations for rectangular conductors with applications to more complicated geometries," *J. Res. Nat. Bureau Stand., Eng. Instrum.*, vol. 69C, no. 2, pp. 127–137, 1965.
[27] A. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Dev.*, vol. 16, pp. 470–481, 1972.
[28] K. Ammous, B. Allard, O. Brevet, H. El-Omari, D. Bergogne, D. Ligot, R. Ehlinger, and H. Morel, "Error estimation of power switching losses based on electrical measurement," in *Proc. IEEE PESC'00*, 2000, pp. 1549–1598.
[29] IC-CAP User's Manual, Hewlett-Packard. (2003). [Online]. Available: Available: http://www.hp.com
[30] M. Domeij, J. Lutz, and D. Silber, "On the destruction limit of Si power diodes during reverse recovery with dynamic avalanche," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 486–493, Feb. 2003.
[31] J. Lutz, "Fast recovery diodes—Reverse recovery behavior and dynamic avalanche," in *Proc. Int. Conf. Microelectron.*, vol. 1, 2004, pp. 11–16.
[32] J. Karamarkovic, T. Pesic, and N. Jankovic, "An analytical approach to kirk effect modeling," in *Proc. Int. Semiconductor Conf.*, vol. 1, 2000, pp. 311–314.
[33] K. Shenai, P. Singh, S. Rao, D. Sorenson, K. Chu, and G. Gaylon, "On the reliability of dc–dc power converters," in *Proc. Energy Conversion Engineering Conf. Exhibit*, vol. 2, 2000, pp. 1480–1490.
[34] C. Lin, B. Allard, H. Morel, and J. Chante, "Technological parameter identification of PiN diode using transient signal parameter fits," in *Proc. Eur. Power Electronics Conf.*, vol. 2, 1993, pp. 29–33.
[35] A. Strollo and E. Napoli, "Improved PiN diode circuit model with automatic parameter extraction technique," in *Proc. Inst. Elect. Eng.*, vol. 144, 1997, pp. 329–334.
[36] Y. Yuan and Z. Qian, "An improved lumped-charge model and parameter extraction approach of PiN diodes," in *Proc. IEEE PESC'02*, vol. 3, 2002, pp. 1301–1304.
[37] X. Kang, A. Caiafa, E. Santi, J. Hudgins, and P. Palmer, "Parameter extraction for a power diode circuit simulator model including temperature dependent effects," in *Proc. IEEE APEC'02*, vol. 1, 2002, pp. 452–458.
[38] S. Sze, *Physics of Semiconductor Devices*, 3rd ed. New York: Wiley, 2001.
[39] B. Baliga, *Modern Power Devices*, 2nd ed. Malabar, FL: Krieger, 1995.
[40] S. Sze and G. Gibbons, "Avalanche breakdown voltages of abrupt and linearly graded p-n junctions in ge, si, gaas, and gap," *Appl. Phys. Lett.*, vol. 8, pp. 111–121, 1966.
[41] V. 6.0.3: User's Guide, Phoenix Integration Model Center. (2004). [Online]. Available: http://www.phoenix-int.com/products

[42] V. 3: User's Guide, Mathworks Optimization Toolbox. (2004). [Online]. Available: http://www.mathworks.com/products/optimization
[43] S. Gamal, "Analysis and modeling of power PiN diode behavior at high temperature," Ph.D. dissertation, INSA de Lyon, France, 1992.
[44] B. Allard, H. Garrab, W. Mi, K. Ammous, and H. Morel, "Switching parameter maps—-A new approach to the validity domain of power device models," in *Proc. IEEE PESC'03*, vol. 3, 2003, pp. 1220–1225.
[45] M. A. Green, "Intrinsic concentration, effective densities of states, and effective mass in silicon," *J. Appl. Phys.*, vol. 67, no. 6, pp. 2944–2954, 1990.
[46] D. Klassen, I. Slotboom, and H. De-Graaff, "Unified apparent band gap narrowing in n and p type silicon," *Solid-State Electron.*, vol. 35, no. 2, pp. 125–129, 1992.
[47] M. S. Tyagi and R. Van-Overstraeten, "Minority carrier recombination in heavily-doped silicon," *Solid-State Electron.*, vol. 26, no. 6, pp. 577–597, 1983.
[48] R. Sunkavalli, A. Tamba, and B. Baliga, "Step drift doping profile for high voltage di lateral power devices," in *Proc. IEEE Int. SOI Conf.*, 1995, pp. 139–140.

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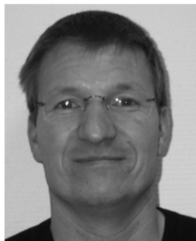

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