A 4H-SiC High-Power-Density VJFET as Controlled Current Limiter

Dominique Tournier, Philippe Godignon, Joseph Montserrat, Dominique Planson, Christophe Raynaud, Jean Pierre Chante, Jean-François de Palma, and Franck Sarrus

***Abstract*—Considering fault current limiters for serial protection, many structures exist, from regulation to other complex systems such as circuit breakers, mechanical switches, or more conventional fuses. Up to now, only a few semiconductor current limiter structures have been described in the literature. Although current-regulative diode components already exist, their voltage and current capabilities ($V_{BR} = 100$ V, $I_{\max} = 10$ mA), do not allow their use in power systems. This paper presents both simulation study and experimental results of a bidirectional current limiter structure based on a vertical SiC VJFET. The device was designed for serial protection in order to limit I^2t value. Finite-element simulations were performed with ISE-TCAD software to design the device and evaluate its static electrical characteristics. Then, dynamic simulations were performed to underline current reduction ability and power losses adjustment by gate resistance value optimization. Finally, electrical characterization for a unidirectional and a bidirectional device were done up to 400 V. The measured specific on resistance R_{ON} is in the range of 176 m$\Omega \cdot$ cm^2. Limiting capabilities have also been measured for a bidirectional device made of two unidirectional devices connected head to tail. The highest breakdown voltage value in "current limiting state" was measured to be ∼810 V, corresponding to a high power density of 140 kW/cm^2.**

***Index Terms*—Command integration, current limiter, high voltage, JFET, serial protection device.**

I. Introduction

The SiC-semiconductor-based devices are suitable for high-current and high-voltage applications [1], [2]. A promising application of SiC-based devices is current limitation for power system protection [3], [4], which benefits from its high thermal conductivity and wide bandgap. Most silicon components realized in SiCs, Schottky diodes, MOSFETs, and MESFETs, show good electrical and thermal characteristics [2]. A few SiC current limiters were presented in [5] and [6]. This paper targets the design, manufacture, and characterization of a new VJFET (Fig. 1), which implements both gate and source in buried layers. In the steady state, the voltage drop across the component must be as low as possible. In the active state (limiting phase), the current limiter must sustain a high current, under high-voltage bias. The resulting high power density must not cause the component failure. We describe the structure, the behavior of the component, and the adjustable parameters. Then, dynamic simulations are discussed. Finally, experimental electrical characteristics of both unidirectional and bidirectional current limiters are presented.

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D. Tournier, P. Godignon, and J. Montserrat are with the Centro Nacional de Microelectronica, 08193 Bellatera, Spain (e-mail: Dominique.Tournier@cnm.es; Philippe.Godignon@cnm.es; Josep.Montserrat@cnm.es).

D. Planson, C. Raynaud, and J. P. Chante are with the Centre de Génie Electrique de Lyon-INSA, 69621 Villeurbanne, France (e-mail: Planson@cegely.insa-lyon.fr; Raynaud@cegely.insa-lyon.fr; Chante@cegely.insa-lyon.fr).

J.-F. de Palma is with Ferraz Shawmut, Inc., Newburyport, MA 01950-1930 USA (e-mail: jeanfrancois.depalma@ferrazshawmut.com).

F. Sarrus is with Ferraz Shawmut, 69720 St Bonnet de Mure, France (e-mail: Franck.Sarrus@fr.ferrazshawmut.com).

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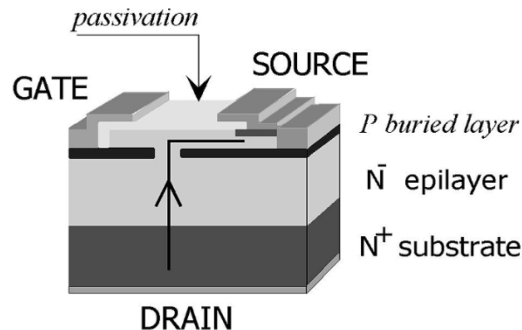

Fig. 1. Cross section of the VJFET.

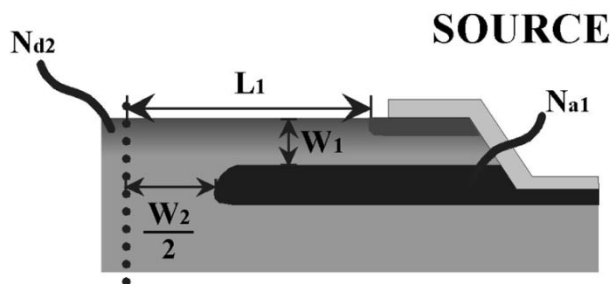

Fig. 2. VJFET parameters to be optimized.

II. SiC VJFET Controlled Current Limiter

A. Structure Description

The novelty of this device consists in the design of the gate, which is formed by a buried layer. Fig. 1 shows the cross section of the VJFET and Fig. 2 the main parameters to adjust. This device has a channel divided in two parts: a vertical one and a lateral one. The source is grounded and current flows from drain to source. P-buried layers are designed so that the

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TABLE I
MAIN PARAMATERS OF THE VJET

	Doping concentration (cm^{-3})	Thickness (μm)
Epitaxial layer	8×10^{15} cm^{-3}	18
P-buried layer	$N_{a1} = 2\times10^{18}$ cm^{-3}	2
Surface channel	$N_{d2} = 3\times10^{16}$ cm^{-3}	0.5

VJFET is normally on and presents a low specific resistance. When the drain voltage rises, the current saturates at a voltage corresponding to the pinch-off of both vertical and horizontal channels. In the saturation mode, the device presents an important on resistance (R_{ON}), resulting from the serial resistance of both parts of the channel and the drift resistance of the epitaxial layer. Due to self-heating, current decreases as the voltage increases (since electron mobility decreases and induces a current reduction). This effect is amplified while increasing the limiting current density. When a negative bias is applied between gate and source, the p-n junction formed by the p-well and the epitaxial layer is reverse biased leading to current modulation. A tradeoff between specific resistance and blocking capabilities was investigated by simulations. The main parameters are summarized in Table I.

B. Static Simulations

In order to optimize the structure layout, a global optimum parameter was defines. It derives from the classical equations of a VJFET [7], which define the relations between pinch-off voltage V_p (pinch-off current I_p, transconductance...) and both geometrical and doping parameters as summarized hereafter.

$$
\begin{aligned}
V_p &= \frac{q \cdot N_{d2} \cdot w_1^2}{2 \cdot \varepsilon} \\
I_p &= \frac{Z \cdot \mu \cdot q^2 \cdot N_{d2}^2 \cdot w_1^3}{6 \cdot \varepsilon \cdot L_1} \\
g_{ms} &= \frac{Z \cdot \mu}{L_1} \cdot (2 \cdot \varepsilon \cdot q \cdot N_{d2})^{1/2} \cdot \left[V_p^{1/2} - (V_{di} - V_g)^{1/2}\right] \\
g_o &= \frac{Z \cdot \mu \cdot q \cdot N_{d2} \cdot w_1}{L_1} \\
&\text{classical equations of a JFET.} \qquad (1)
\end{aligned}
$$

These equations were applied to the current-limiter structure with the geometrical parameters presented in Fig. 2. The global optimum parameter defined in (2) allows investigation of a tradeoff in terms of on resistance (g_0), current modulation (g_{ms}), and power losses in the limiting state $(V_P \times I_P)$

$$
\mathrm{Opt}(W, Nd, L) = \max \cdot \left(\frac{g_0 \cdot g_{ms}}{V_p \cdot I_p}\right)_{(W,Nd,L)}. \qquad (2)
$$

It allows us to get a range of parameters to be investigated by fine simulations.

As an example, considering a channel doping concentration of 3×10^{16} Atoms $\times$ cm^{-3}, the optimal channel thickness is assumed to be ~ 0.4 μm (Fig. 3). To estimate the peripheral effect on the electrical characteristics, finite-element simulations (using ISE-TCAD [8]) are useful. In that case, different models are used, taking into account physical properties of silicon carbide. As the dissipated power can reach high values, the mobility temperature dependence is taken into account [using the Caughey–Thomas model (see Table II)]. Most of parameters were given by Ruff [9] or are extracted from experimental results [10].

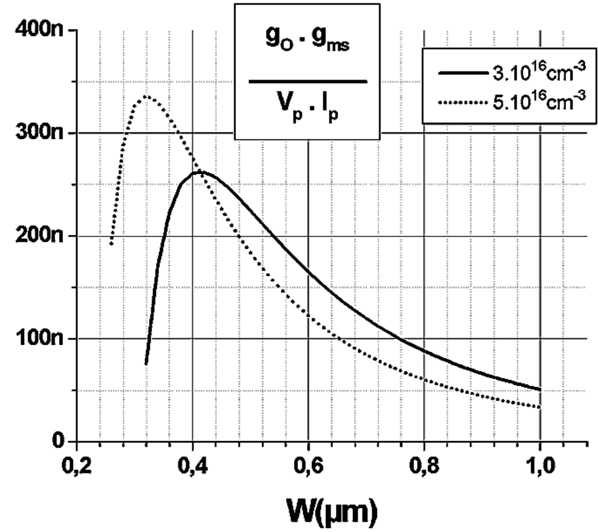


Fig. 3. Optimal channel thickness estimation.

TABLE II
MOBILITY MODEL AND PARAMETERS USED FOR SIMULATION (CAUGHEY–THOMAS MODEL)

$$
\mu_{n,p} = \mu_{\min 1} + \frac{\mu_{\max}\left(\frac{T}{300}\right)^{-\xi} - \mu_{\min 2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}}, \qquad N_i = N_A
$$

Paramètres	4H-SiC	
	µn	µp
μ_{max} ($cm^2.V^{-1}.cm^{-1}$)	870	120
μ_{min1} ($cm^2.V^{-1}.cm^{-1}$)	0	0
μ_{min2} ($cm^2.V^{-1}.cm^{-1}$)	0	0
Cr (cm^{-3})	2.10^{17}	5.10^{19}
α	0,55	0,3
ξ	2	2

The effect on electrical characteristics of each parameter presented in Fig. 2 was estimated by finite-elements simulation. As an example, channel doping level N_{d2} has been investigated. Current density dependence and self-heating effect are presented in Fig. 4 (both increasing while rising doping concentration). The simulated specific resistance R_d in the linear mode is in the range of 150 m$\Omega \cdot \mathrm{cm}^2$ at $V_{DS} = 1$ V.

The saturation current dependence on channel implanted dose D ($D = N_{d2} \times w_1$) was checked by means of finite-element simulations. This lets us choose a set of fabrication parameters considering, for example, the desired current saturation value (Fig. 5). Additional parameters such as the breakdown voltage have been taken into account for the design of the final demonstrator.

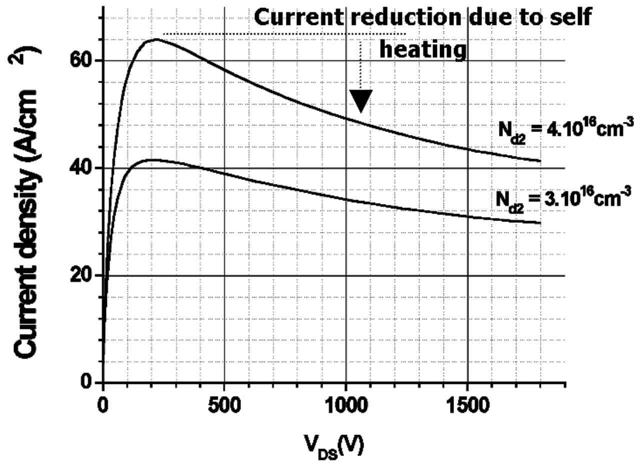


Fig. 4. Influence of the surface channel doping on the current density and self-heating effect.

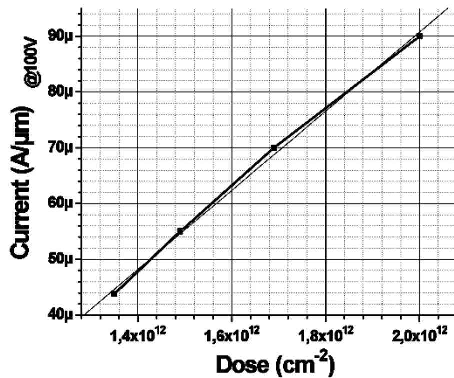


Fig. 5. Saturation current dependence versus channel dopant dose.

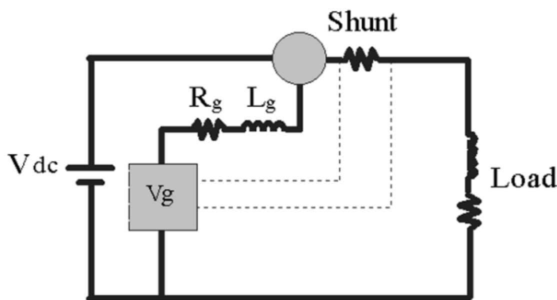


Fig. 6. Electrical circuit for switching.

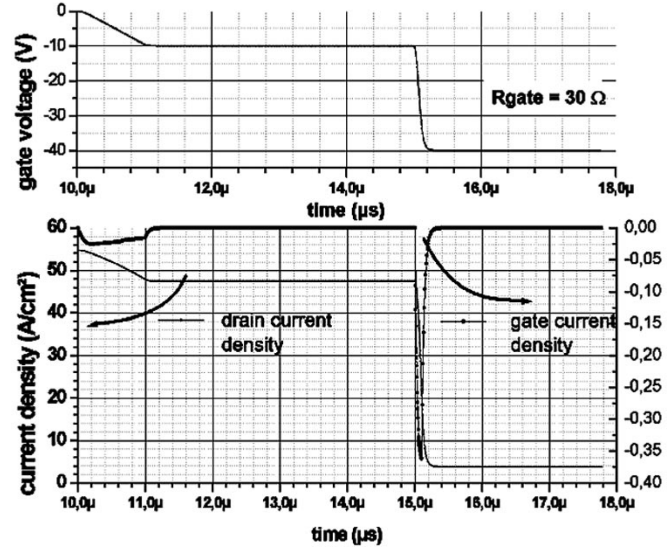


Fig. 7. Current reduction and switch-off waveform.

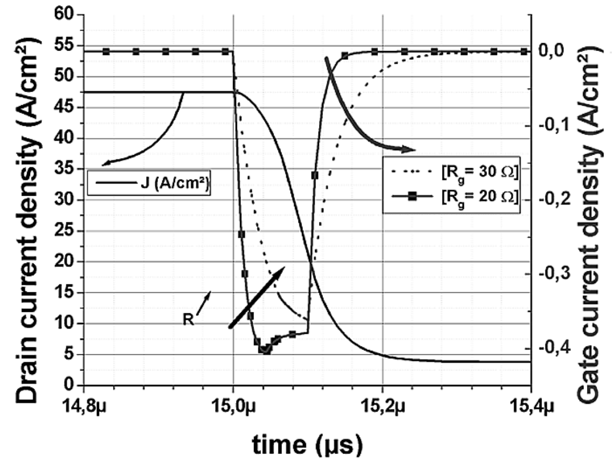


Fig. 8. Switch-off characteristics details for two $\mathrm{R_{gate}}$ values.

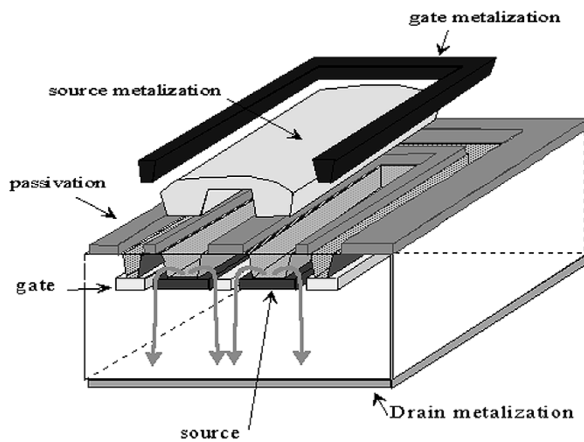
TABLE III
COMMUTATION LOSSES AS A FUNCTION OF R_G

R_G	$I_{Gmax\,(A/cm^2)}$	$P_{off\,(W/cm^2)}$
20	- 0.41	0.146
30	-0.36	0.133

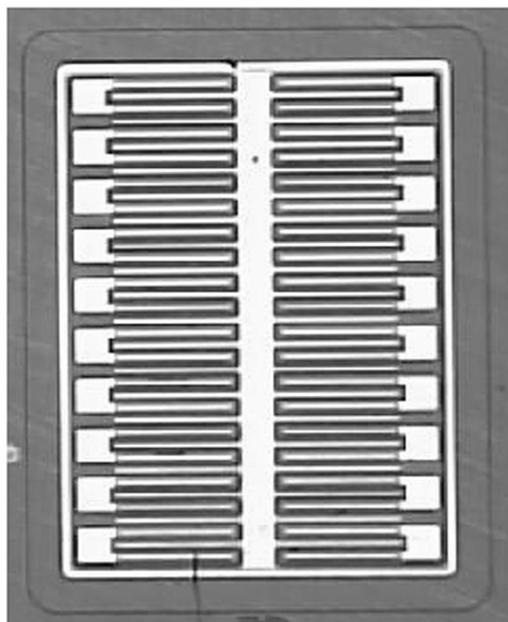
C. Dynamic Simulations

Mixed-mode simulations using a Spice circuit and finite elements for the VJFET were done to evaluate switching performance of the circuit described in Fig. 6. Parasitic wiring inductance has been taken into account. Using a shunt for current sensing and an appropriate electronic command block allows us to modulate the VJFET gate voltage in this way to reduce the current in the circuit. The simulated electrical circuit is presented in Fig. 7. Switching simulations were performed with a two-step gate bias.

The first gate bias step underlines the current reduction ability ($V_{GS} = -10$ V at $t = 10$ μs). Then, applying a gate bias $V_{GS} = -40$ V at $t = 15$ μs allows us to shut down the current in the circuit as presented in Fig. 7. The switch-off gate current is dependent on the gate resistance value and voltage rise time. Adjusting the resistance value allows us to control the gate switch-off power losses, without an effect on drain current value and switch-off time, as shown in Fig. 8. Consequently, gate power losses and peak current are reduced by around 10% as shown in Table III.



(a)



(b)

Fig. 9. (a) Interdigitated structure cross section. (b) Fabricated interdigitated VJFET (1.4 × 1.8 mm).

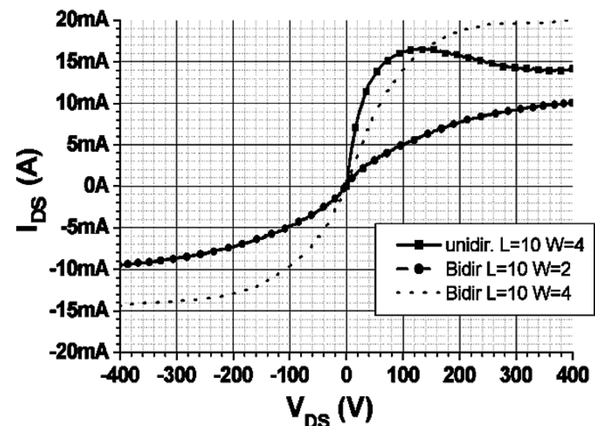


Fig. 10. Electrical measured characteristics for unidirectional and bidirectional limiters.

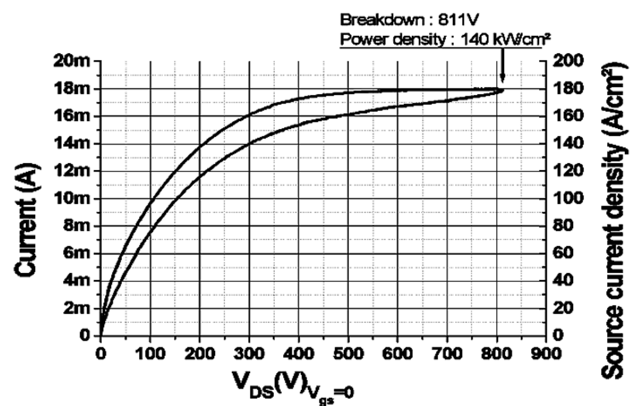


Fig. 11. High breakdown voltage measurement of a unidirectional current limiter (sinusoidal waveform, 50 Hz).

III. Device Fabrication and Characterization

A. Device Fabrication

Various device layouts have been implemented (such as an interdigitated device presented in Fig. 9), to validate the process technology, parameters adjustments, and the device performance. Key points of the device fabrication are high energy implantation, annealing activation, and ohmic contact formation. State-of-the-art values [2] of ohmic contact were measured on the first batch of VJFETs fabricated ($\approx 10\ \mu\Omega \cdot \mathrm{cm}^2$).

B. Static's Measurements

Fig. 10 presents the measured electrical characteristics for a unidirectional VJFET. Unidirectional measurements were done by applying 0.5-s pulse ($f = 2$ Hz), with drain biased up to 400 V. The specific on-resistance varies from 176 up to 237 $\mathrm{m}\Omega \cdot \mathrm{cm}^2$ for the matrix structures. The maximum pulsed power density dissipated in the limiting mode is 160 kW/cm^2. Limiting capabilities have also been measured for a bidirectional device made of two unidirectional devices connected head to tail (i.e., drain connected). This one exhibits a specific on-resistance of 700 $\mathrm{m}\Omega \cdot \mathrm{cm}^2$. The highest breakdown in the "current-limiting state" was measured to be ~810 V (Fig. 11), corresponding to a high pulsed power density of 140 kW/cm^2.

C. Dynamic's Measurements

The response time of the current limiter was checked by means of short-circuit measurements, using the following electrical circuit setup (Fig. 12). The power supply used was a 240-V 50-Hz sinusoidal source. Load was 5-W/240-V bulbs. Using the mechanical switch, a short circuit was performed on one of the lights serially plugged with a current limiter. Both VJFET current and voltage evolution were measured in the case of short circuit.

The gate of the VJFET was not connected in order to show the self-protection capability of the device. Without any external electronic system, the VJFET is able to protect against short circuit as shown in Fig. 13. A response time of $t_r = 0.7\ \mu$s was measured, with a limited current $I_{cc} = 270$ mA after stabilization.

Considering the impedance of the electrical circuit, without serial protection the fault current rise up would have been 43 A/μs. This measurement clearly demonstrates the efficiency

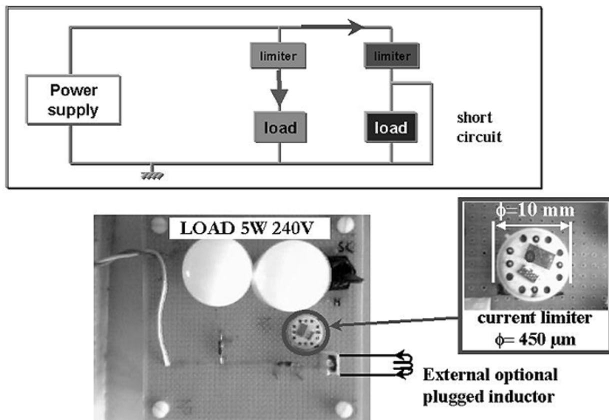


Fig. 12. Electrical circuit used to performed short-circuit measurements.

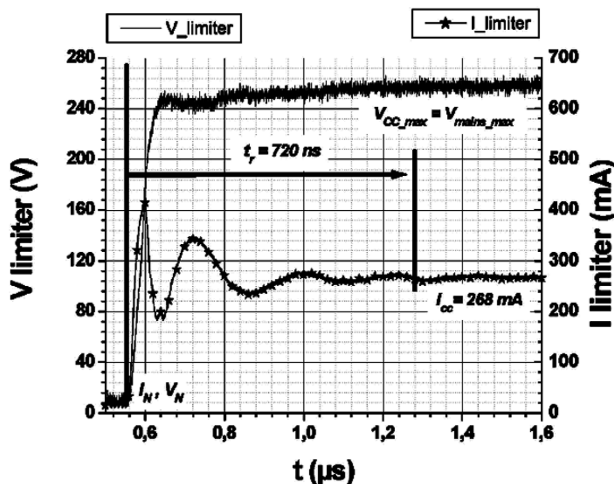


Fig. 13. VJFET response to a short circuit (measurements).

of serial protection using a VJFET as a current limiter. The short circuit was maintained during more that 5 min, without any failure of the device, which was able to sustain short-circuit power of 70 W (an equivalent power density of 75 kW/cm^2). Temperature increase in that case is lower than 70 °C.

IV. Conclusion

This paper has demonstrated the feasibility of an SiC current limiter with high power density. The design was made using the ISE software with respect to the technological limitations. The first demonstrator exhibits optimistic characteristics. Bidirectional components were measured by associating two devices head to tail. Moreover, the SiC VJFET manufacturing process is compatible with the SiC MESFET manufacturing process [11]. This allows us to foresee the integration of a self-controlled current limiter by an appropriate association of FET transistors.

A short-circuit demonstration was done using 5-W/240-V bulbs as a load. A very low response time to short circuit has been measured (as low as 1 μs). This device could be used in applications such as current limitation in the case of a short circuit of an electrical system. Using such a component could allow an increase of the current ratings of classical mechanical devices. The next challenge consists of both current sensing and current modulation in the limiting state using the gate electrode so as to reduce short-circuit power losses.

Acknowledgment

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Dominique Tournier (S'02) was born in Bourgoin-Jallieu, France, in 1973. He received the Ph.D. degree from the Institut National des Sciences Appliquées (INSA), Lyon, France, in 2003.

In 2003, he joined the Centro Nacional de Microelectronica, Bellaterra, Spain. His interests are silicon carbide device design and fabrication for high-power electronics applications.

Philippe Godigon received the Ph.D. degree in electrical engineering from the Institut National des Sciences Appliquées (INSA), Lyon, France, in 1993.

Since 1990, he has been with the Power Device and System Group, Centro Nacional de Microelectronica, Bellaterra, Spain, working on Si IGBT/VDMOS and SiC devices design and technologies. His expertise covers device technological process development and mask design as well as electrical characterization. He has authored more than 70 publications and conference papers on SiCs.

Joseph Montserrat received the B.S. and Ph.D. degrees in physics from the University of Barcelona, Barcelona, Spain, in 1985 and 1991, respectively.

In 1987, he joined the Centro Nacional de Microelectronica, Bellaterra, Spain, where he works as a Process Engineer in the Clean Room Group. He is responsible for the ion implantation and metallization areas. His main research interest is silicon technology for the manufacture of CMOS integrated circuits, power devices, and microelectronic sensors.

Dominique Planson was born in Paris, France, in 1965. He received the electrical engineering and Ph.D. degrees from the Institut National des Sciences Appliquées (INSA), Lyon, France, in 1991 and 1994, respectively.

In 1993, he joined INSA as an Associate Professor, where, since 1994, he has been an Assistant Professor. He is with the Centre de Génie Electrique de Lyon (CEGELY)-INSA, Villeurbanne, France, where his research is focused on silicon carbide power device design and applications of SiCs to power electronics.

Christophe Raynaud was born in Vienne, France, in 1969. He received the engineering and Ph.D. degrees from the Institut National des Sciences Appliquées (INSA), Lyon, France, in 1992 and 1995, respectively. His Ph.D. studies were devoted to characterizations of SiC bipolar and Schottky diodes and MOS devices in the Materials Physics Laboratory.

He also worked for three years on submicrometer silicon-based MOSFETs and EEPROMs, in particular, in charge pumping measurements, in modeling quantum effects in ultrathin oxide MOS, and studying EEPROM aging, in collaboration with ST Microelectronics. Since 1999, he has been Assistant Professor at INSA, where his research activities at the Centre de Génie Electrique de Lyon (CEGELY)-INSA, Villeurbanne, France, are focused on high-voltage silicon-carbide-based devices in the area of failure analysis.

Jean Pierre Chante was born in Lyon, France, in 1942. He received the "Doctorat d'Etat" degree from the University of Lyon, Lyon, France, in 1981.

From 1980 to 1986, he managed a research team in the field of power semiconductor devices at the Ecole Centrale de Lyon. Since 1986, he has been a Professor of Electronic Components and Applied Electronics at the Institut National des Sciences Appliquées (INSA), where he is the Head of the Power Devices and Applications Team which is part of the Centre de Génie Electrique de Lyon (CEGELY)-INSA, Villeurbanne, France. He is also in charge of the Centre Inter-Universitaire de Microélectronique de la Région de Lyon, which is a regional research center in the microelectronics field. His interests are in high-temperature electronics, SiC-based components, advanced power devices, and CAD tools for power electronics.

Jean-François de Palma was born in Torino, Italy, in 1963. He received the Ph.D. degree from the Institut National des Sciences Appliquées (INSA), Villeurbanne, France, in 1992.

In 1992, he joined Ferraz, St Bonnet de Mure, France, where, as a member of the R&D group, he worked on semiconductor market trend and performance analyses, TVSS components, pyrotechnic devices, and fuse development. In 1995, he moved to Ferraz Corporation, NJ, as Engineering Manager. From 1995 to 1998, he helped U.S. customers select fuses for their applications. In 1998, he returned to Ferraz as Manager of the Fuse Development Group, working mainly on fuses for IGBT case rupturing applications, high-voltage high-current fuses, and new technology for square-body fuses. In 1999 Ferraz, France, and Gould Shawmut merged, becoming Ferraz Shawmut. In 2000, he joined Ferraz Shawmut, Inc., Newburyport, MA, as the North American R&D Director.

Franck Sarrus was born in Guéret, France, in 1965. He received the Dipl.Eng. degree in electrical engineering from the University of Clermont Ferrand, Clermont Ferrand, France, in 1992, and the Ph.D. degree from the University of Lyon, Lyon, France, in 1995.

In 1995, he jointed Ferraz Shawmut, St Bonnet de Mure, France, as an Electrical Engineer on the research team. Since 2000, he has been an R&D Manager.