

Paralleling of Low-Voltage MOSFETs Operating in Avalanche Conditions

Cyril BUTTAY, Olivier BREVET, Bruno ALLARD, Dominique BERGOGNE, and Hervé MOREL
CEGELY,
INSA de Lyon
Bâtiment Léonard de Vinci,
Avenue Capelle,
69621, Villeurbanne, France
tel. 0033 (0)4 72 43 82 38
email: cyril.buttay@insa-lyon.fr
<http://cegely.cnrs.fr>

Keywords

Automotive component, automotive electronics, device modelling, MOSFET, thermal design.

Abstract

This paper addresses the behavior of low voltage MOSFETs under breakdown avalanche operation. The phenomena leading to avalanche operation of the MOSFET transistors in automotive applications are first presented. Then, after a brief description of the model and of the experimental identification of its parameters, electrothermal simulations are performed. A special focus is given to the current balance between paralleled MOSFETs, because in this case breakdown voltage mismatches are a well-known reliability issue. These simulations demonstrate the influence of the specific avalanche path resistance on current sharing. Calculations performed using the proposed model give results far less pessimistic (lower temperature rise on the most stressed transistor) than classical temperature-dependant-only avalanche models. This avoids expensive specifications narrowing when designing for mass-market applications (where wide manufacturing dispersions occur).

1 Introduction

1.1 MOSFET transistors parallel assembly under avalanche operation

Low voltage MOSFETs have become devices of choice in automotive applications. Their low ON-resistance ($R_{DS(on)}$) allows high current operation while keeping efficiency at high levels. Dramatic improvements of $R_{DS(on)}$ for low voltage transistors (< 50 V) have been permitted by increasing cell density up to several millions per square inch [1].

However, in some automotive applications, such as Integrated Starter Alternator (ISA), MOSFETs still have to be paralleled to supply a higher current (up to several hundreds of Amps). To keep $R_{DS(on)}$ low, transistors are selected with the lowest Breakdown Voltage (V_{BR}) rating available (typically 20 V devices for 14 V applications) [2]. With such a low voltage rating, the voltage spikes occurring during each commutation lead to avalanche of the transistors.

Unfortunately, manufacturers cannot ensure tight tolerances on breakdown voltages, due to process dispersions : two 20 V rated MOSFETs of the same reference can exhibit V_{BR} differences of several Volts. In a parallel assembly, this would result in having all the avalanche current flowing through only one transistor (the one with the lowest V_{BR}).

However, the Avalanche breakdown voltage is a well known temperature sensitive parameter that increases when the transistor heats. It is therefore usually considered that paralleled MOSFET will reach an equilibrium where the transistor having lowest breakdown voltage conducts first, goes hotter

making its V_{BR} to be equal to that of the remaining MOSFETs [3]. Therefore, current balance between paralleled MOSFET transistors is supposed to be accomplished by thermal effects.

However, as thermal transients are relatively slow (some tens to hundreds of microseconds to heat the active area of a transistor, depending on avalanche power level), one still could expect that only one single transistor will carry all the current during this period. In the case of short periods of avalanche operation, this transistor can face high thermal cycling, resulting in poor reliability.

1.2 Avalanche in automotive environment

It has been stated above that avalanche operation is caused by the small margin between automotive operating voltage (typically 14 V) and the breakdown voltage of the transistors (20 to 25 V). In order to keep converter costs low, filtering capacitors are reduced to the lowest value possible. Therefore, the inductive behavior of the wires connecting the converter to the vehicle battery is no longer masked by these capacitances. This results in a voltage spike across the transistors during turn-off.

Another cause of avalanche operation, more specific to the automotive environment, is the *load-dump* [4], [5], which is a spurious battery disconnection while it is being charged by the alternator. If this occurs, there is no more device to limit the vehicle network voltage and absorb the current generated by the alternator. Therefore, the alternator magnetic energy has to be dissipated by other means in order to avoid a voltage rise that could exceed 100 V.

That regulating role is fulfilled by the MOSFET inverter (or by the diode rectifier bridge in classical alternator applications). Due to instability of the low-voltage MOSFET transistors when in saturation mode [6], it is not possible to use them for linear regulation. Therefore, the only way to clamp the network voltage is to use the transistors in avalanche operation.

2 Low voltage MOSFET structures

Power MOSFET transistors are very well suited to low voltage applications as their low on-resistance creates lower voltage drop than with IGBTs.

$R_{DS_{on}}$ value is the key parameter of these high-current devices (current ratings over 100 A in a *D2PAK* package are not uncommon). Several parameters are responsible for the $R_{DS_{on}}$ value of a MOSFET (epitaxial layer resistance, JFET effect,... [2]), but for low-voltage devices, channel resistance and packaging (bond-wires and connections) are the most important.

Channel resistance is proportional to the MOSFET channel width. Several technologies are used to increase this width in a constant transistor area (i.e increase the channel density): strip layout, trench gate [2], [7]...

Measurements made in this paper have mainly been carried out on *STMicroelectronics STripFET STB210NF02* transistors. These MOSFETs have been described in literature [8]–[10]. They use planar channel technology (i.e non trench) with a strip layout that allows the increase of channel density by “simplifying the silicon fabrication steps” [9].

3 Measurement setup

The measurement setup that is used to identify the avalanche model parameters has been described in details in [11]. The principle is to measure the transistor temperature just after the avalanche pulse by the means of a thermal sensitive parameter : the body diode forward voltage drop. Successive measurements are performed with increasing avalanche pulse duration. It is then possible to build the temperature evolution by superposing all the measurements. The schematic of this system is given in figure 1(a).

3.1 Principle and schedule of a measurement iteration

Driving waveforms are pictured in figure 1(b). At the beginning of a measurement cycle (stage 1), the voltage across the capacitance is v_c , and current in the inductor is zero. During the second stage, inductor L is charged by closing switch ①, making v_c decrease down to zero. At this moment (stage 3), current in L is maximum and ① is opened (① and ② were closed before). Therefore current flows through ③, which is the Device Under Test. Some microseconds later (short enough for self-heating to be negligible) DUT is opened, triggering avalanche process. As ① has higher V_{BR} rating,

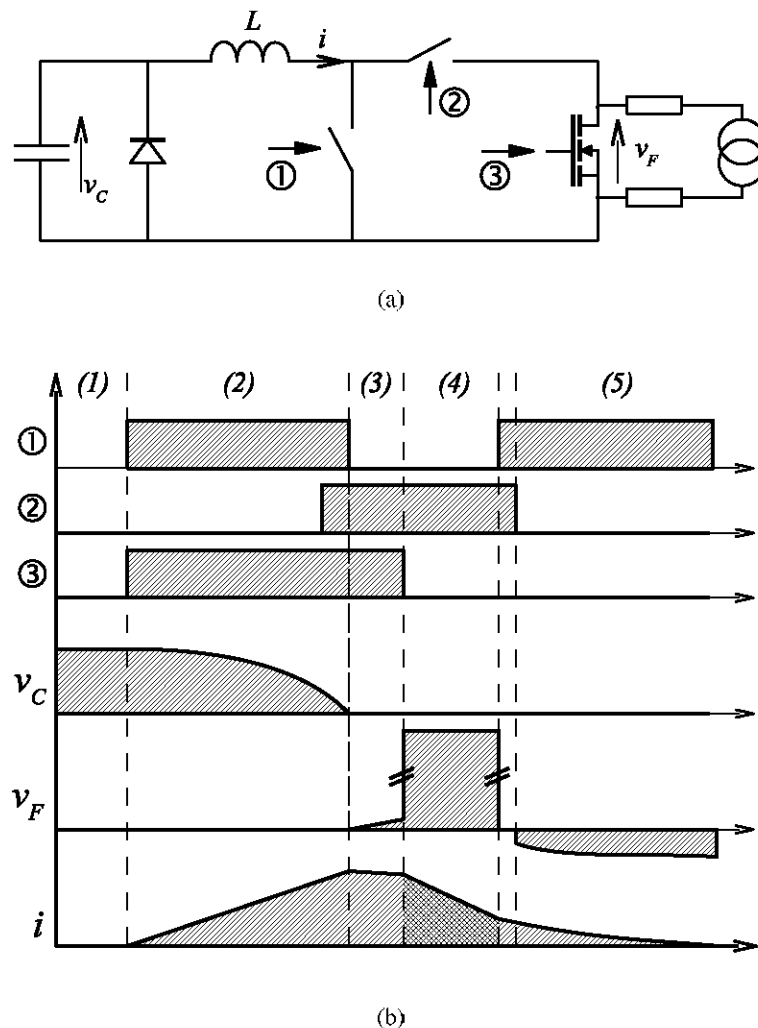


Fig. 1. (a) test setup allowing temperature profile measurement and (b) corresponding waveforms.

breakdown occurs in the DUT (phase 4). After an arbitrary delay, ① is closed once again to divert inductor current, then ② is opened to isolate the DUT (phase 5). Temperature is obtained by biasing the intrinsic body diode of the MOSFET by a low-value measuring current and acquiring the voltage drop V_F [12].

3.2 Measurements exploitation

This process is repeated several times, with increased avalanche pulse duration (this corresponds to an increase of stage 4 duration in figure 1(b)). Measurements acquired during each iteration are then superimposed (figure 2). Drain current and drain to source voltage during avalanche are plotted respectively in figures 2(a) and 2(b). Their "sliced look" is due to the superposition of successive acquisitions with increasing avalanche duration. At the end of each acquisition, body diode forward voltage is recorded, and plotted in figure 2(c). Using the linear relationship between forward-biased voltage drop of a diode and its temperature that was obtained through previous calibration (the $V_F = f(T)$ is shown in figure 3), it is then possible to plot temperature evolution of the MOSFET during and after avalanche (figure 2(d)).

4 A simple electrothermal model

An interesting fact is that peak temperature is reached at $t = 400 \mu s$ (see figure 2(d)), while peak drain to source voltage is around $t = 150 \mu s$ (figure 2(b)). This denotes that V_{DS} evolution is not

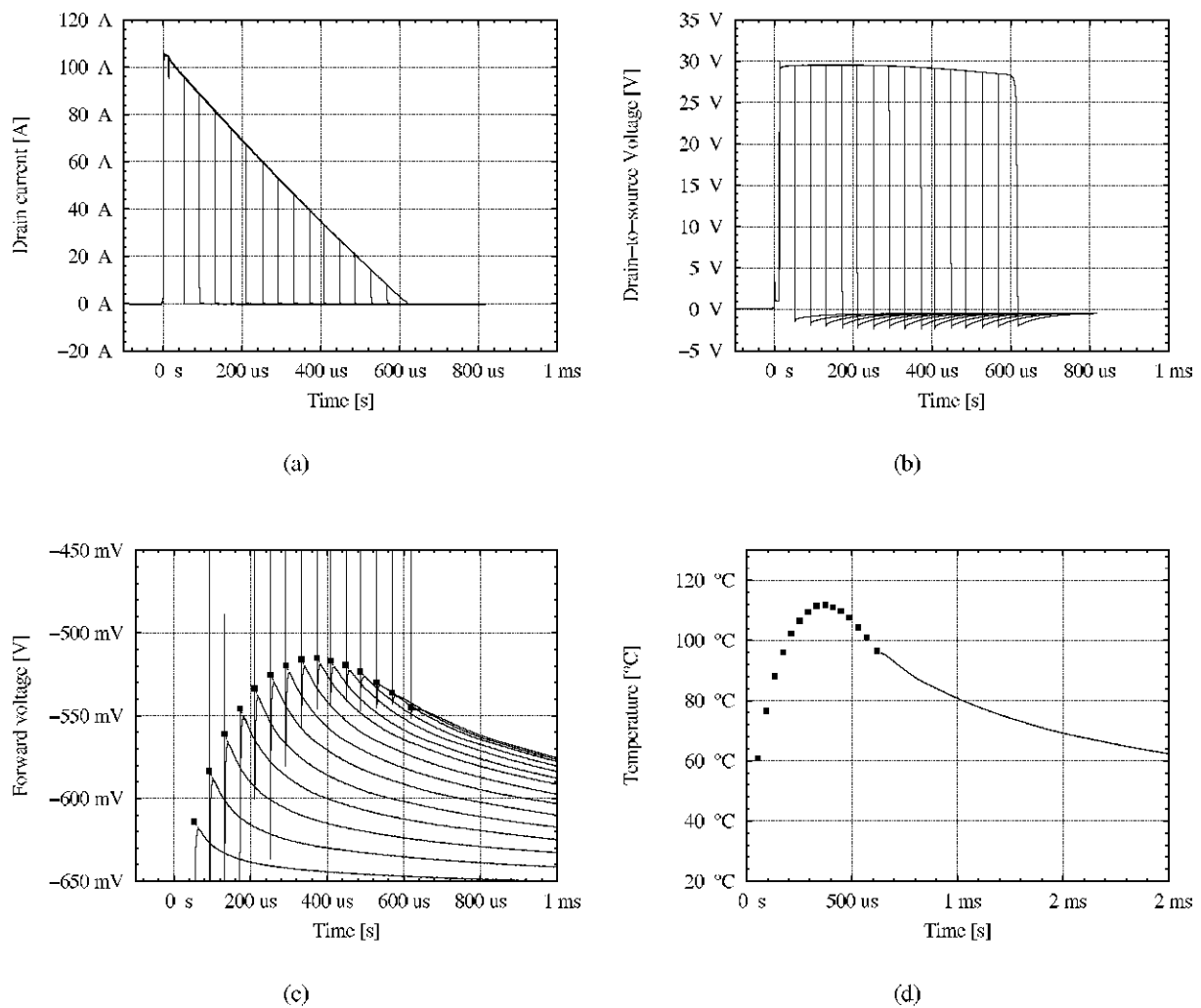


Fig. 2. Figures (a) to (c) are measurements performed using the proposed test setup: (a) and (b) are respectively the drain current and the drain-to-source voltage of the MOSFET under test during avalanche, (c) is the drain-to-source voltage of the MOSFET under test after avalanche with forward biasing of its body diode (this corresponds to a close-up view of (b)). As the forward voltage drop of a diode is linearly dependent on its temperature, it is possible to plot the temperature profile during avalanche (d) from (c).

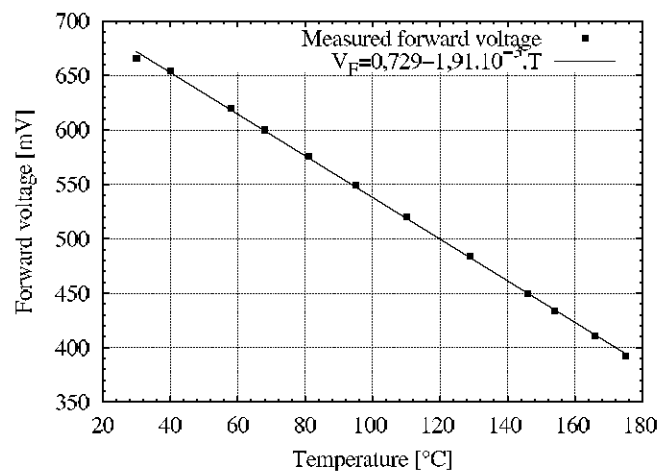


Fig. 3. Calibration curve of the temperature-sensitive parameter. The forward voltage drop of the MOSFET body diode, under a 0.6 A bias current, decreases linearly with increasing temperature.

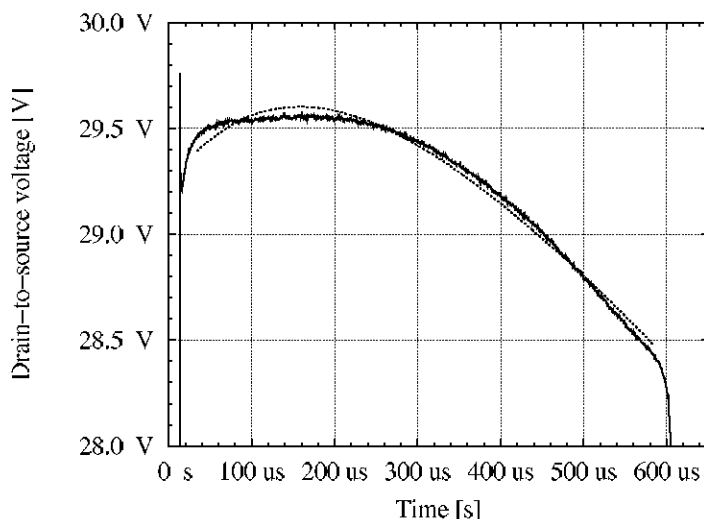


Fig. 4. Comparison between measured and calculated drain-to-source voltage during avalanche. Calculated waveform is obtained by feeding equation (1) with the measured avalanche current and transistor temperature data.

only related to the die temperature. Furthermore, V_{DS} is higher at the beginning of the current pulse (where chip temperature is as low as 30°C, and drain current is more than 100 A) than at the end (temperature is then almost 100°C, but current is near zero A). This demonstrates a resistive behavior during avalanche, as breakdown voltage is dependent on the avalanche current.

4.1 Breakdown voltage model

A very simple model describing drain to source voltage as a function of drain current and chip temperature is as follows:

$$V_{BR}(T) = V_{BR_0} + \beta T + R_{BR} I_D \quad (1)$$

This expresses the linear dependence of the breakdown voltage V_{BR} with temperature and with drain current. T is the transistor temperature (in Celsius degrees), V_{BR_0} is the 0°C breakdown voltage, and β reflects temperature dependence of V_{BR} ($V \cdot ^\circ C^{-1}$). R_{BR} is the avalanche path resistance (Ω).

The parameter set is chosen as to minimize (least square criterion):

$$\sum_{i=0}^N (V_{DSi} - V_{BR_0} - \beta T_i - R_{BR} I_{Di})^2 \quad (2)$$

Where V_{DSi} , T_i and I_{Di} are respectively the discretized i^{th} point of the drain-to-source, transistor temperature and drain current waveforms. An interpolation algorithm is used to compute the value of T_i between the points of figure 2(d).

The results of the identification process are as follow :

- $V_{BR_0} = 26.9 V$;
- $\beta = 14.8 mV \cdot ^\circ C^{-1}$;
- $R_{BR} = 12 m\Omega$, 4 times bigger than the $R_{DS_{on}}$ of the MOSFET (*STMicroelectronics STB210NF02*, 2.6 m Ω).

A comparison between the measured drain-to-source voltage and the corresponding waveform computed using equation (1) fed with measured drain current and transistor temperature shows a good agreement (see figure 4).

4.2 Thermal model

In order to perform electrothermal avalanche simulations, it is necessary to add a thermal model to the electrical model proposed above. This thermal model allows for transistor temperature calculation from the dissipated power waveform.

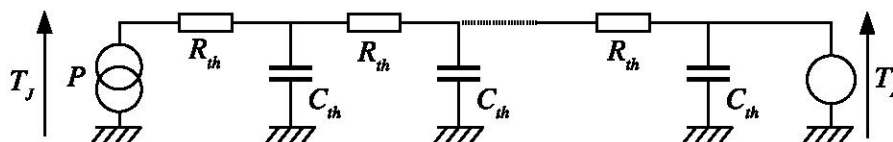


Fig. 5. Thermal model based on an electrical-equivalent network. The simulations presented in this paper were performed using 100 R_{TH} - C_{TH} -cells as a thermal model for the silicon die.

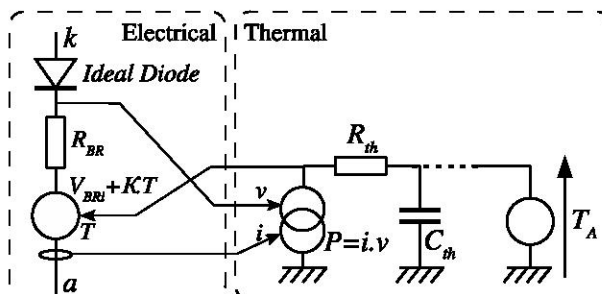


Fig. 6. Electrothermal model of avalanche

A classical thermal R_{TH} , C_{TH} network (see figure 5), based on unidimensional finite differences discretization is calculated [13] using the following relationship:

$$\begin{cases} R_{TH} = \frac{h}{KA} \\ C_{TH} = hA\rho c \end{cases} \quad (3)$$

Where A is the transistor die area (m^2), h the discretization width (m) and K , ρ and c are respectively the silicon thermal conductivity ($W.m^{-1}.K^{-1}$), density ($g.m^{-3}$) and specific heat ($J.g^{-1}.K^{-1}$). To achieve better accuracy over several hundreds of microseconds, the copper heat spreader (located under the silicon die) must also be taken into account, also using equation set (3). Finite-differences-based thermal modeling is not the most efficient [14], but providing enough subdivisions are considered, it is accurate for short power pulses (some microseconds).

Finally, some empirical modifications are mandatory to take into account the source metalization and bond-wires: at the beginning of heating, the heat flux is not unidirectional, as surface metallization (several microns thick) and bond-wires (up to $500 \mu m$ in diameter) represent an extra thermal capacitance, equivalent to about $40 \mu m$ of silicon above the active area. It has been experimentally verified both on encapsulated and bare-die transistor that epoxy encapsulation has negligible influence on thermal transients during avalanche.

The whole electrothermal model is therefore obtained by adding the electrical model of eq. (1) and the thermal network (figure 5), as depicted in figure 6. As this model is implemented into *Pspice*, which does only allow for electrical modeling, the thermal model is represented using electrical components such as resistance, capacitances, and current (representing power) and voltage (equivalent to temperature) sources.

Figure 7 shows a comparison between chip temperature and drain to source voltage obtained by the previous measurements and by simulation using the electrothermal model depicted in figure 5. 100 subdivisions have been considered in the silicon die thickness, and 30 for the copper heat spreader. It can be seen that the thermal model is valid up to $300 \mu s$ after the beginning of the avalanche pulse, but over that time, it is no longer accurate, as heat flow in the copper heat spreader is no more unidimensional.

5 Application to simulation of MOSFET paralleling

No previous work addressing MOSFET paralleling during avalanche taking into both account temperature *and* drain current influence was found in literature. In [15], authors only take R_{BR}

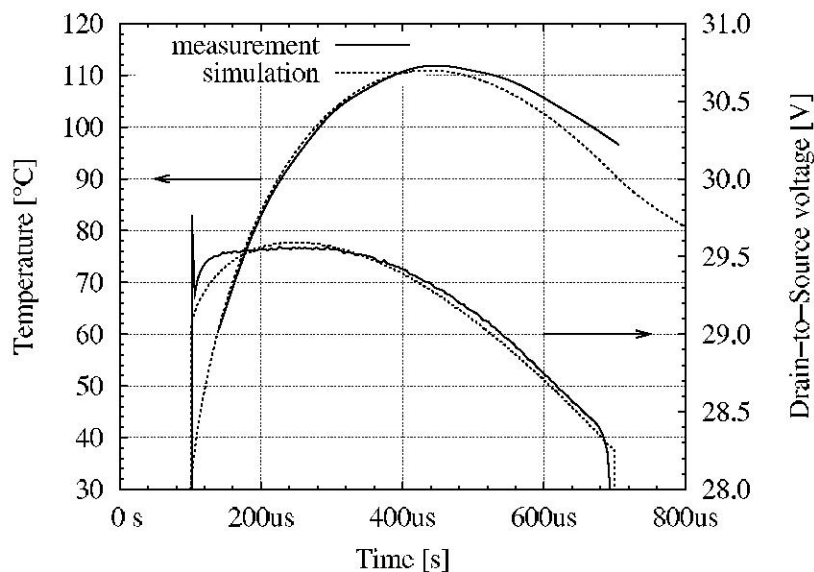


Fig. 7. Comparison between simulated and experimental drain-to-source voltage and transistor temperature.

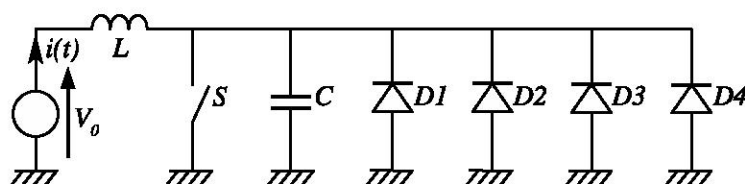


Fig. 8. Electrical schematic used for simulation. Switch S is turned-on to charge the inductor L , and then turned-off. This results in avalanche operation of the body diodes ($D1$ to $D4$) of the four parallel MOSFET transistors. The electrothermal avalanche model of the diodes is depicted in figure 6.

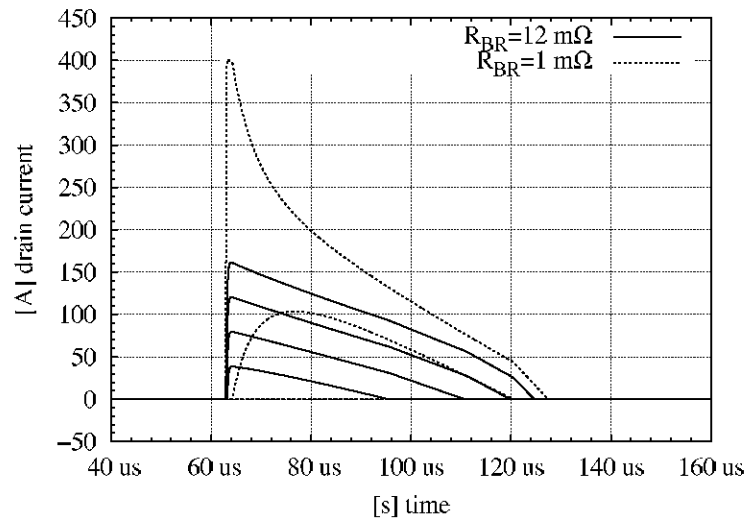
into account, while authors of [3] only consider thermal effects. In this section, simulation will be performed to estimate the influence of V_{BR_0} dispersions on current sharing during avalanche.

As explained in section 1.1, breakdown voltage mismatches between paralleled transistors can have a strong effect on reliability, as they can result in a high thermal cycling of one of the transistors. As experiments are difficult to carry out when addressing transistors manufacturing dispersions (this would require to have a transistor set that is representative of these dispersions), simulation is well suited to analyze the influence of V_{BR} mismatches.

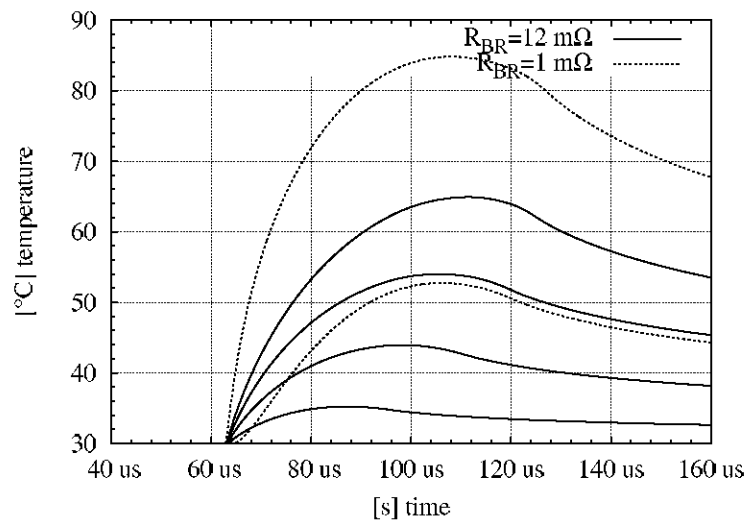
The schematic of figure 8 has been used to simulate the behavior of unmatched transistor paralleling. An inductor is charged by turning switch S on. When S is turned-off, voltage rises across the diodes $D1$ to $D4$ until it reaches the breakdown voltage of one of the diodes. Then avalanche phenomenon begins, and lasts until the inductor is totally discharged.

Using the four-paralleled devices system of figure 8, with V_{BR_0} values ranging from 25.5 V to 27 V (evenly spaced), two simulation runs have been carried out with varying R_{BR} value. In the first case, only the wiring resistances are taken into account for R_{BR} (bond-wires, transistor connections...) and are estimated to 1 m Ω . In the second case, the value of R_{BR} obtained through the identification process described in section 4.1 (12 m Ω) is considered. Results are plotted in figure 9. Figure 9(a) shows the drain currents in both cases and figure 9(b) the corresponding temperature waveforms.

In the first case, R_{BR} is low, so it has almost negligible influence on current sharing. At the beginning of the avalanche pulse, the transistor with the lowest V_{BR} (25.5 V) has to sustain all the current flowing through L . Its temperature rises quickly, making its breakdown voltage increase up to the second lowest V_{BR_0} value (26 V). Then avalanche current flows through two transistors, but further increase in the breakdown voltage will not be large enough to reach V_{BR_0} of the third transistor. This results in large self-heating of the first transistor (55°C above ambient).



(a)



(b)

Fig. 9. simulated drain current (a) and temperature (b) in a four-transistor-parallel assembly with breakdown voltage mismatches.

In the second case, R_{BR} is much higher (12 m Ω). As V_{BR_0} mismatches are set to 0.5 V between two transistors, the maximum resulting current unbalance is $I = \frac{0.5}{12 \cdot 10^{-3}} = 41$ A. It can be seen on figure 9(a) that this results in better current sharing between all transistors, as they all conduct as soon as the switch S is turned-off. Maximum temperature rise is then 35°C above ambient (figure 9(b)).

The positive influence of the avalanche path resistance on current sharing is demonstrated. Because of its high value (in the order of four times the $R_{DS_{on}}$), it is responsible for voltage drop comparable to the V_{BR} mismatches between transistors, and therefore acts as a feedback to minimize current unbalance. The influence of temperature is also non negligible, as 55 °C increase in temperature involves a 0.8 V increase of the breakdown voltage of transistors.

Simulations performed with the classical avalanche model (only temperature dependent) yield to a 55 °C temperature rise, far more than the results obtained using the proposed model (35 °C). As this latter model has proven to be accurate (see the experimental validation of figure 7), one can expect

a real temperature increase lower than that estimated using the classical model. In the design stage, this translates into wider acceptable limits on V_{BR} dispersions, and maybe no necessary screening on this parameter. This in turn reduces costs.

6 Conclusion

The interest of electrothermal avalanche simulation when transistors operate in parallel has been demonstrated. Breakdown voltage mismatches between transistors can result in stressing one of the transistors of the assembly.

The proposed electrical model has a very simple expression. Its parameters are experimentally obtained using a dedicated test setup. The thermal model is obtained through calculation. The combination of these two models shows good accuracy.

Using this electrothermal model, simulations are performed to estimate the influence of breakdown voltage mismatches on transistors temperature. It is shown that temperature increase is over-estimated using classical models in comparison to the experimentally verified proposed model. This is due to the balancing effect of a specific avalanche path resistance. Failure to consider this resistance in the avalanche simulations yields to about 40 % error in the computed temperature rise.

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