Model Requirements for Simulation of Low-Voltage MOSFET in Automotive Applications

Cyril Buttay, *Member, IEEE*, Hervé Morel, *Member, IEEE*, Bruno Allard, *Senior Member, IEEE*, Pierre Lefranc, and Olivier Brevet

***Abstract*—This paper focuses on the modeling of low-voltage automotive power electronic circuits to obtain accurate system simulation, including estimation of losses. The aim is to compare several metal-oxide semiconductor field-effect transistor (MOSFET) models to find out which can be used for low-voltage, high-current automotive converter simulations. As these models are intended for system simulation, only analytical models are addressed as they may be implemented into any circuit simulator. The different modes of operation of the switches are described (commutation, synchronous rectification, avalanche...), and several models of the power MOSFET transistor, allowing for simulation in these modes, are presented. Special care is given to the parameter extraction methods and to the interconnection model of the commutation cell. The four test circuits used to identify the low-voltage power MOSFET model parameters are presented. Comparison between simulations and measurements obtained with a calorimeter are then detailed. This measurement method is accurate and offers a simple way to prove the quality of simulation results. It is shown that the parameter identification is of major concern to achieve high accuracy, as classical Spice models can give good results, providing the model parameters are correctly set.**

***Index Terms*—Characterization, circuit parasitics, electrothermal, model, power metal-oxide semiconductor field-effect transistor (MOSFET), validation.**

NOMENCLATURE

α	Power diode model empirical parameter.
ϵ_{Si}	Silicon permittivity ($1.04.10^{-8}$ F.m^{-1}).
η	Static feedback factor for threshold.
γ	Dependence of V_{BR} with temperature (V.K^{-1}).
ρ	Density (g.m^{-3}).
τ_A	Minority carriers lifetime (s).
τ_D	Ratio coefficient between hole current and stored charge in PiN diode model.
θ	Mobility degradation factor (V^{-1}).
A	Junction area (m^2).
A_{GD}	Gate-drain facing area (m^2).
A_{MOS}	Transistor die area (m^2).
c	Specific heat ($\text{J.g}^{-1}.\text{K}^{-1}$).
C_{GD}	Gate-to-drain MOSFET capacitance.
C_{GS}	Gate-to-source MOSFET capacitance.
C_{JO}	Zero-bias junction capacitance (F).
C_{oxd}	Oxide capacitance (F).
C_{TH}	Thermal capacitance (J.K^{-1}).
$E_{\text{commut.}}$	Commutation energy losses (J).
E_{off}	Switching to off-state energy losses (J).
E_{on}	Switching to on-state energy losses (J).
E_{total}	Converter energy losses (J).
F	Switching frequency (Hz).
h	Discretization step for thermal modeling (m).
I_D	Drain current (A).
I_S	Saturation current (A).
K	Thermal conductivity ($\text{W.m}^{-1}.\text{K}^{-1}$).
K_P	Transconductance parameter (A.V^{-2}).
K_{Plin}	Transconductance parameter in linear region (A.V^{-2}).
K_{Psat}	Transconductance parameter in saturation region (A.V^{-2}).
L	Channel length (μm).
L_D	Drain inductance (H).
L_G	Gate inductance (H).
L_S	Source inductance (H).
M	Junction grading coefficient.
N	Doping (m^{-3}).
$P_{\text{cond.}}$	Conduction power losses (W).
P_{off}	Losses in off-state (W).
P_{on}	Losses in on-state (W).
P_{total}	Total power losses (W).
q	Electron charge (C).
R_S	Ohmic resistance (Ω).
R_{DSon}	On-state resistance (Ω).
R_D	Drain resistance (Ω).
R_G	Gate resistance (Ω).
R_S	Source resistance (Ω).
R_{TH}	Thermal resistance (K.W^{-1}).
t_{off}	Duration of the off-state (s).
t_{on}	Duration of the on-state (s).

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TT Transit time (s).
V_J Junction potential (V).
V_{bi} Junction building potential (V).
V_{BR} Avalanche path resistance (Ω).
V_{BR} Breakdown voltage (V).
V_{DS} Drain-to-source voltage (V).
V_{GS} Gate-to-source voltage (V).
V_{n0} Fitting parameter for diode static characteristic.
W Channel width (μm).
W Junction width (μm).

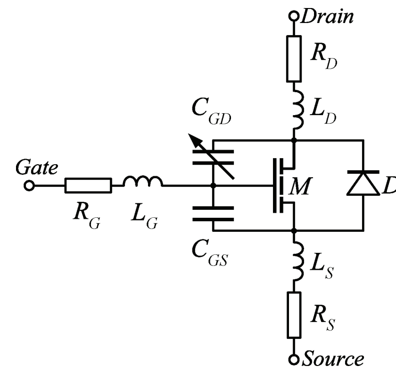

Fig. 1. Generic circuit model of the MOSFET transistor.

I. Introduction

In LOW voltage applications, as most automotive applications are, metal-oxide semiconductor field-effect transistors (MOSFETs) have become the most widely used power switch. Low on-resistance (R_{DSon}) combined with simplicity of drive are its key advantages.

The automotive industry now relies on power electronics for numerous features, and much more are to come [1]. In such a mass-market, optimization is mandatory to reduce converters costs. This, in turn, requires reliable design tools based upon simulation.

Classical design methods, which use breadboarding intensively, are not sufficient to analyze the behavior of a system in detail. Simulation allows for a deeper analysis of a system, including, for example, parameter mismatches due to manufacturing tolerances.

Automotive power converters are constructed using specific technologies (thermal enhanced substrates such as direct-bonded copper (DBC) or insulated metal substrate (IMS), and direct chip bonding to reduce manufacturing costs…) specifically adapted to mass production, but very expensive for prototyping. Computer simulation enables one to reduce experimental steps, resulting in faster and cheaper design processes.

MOSFET paralleling gives an example of the key advantages: it is possible to obtain the drain current in each transistor by simulation (while experiments would require intricate modification of the circuit to insert current probes), but it is also possible to determine the influence of parameter mismatches between transistors (what does occur if one of the MOSFETs has a threshold voltage lower than the others?), or the influence of the circuit layout (when modeling the interconnections). Using simulation, one can ensure that a particular design is suitable for mass production.

This paper focuses on the modeling of low-voltage, high-current automotive power electronic circuits using power MOSFETs. This modeling is intended to be used in classical circuit simulators, so only analytical models based on an equivalent-circuit representation are addressed (see Fig. 1). Accurate models, using for example finite element modeling (FEM), are far too CPU-intensive for the usual system simulations. Furthermore, these later models require technological knowledge of the transistor manufacturing process that is not available. However, despite the use of analytical models, the aim of this paper is to study the possibility of performing accurate simulation of systems, including losses and waveform estimation.

In the following section, the low-voltage commutation cell is presented, including its modes of operation. From this, it is possible to determine the specifications of the transistor model. Then, in Section III, two transistor models are presented, the first using the classical Spice models (for the static characteristic and the body diode), and a second using power-electronics specific models. Special attention is paid to interconnection modeling. Parameter extraction is presented in Section IV, as it is a very important stage to ensure accurate simulation. Validation of the modeling process is presented in Section V, where comparisons of experimental and simulation results are detailed. Finally, the key points of low-voltage power electronics modeling are discussed in Section VI.

II. Applications and Performance Requirements

Some authors in [2] have listed the performances a MOSFET model has to achieve depending on the converter architecture (buck, boost, flyback…). This is mainly based on a classical commutation cell (MOSFET + external diode) representation. Therefore, except for the inverter (the only studied converter with bidirectional current capability), body diode reverse recovery modeling is not required in a MOSFET model.

This is no longer true in low-voltage applications, as synchronous rectification is widely used to increase the converter efficiency. The commutation cell becomes an inverter leg, i.e., it is constituted of two MOSFET transistors. Commutation occurs between one transistor and its body diode (synchronous rectification) or the body diode of the other transistor (as in a classical MOSFET-diode commutation cell). A dead-time is necessary between the transistor commutations to avoid power supply short-circuits. In case of inductive load, the current path suffers no interruption and the MOSFET transistor body diodes are solicited. Therefore, a complete diode representation must be implemented into the transistor model to achieve accurate waveform simulation.

Possible mode of operation of a MOSFET transistor in an inverter or a reversible dc/dc converter are as follows:

- bidirectional current flow through the channel of the transistor;
- current flow through the body diode;
- synchronous rectification, i.e., short-circuit of the body diode by the transistor channel itself;

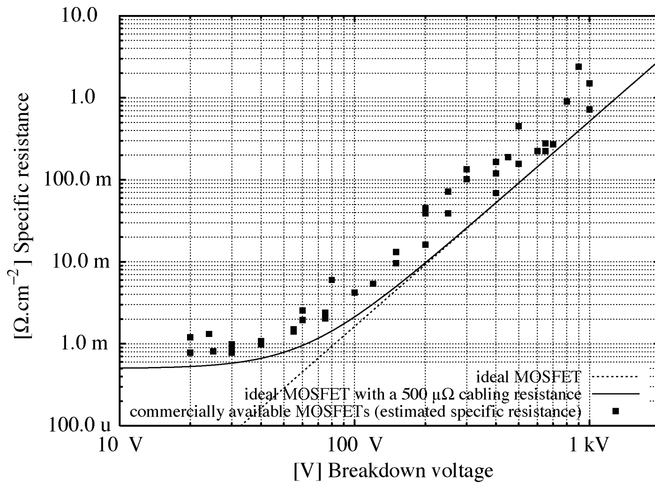

Fig. 2. Evolution of the R_{DSon} with breakdown voltage ratings. Data was computed from R_{DSon} of commercially available devices from International Rectifier, Infineon, and STMicroelectronics packaged in a D2PAK case, assuming 30-mm^2 die area. Ideal R_{DSon} values were calculated using equations in [3].

- blocking state;
- unclamped inductive switching, that may result in avalanche operation;
- avalanche operation caused by vehicle network over-voltage.

The former three items require complete modeling of the static behavior of the transistor, including its body diode. The latter two items are specific to low-voltage automotive converters. Fig. 2 pictures the estimated on-state resistance (R_{DSon}) of commercial MOSFET devices versus their voltage rating. As expected, R_{DSon} increases with voltage rating. To keep high efficiency in converters, transistors with breakdown voltage close to the converter operating voltage are used. This results in avalanche operation of the MOSFETs during turn-off (unclamped inductive switching condition) and during load-dump (an automotive-specific configuration where the battery is disconnected, resulting in a voltage rise on the vehicle electrical network that may exceed transistor breakdown voltage ratings [4]). Therefore, avalanche is then a truly operating mode that has to be correctly simulated.

Due to their low-voltage ratings, automotive converters in the range of several kilowatts have to switch high currents. Surface-mount transistors with 100-A ratings are not uncommon. MOSFET package interconnections behavior has a strong influence on commutation (due to inductive phenomena) and on conduction (package wiring and substrate resistance account for half of the total R_{DSon} as shown in Fig. 3). Interconnection parasitics must be accurately modeled.

Finally, a generic MOSFET model is shown in Fig. 1. Models based on equivalent circuits are widely used for MOSFETs, as they give good results. Furthermore, equivalent circuits can be implemented in any circuit simulator.

III. Models for Low-Voltage Applications

As mentioned above, synchronous rectification is widely used in low-voltage applications. Consequently, the commutation cell becomes an inverter leg. In the rest of this paper, modeling of this structure addresses two issues: the MOSFETs and the circuit interconnection parasitics (mainly resistive and inductive).

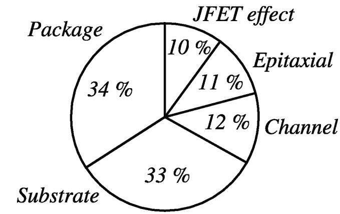

Fig. 3. Contribution of the on-resistance for a 30-V N-channel MOSFET. Source: STMicroelectronics, http://www.st.com

A. Low-Voltage MOSFET Technology

The main characteristic of a low-voltage MOSFET is its on-resistance value (R_{DSon}), as it is directly related to conduction losses. While in high-voltage MOSFETs the epitaxial layer is predominant, this is no longer true for low-voltage technologies (see Figs. 2 and 3).

Channel and JFET-effect resistances are non negligible in MOSFETs. Many authors have proposed solutions to either increase channel width density (thus reduce total channel resistance), or reduce the JFET-effect caused by the MOSFET cell pitch shrinking (trench MOSFET technology addresses this issue [3], [5]).

However, the two main contributions to R_{DSon} (see Fig. 3) are the substrate resistance (due to the silicon die thickness, 200 to 300 μm) and packaging resistance (transistor legs, bond wires). Intensive work is done to reduce this latter resistance: the use of multiple thick bond wires (up to 500 μm in diameter), replacement of bond wires by copper strap, or the use of flip chip approach. All of these methods are already commercially available. Their use in automotive applications is mainly limited by their weakness to thermal cycling (mostly for bondless approaches).

Another feature of automotive power MOSFETs is their ruggedness to avalanche phenomenon. As demonstrated in Section II, avalanche operation is not uncommon in low-voltage converters. This has a strong influence on transistor design.

The main failure mechanism in classical power MOSFETs during avalanche operation is the triggering of the parasitic bipolar transistor. The classical workaround to avoid this triggering is to short emitter and base (source and P implant of the MOSFET) of this bipolar transistor. However, as MOSFET cell pitch is reduced to increase channel density (as stated above), it becomes harder to ensure perfect contact between base and emitter of all the parasitic transistors (i.e., make contact in every cell of the MOSFET). A stripe layout has been proposed [6] to ensure the contact. Basically, stripe-routed transistors have less cells than those using the classical mesh layout, so these cells are bigger (at a given channel density), making contact easier. According to manufacturers such as International Rectifier, failure in avalanche-rated MOSFETs is no longer caused by bipolar transistor locking, but only by thermal limitations.

Finally, another specificity of the automotive environment is high temperature. Automotive-class power MOSFETs have to withstand ambient temperature over 100 °C. These components are usually rated for 175 to 200 °C operating temperature, along with strong thermal cycling. It is worth noting that the main

limitation to the operating temperature of these transistors is due to the packaging (die soldering and bondwire attachments).

B. MOSFET Static Characteristic

The static characteristic of the MOSFET, modelized by the FET M and the wiring resistances R_S and R_D in Fig. 1 is classically written as the function $I_D = f(V_{GS}, V_{DS})$.

The accuracy of this function is of particular interest because it will directly impact the accuracy of the static drain current and drain-to-source voltage estimations, i.e., the conduction losses of the transistor.

Special attention should be given to the linear (triode) area of the static characteristic, where the conducting MOSFET behaves like a resistance (for low V_{DS}). This is supposed to be the normal working mode (low-voltage drop when conducting current), and therefore will have a strong influence on conduction losses.

Two static models are addressed. The first is the Spice level-3 MOS model, originally designed for integrated electronic simulation, but widely used for power MOSFET models due to the large availability of Spice simulators. The second is specifically adapted to power electronics by the implementation of two Kp parameters [7] where the Spice level-3 model only uses one. This gives an extra degree of freedom for curve fitting. This model is inspired from the original approach by Heffner with the insulated gate bipolar transistor (IGBT) model in [8], and it is often implemented in SABER models.

1) Spice Level 3 Model: The level-3 Spice MOSFET model is semi-empirical in that it can be supplied with technological parameters (transistor size, doping, etc.) or with data from experimental identification. A simplified equation is as follows:

$$I_D = 0, \text{ for } V_{GS} < V_{th} \tag{1}$$

$$Ids = \beta \left[V_{GS} - V_{th} - (1 + f_b)\frac{V_{DS}}{2} \right] V_{DS} \quad \text{for } V_{GS} \geq V_{th} \tag{2}$$

with $\beta = K_P(W/L)$, K_P is the transconductance parameter and W and L are, respectively, the channel width and length. f_b is a correction factor required for short channel effects and narrow channel width effects [9]. For a power MOSFET (vertical MOSFET), V_{th} can be written as

$$V_{th} = V_T - \sigma V_{DS}. \tag{3}$$

2) Kp model: This model is close to the Spice level-3 MOSFET model, except that the K_P parameter is replaced by $K_{P_{lin}}$ and $K_{P_{sat}}$ to enable different values for K_P in linear and saturation regions, respectively. Drain current can therefore be written as

$$I_D = 0, \text{ for } V_{GS} < V_{th} \tag{4}$$

$$I_D = K_{P_{lin}} \frac{(V_{GS} - V_{th})V_{DS} - \frac{K_{P_{lin}}}{2K_{P_{sat}}} V_{DS}^2}{1 + \theta(V_{GS} - V_{th})} \quad \text{for } V_{DS} \leq (V_{GS} - V_{th})\frac{K_{P_{sat}}}{K_{P_{lin}}} \tag{5}$$

$$I_D = K_{P_{sat}} \frac{(V_{GS} - V_{th})^2}{2[1 + \theta(V_{GS} - V_{th})]} \quad \text{for } V_{DS} > (V_{GS} - V_{th})\frac{K_{P_{sat}}}{K_{P_{lin}}}. \tag{6}$$

As with the Spice model, the σ parameter expresses the dependence of the threshold voltage with the drain-to-source voltage using (3).

C. Capacitances

Due to its MOS structure, the MOSFET exhibits two capacitances—gate-to-drain C_{GS} and gate-to-source C_{GS} (a third, due to the drain-source junction is taken into account in the diode model). These capacitances have a strong effect on transistor dynamics: as they are both connected to the gate, they must be charged (respectively discharged) to turn-on (respectively turn-off) the transistor. Their rate of charge will therefore determine the switching speed of the transistor [10]. Moreover, the gate-drain capacitance (C_{GD}) causes the Miller effect: during the transistor commutation, its drain potential varies, resulting in a capacitive current through C_{GD} that increases the amount of charge to supply (or to extract) to turn-on the transistor (respectively turn-off).

These capacitances must be represented to achieve good simulation of the MOSFET commutations. Unfortunately, they are nonlinear and strongly depend on the voltage. Budihardjo *et al.* wrote that these nonlinearities need to be modeled accurately [2], but in most of the available MOSFET models, only the nonlinearities of C_{GD} are considered. C_{GS} is supposed as constant in most models as it is mainly caused by the proximity between gate and source electrodes (forming a capacitance with two metal electrodes), and because of the predominance of C_{GD}—due to the Miller effect—during commutations.

The classical capacitance model that is used in this paper uses a constant capacitance C_{GS} for the gate-to-source capacitance, and expresses the gate-to-drain capacitance as

$$C_{GD} = \begin{cases} C_{oxd}, & \text{for } V_{GD} \leq 0 \\ \frac{C_{oxd} \cdot C_{gdj}}{C_{oxd} + C_{gdj}}, & \text{for } V_{GD} > 0. \end{cases} \tag{7}$$

With the capacitance C_{gdj}, corresponding to the capacitance of the space-charge region written as

$$C_{gdj} = \frac{\epsilon_{Si} A_{GD}}{\sqrt{\frac{2\epsilon_{Si} V_{GD}}{qN}}}. \tag{8}$$

D. Diode

1) Standard Spice PN Junction Model: Such a model is usually not suitable for power electronic applications, because high level injection is not considered in the diode epitaxial base.

To obtain "good" agreement the following are required:

- I_S for low current forward characteristic;
- R_S for high current forward characteristic;
- V_{bi} may be adjusted for the threshold agreement;
- C_{j0} is obtained from capacitance measurement at $V_{AK} = 0$ V;

- TT is set to the ambipolar lifetime but it turns out to be unsatisfactory [11].

2) Considering High-Level Injection: High level injection should be considered in the diode model. Analytical circuit models have been reported in literature [12]. However, a refined diode model is not significant for the system simulation as the diode is only scarcely solicitated in high injection in the specific case of a synchronous inverter.

Authors have noted the short ambipolar lifetime of the body diodes of the commercial MOSFET for automotive applications.

3) Behavior Under Avalanche Conditions: The avalanche operation is stressful as it involves high loss levels and therefore temperature cycling. Furthermore, manufacturing tolerances on breakdown voltage (V_{BR}) are wide (several volts for a 20-V-rated transistor). This can make paralleling of transistors under avalanche operation difficult, as the transistor with the lowest V_{BR} of the assembly has to sustain all the avalanche current. Fortunately, this breakdown voltage has a positive-coefficient dependence with temperature, so it is usually considered that in a parallel assembly, a transistor with the lowest V_{BR} conducts first, self-heats, resulting in a V_{BR} increase up to the V_{BR} of the remaining MOSFETs of the assembly [13].

It has been shown in [14] that V_{BR} is not only temperature-dependent, but also strongly related to the drain current. A specific resistance of the avalanche path, several times higher than the R_{DSon} has a strong influence on the breakdown voltage. Therefore, during avalanche, the following expression has been proposed:

$$V_{BR} = V_{BR0} + \gamma T + R_{BR} I_D. \tag{9}$$

E. Thermal Issues

As indicated in Section III-D-3, temperature has a strong influence on transistor behavior. Temperature transients are very slow compared to electrical commutation speed. A thermal model must therefore take into account the propagation of heat.

Analytical resolutions of the heat equation have been proposed by many authors [15]. Their main drawback is the impossibility to implement them in a classical circuit simulator. To overcome this limitation, a discretization of the heat equation as a thermal RC circuit, using for example the finite differences method, is classically used [16].

Assuming the thermal assembly can be considered as a unidimensional system, with constant-step discretization h, values of R_{th} and C_{th} can be written as

$$R_{TH} = \frac{h}{K A_{MOS}} \tag{10}$$

$$C_{TH} = h A_{MOS} \rho c \tag{11}$$

where R_{TH} and C_{TH} are the elementary resistance and capacitance of the thermal network, K, ρ, and c are, respectively, the thermal conductivity, the density, and the specific heat of the material, and A_{MOS} is the surface of the assembly.

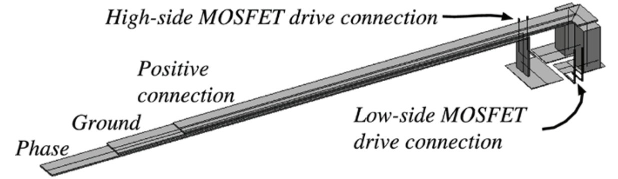

Fig. 4. Structure of the commutation cell as described with InCa. Long copper busbars are mandatory to connect the cell when in the calorimeter described in Section V.

F. Interconnection Model

It has been shown by many authors that interconnection has a strong influence on switching waveforms in power converters [17], [18]. This is due to the high-frequency switching operation, that leads to very fast current and voltage transients, where parasitic capacitances and inductances—due to the circuit layout—will play a major role.

In low-voltage power electronics, the major concern is related to the current transients: when keeping converter output power constant, lowering voltage results in higher currents. Converters rated at several kilowatts under 12 V switch currents of several hundreds of amps. Therefore, special care will be given to parasitic inductance modeling. Moreover, the resisitive aspect of the interconnections also deserves modeling: MOSFETs with R_{DSon} lower than 3 mΩ are not uncommon, while a thick (100 to 200 μm) and short (one or two centimeters) track of copper printed circuit board (PCB) is rated at some fractions of a milliohm. Interconnection resistive parasitics are then comparable to the MOSFET R_{DSon}.

In experiments described hereafter, interconnection modeling is performed using specific software $(InCa)$ [19], based on the partial elements equivalent circuits (PEEC) method, first introduced by Ruehli [20]. Using this method, a circuit layout can be modelized by one inductance and one resistance per connection. This allows for easy integration of the model into a circuit simulator.

$InCa$ requires a complete three-dimensional (3-D) description of the geometrical structure of the converter. A picture of the 3-D model of the converter studied in this paper is shown in Fig. 4. The structure of this converter, using long, thin copper busbars is required for use with a calorimeter (which allows it to connect the converter—which is in the calorimeter—with the power supplies—which are outside). As these busbars are relatively long, their parasitics are not negligible and have to be modeled. Description of the calorimetric test setup is given in Section V.

IV. Parameter Extraction

In the previous section, the models of the MOSFET transistor and the circuit connections were introduced. Parameters of the interconnection model are computed from a 3-D description of the layout. Unfortunately, for the MOSFET transistors, parameters of the model cannot be obtained directly, as vendors keep their manufacturing process secret.

A way to obtain the transistor model parameters is the identification with experimental results. Classical parameter extraction methods use static and frequency-based measurements to identify most of the components of the model in Fig. 1 [9]. These

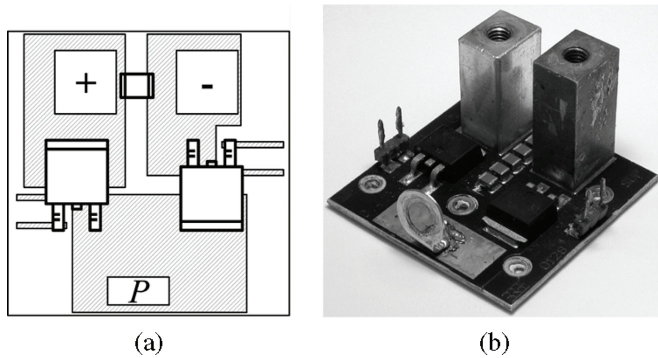

Fig. 5. (a) Drawing and (b) photography of the commutation cell.

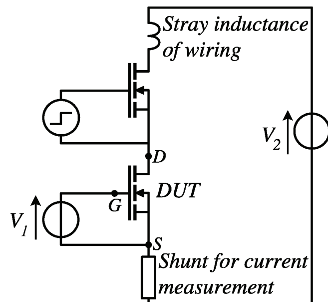

Fig. 6. Circuit for the MOSFET static characterization.

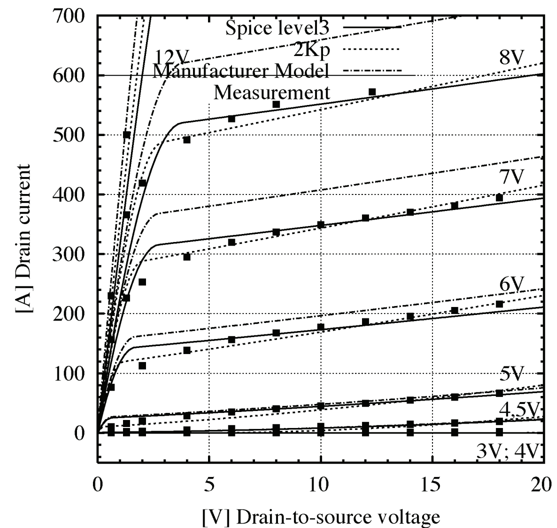

Fig. 7. Measured and simulated static characteristic of a STB210NF02 MOSFET transistor using the test setup in Fig. 6.

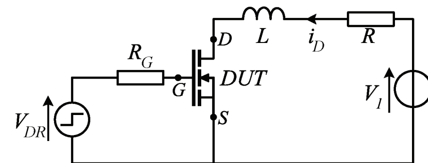

Fig. 8. Circuit for the unclamped inductive switching (UIS) test.

methods are widely used in microelectronics, but impose conditions far from power transistor normal operating conditions.

Methods based on time-domain measurements are preferred. Their main advantage is to use the transistor in its nominal operating conditions. This can result in large power dissipation of the device under test (DUT), what leads to temperature rise. This must be avoided as temperature has a strong effect on MOSFET characteristics. Special care is therefore taken to limit power dissipation during parameter estimation.

A. Static Characteristic Identification

Self-heating of the DUT is the major concern in static characteristic measurements. Instantaneous power dissipation can be high as some experimental points require simultaneously large drain current and drain-to-source voltage.

Static characteristics of transistors are classically obtained by using curve-tracer. For power components, this apparatus uses pulsed measurements with very low duty-cycle to avoid heating of the DUT.

However, the size of the test fixture of the curve tracer (Tektronix 371A), has a nonnegligible parasitic inductance. That inductance slows current rise during measurement pulses and thus causes the curve tracer to generate larger pulses (more than 80 μs). This is sufficient increase the temperature of the DUT. This phenomenon is specific to low-voltage transistors, as low-voltage means slow current transients (small $L(dI_D/dt)$) and high currents.

A specific test bench has been developed to enable short power pulses. It is depicted in Fig. 6, and uses two identical MOSFETs. One, the DUT, has its gate biased by a continuous voltage, while the second is used to generate power pulses. Variable drain-to-source voltage is obtained using a capacitor bank (about 1 mF ceramic and 80 mF electrolytic). Drain current is measured using a T&M SDN-005 aselfic shunt resistor. Total wiring inductance is kept low by reducing the total circuit length to a few centimeters. Such a system can generate current pulses as high as 700 A at drain-to-source voltage below 1 V with a total pulse duration below 20 μs.

A simulated-annealing algorithm [21] is then used to fit the model parameters to experimental data. Results are plotted in Fig. 7. Spice level-3 and 2-Kp model plots are obtained through the identification process, while the manufacturer's model is shown for the sake of comparison. It can be seen that this latter model was optimized for the linear region $(V_{DS} < V_{GS} - V_{TH})$.

As can be seen in Fig. 7, *Spice* level-3 and 2-Kp models (whose parameters were identified by authors) give both satisfying results in the linear and in the saturation region of operation. The manufacturer's model corresponds well in the linear region, but an important mismatch is visible in the saturation region. In power converters, MOSFETs operate in the saturation region during commutation, so the manufacturer's model is unsuitable for commutation losses and waveform prediction. Spice level-3 and the 2-Kp static characteristic models are both suitable for accurate simulation.

B. Unclamped Inductive Switching (UIS) Test

The second identification circuit is the unclamped inductive switching test circuit (UIS), shown in Fig. 8. It is used for the identification of the MOSFET transistor capacitances (C_{GS}, C_{GD}, and the body diode junction capacitance). It replaces the classical frequency-domain measurements.

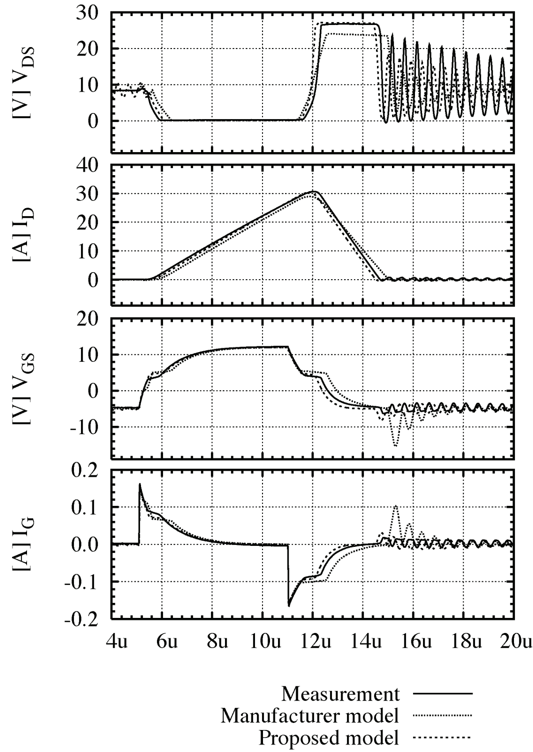

Fig. 9. Measured and simulated voltage and current during the Unclamped inductive commutation, with $R_G = 102\ \Omega$, using the test setup in Fig. 8, and a STB210NF02 MOSFET transistor. Avalanche phenomenon can be noticed during turn-off of the transistor (for t = 12 to 14.2 μs).

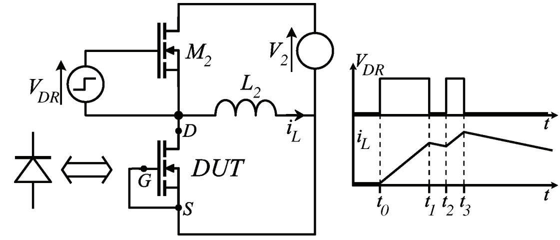

Fig. 10. Circuit for the diode dynamics characterization.

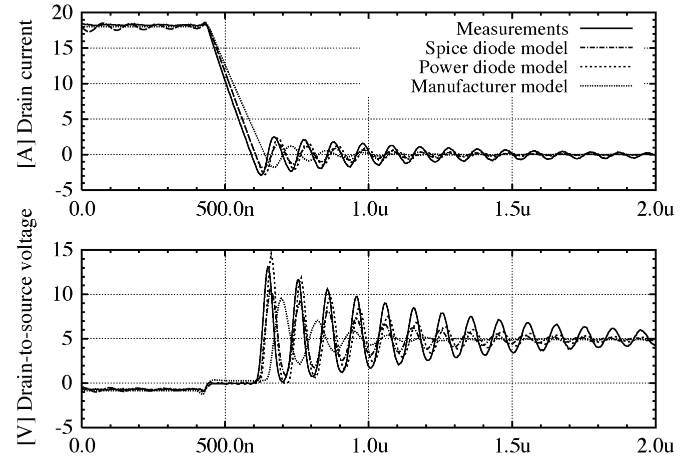

Fig. 11. Measured and simulated voltage and current during opening of the diode of a STB210NF02 MOSFET, with $I_D = 18$ A and $V_{DS} = 5$ V, using the test circuit of Fig. 10.

This circuit is simulated, and results (waveforms of V_{DS}, V_{GS}, I_D and I_G) are compared with measurements, and capacitances parameters are adjusted to obtain good correlation.

As the UIS circuit uses switching, special attention should be paid to the circuit layout model. Inductive and resistive parameters of the interconnection are either identified using fast switchings of the circuit (if the MOSFET is driven fast enough, switching speed of the circuit is mostly dependant on the wiring parasitics) or computed using $InCa$.

During UIS measurement, a large gate resistance is used (typically 100 Ω). This ensures a slow commutation, whose speed is imposed by the charging rate of the transistor capacitances. Results of the identification are plotted in Fig. 9. A good agreement is reached between experimental and simulated waveforms using the classical nonlinear MOSFET capacitances model, providing a good set of parameters is used.

It can be seen in Fig. 9 that the proposed model gives satisfying results (with parameters identified by authors). The manufacturer's model uses the same equations, but with a different set of parameters. Evolution of V_{DS} during turn-off ($t = 12\ \mu$s) does not correspond with experimental waveform, because of different MOSFET capacitances parameters, but also because of different static characteristic models (the MOSFET transistor works in the saturation region during commutation).

C. Reverse Recovery Test

Modeling of the body diode of the MOSFET transistor is mandatory in low-voltage power converters, as they are based on an inverter commutation cell. The main characteristic of a power diode in a switching converter is the reverse-recovery phenomenon. The test circuit in Fig. 10 enables a recovery phenomenon to occur in the DUT. It uses two identical transistors. Gate and source of the DUT are shorted to keep only its body diode, while the second transistor is used to charge the inductance and trigger the recovery phenomenon in the DUT.

As switching phenomena are very fast events (some tens to hundreds of nanoseconds), it is necessary to use an inductance as current source in this circuit. An electronically-regulated current source would be far too slow to maintain constant current during the commutation. The inductance that is used is a high-bandwidth air coil.

Simulations of this test circuit are performed to compare computed and measured drain current and drain-to-source voltage. Parameters are adjusted to obtain good matching. The initial values of parameter A can be assessed from the die surface of the transistor (26 mm^2). A good initial estimate of W and N values is given using the breakdown voltage rating [3].

As this test circuit is a fast switching circuit, good accuracy can only be achieved through circuit parasitics modeling. Then internal MOSFET transistor interconnection parasitics can be identified on the waveforms in Figs. 11 and 12 by fitting simulated results on the drain current decreasing slope and the corresponding drain-to-source voltage plateau (around 500 ns in Figs. 11 and 12). It is obvious that circuit inductance must be kept low to ensure fast current transients during recovery.

Good agreement between simulated and measured waveforms is reached using both the power and Spice diode models. This is unusual in power electronics, as the Spice model does not represent correctly the reverse recovery phenomenon [11].

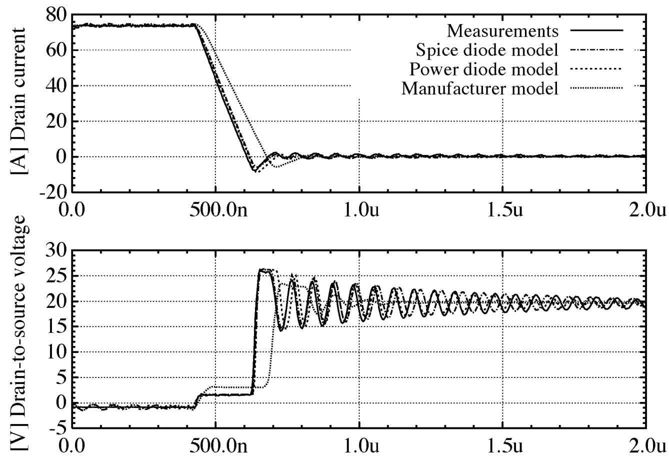

Fig. 12. Measured and simulated voltage and current during opening of the diode of a STB210NF02 MOSFET, with $I_D = 70$ A and $V_{DS} = 20$ V, using the test circuit of Fig. 10.

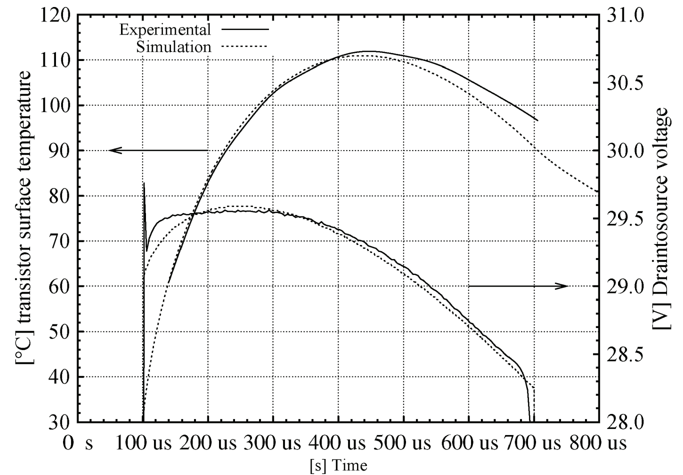

Fig. 13. Comparison between experimental and simulated drain-to-source voltage and transistor temperature during avalanche.

Several specificities of low voltage converters help to explain the good results obtained using the classical Spice model: low-voltage yields to low-current transient (small $L(dI_D/dt)$), which in turn reduces peak reverse recovery current. Then, the body diode of the studied MOSFET transistor is very fast (identified ambipolar lifetime of 25 ns). Finally, it has been indicated that the diode is only solicited for a short time in high-level injection operation during a switching cycle.

The manufacturer's model is based on the Spice diode model, but has a different set of parameters. Results in Figs. 11 and 12 show that this model is unsuitable for commutation simulation, as simulated waveforms differ strongly from experimental data.

D. Avalanche and Thermal Characterization

A test circuit, allowing for accurate identification of the thermoelectrical parameters of the avalanche behavior of the low-voltage MOSFET transistor has been described in detail in [14]. Using this circuit, it is possible to measure not only drain current and drain-to-source voltage waveforms, but also to estimate transient transistor die temperature during avalanche.

In addition to the identification of these three electrothermal parameters (V_{BR0}, γ and R_{BR}), parameters of the thermal network must be computed using (10) and (11). The thermal model uses 100 $R_{TH} - C_{TH}$ cells to represent the transistor die thickness.

A comparison between experimental and simulated drain-to-source and transistor temperature is shown in Fig. 13. Good agreement is achieved from time $=$ 100 μs to 500 μs. Over this time, the thermal model must include accurate description of not only the transistor silicon die, but also the copper heat spreader it is soldered on and the remainder of the thermal assembly (copper tracks, heat sink, etc.). Such thermal modeling is beyond the scope of the present paper.

V. VALIDATION

A summary of all identified parameters, for Spice and power models is given in Table I. In this section, simulations using these models are compared to experimental data.

Four complete MOSFET transistors are used, with a combination of Spice and power models for static characteristics and

TABLE I
PARAMETERS OF THE STB210NF02 MOSFET TRANSISTOR MODELS

Static characteristic			
Spice level-3		2KP	
Parameter	Value	Parameter	Value
K_P	162 $A.V^{-2}$	$K_{P_{lin}}$	256 $A.V^{-2}$
η	0.01	$K_{P_{sat}}$	201 $A.V^{-2}$
θ	0.201	θ	0.298
σ	0	σ	0.0374
V_T	4.4 V	V_T	4.66 V
Diode model			
Spice		power	
Parameter	Value	Parameter	Value
I_S	0.03 nA	W	1.6 μm
C_{JO}	0.519 nF	A	13 mm^2
TT	15 ns	τ_A	22.5 ns
V_J	0.768 V	τ_D	40 ns
M	0.325	α	0.01
R_S	0.25 $m\Omega$	N	3.10^{16} cm^{-3}
		V_{bi}	0.63 V
		V_{n0}	0.028
		V_{BR_0}	26.9 V
		γ	14.8 $mV.K^{-1}$
		R_{BR}	12.1 $m\Omega$
Capacitances and package models			
Capacitances		Package interconnection	
Parameter	Value	Parameter	Value
A_{GD}	0.25 cm^2	R_G	4 Ω
C_{oxd}	6 nF	R_S	800 $\mu\Omega$
C_{GS}	3.3 nF	R_D	200 $\mu\Omega$
		L_G	10 nH
		L_S	4 nH
		L_D	2 nH

diode (see Table II). Other parameters of Table I are the same for all models, except for the manufacturer's model, using its own set of parameters.

TABLE II
MOSFET TRANSISTOR MODELS OBTAINED BY A COMBINATION OF ELEMENTARY MODELS

Model	static characteristic	diode
Spice level-3	level-3	Power model
Spice diode	2Kp	*Spice* diode model
power	2Kp	Power model
Manufacturer	level-3	*Spice* diode model

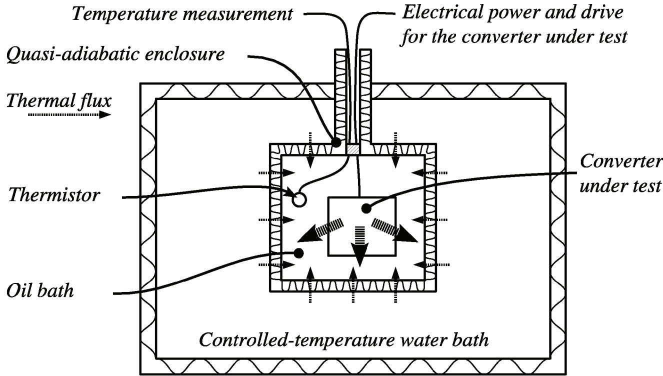

Fig. 14. Principle of the energy-calorimeter used.

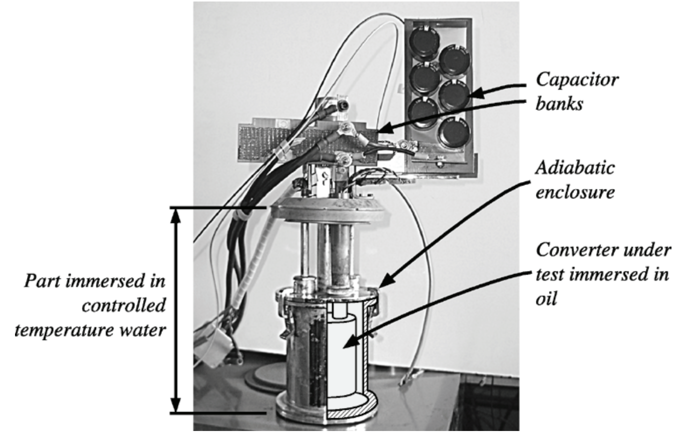

Fig. 15. Photography of the calorimeter head.

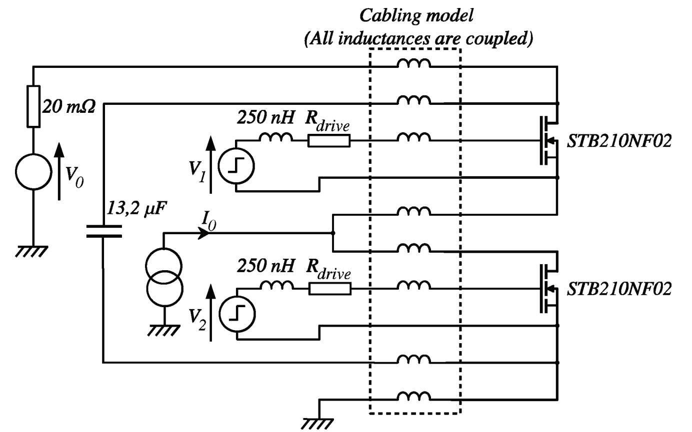

Fig. 16. Complete schema used for loss simulation.

A. Calorimeter Setup

Calorimetric measurements are the most accurate way to obtain power converter overall losses. Electrical measurements suffer severe limitations due to the high switching speed of power electronics (this requires high-bandwidth voltage and current acquisition). Moreover, as electrical measurements require $P_{\text{input}} - P_{\text{output}}$ computation and as converter efficiency is high, the results are prone to great inaccuracy [22].

Compared to the calorimeters described in [22], which measure dissipated power in continuous operation, the calorimeter described here measures energy (see Fig. 14). The converter under test is placed in an adiabatic enclosure, filled with oil. This enclosure is immersed in a controlled-temperature bath, in order to keep the unavoidable heat leakages constant.

When the converter under test operates, it dissipates power that, in turn, makes the oil temperature increase. As the specific heat of the adiabatic enclosure (i.e., of oil, converter, and measurement devices) is known (through experimental calibration), dissipated energy can be calculated from the oil temperature rise.

An external control system enables the converter under test to operate for a precise length of time. This allows calculation of the dissipated power from the dissipated energy measurement.

The converter under test is the commutation cell pictured in Figs. 4 and 5. The long busbar visible in Fig. 4 is used to connect the commutation cell itself with power supplies that are kept outside the calorimeter. Fig. 15 shows the calorimeter head, with the capacitor bank directly connected to the busbar extremity.

The schema of Fig. 16 was used to perform loss simulations.

B. Results

Simulation and measurements were performed with varying gate resistance, dead-time between turn-off of a transistor and turn-on of the other, load current, and supply voltage. For the sake of brevity, only one load current and supply voltage are considered here. For each set of parameters, measurement and simulation were performed at several switching frequencies. This allows for separation between conduction and commutation losses. Converter energy losses during one commutation cycle can be written as (considering that on and off state refer to the state of the low-side transistor of the inverter leg)

$$E_{\text{total}} = P_{\text{off}} t_{\text{off}} + E_{\text{on}} + P_{\text{on}} t_{\text{on}} + E_{\text{off}} \quad (12)$$

where P_{off} and t_{off} are conduction losses and duration in the off-state (P_{on} and t_{on} refer to the on-state), and E_{on} and E_{off} are commutation energies to switch to on and off states, respectively.

Providing low and high-side transistors of the low-voltage commutation cell (inverter leg) are identical, P_{off} and P_{on} are the same. Moreover, $t_{\text{on}} + t_{\text{off}} = (1/F)$, with F the switching frequency. Therefore, the total power dissipation may be estimated as

$$P_{\text{total}} = E_{\text{total}} F \quad (13)$$
$$= P_{\text{off}} + P_{\text{on}} + (E_{\text{on}} + E_{\text{off}})F \quad (14)$$
$$= P_{\text{cond.}} + E_{\text{commut.}}.F. \quad (15)$$

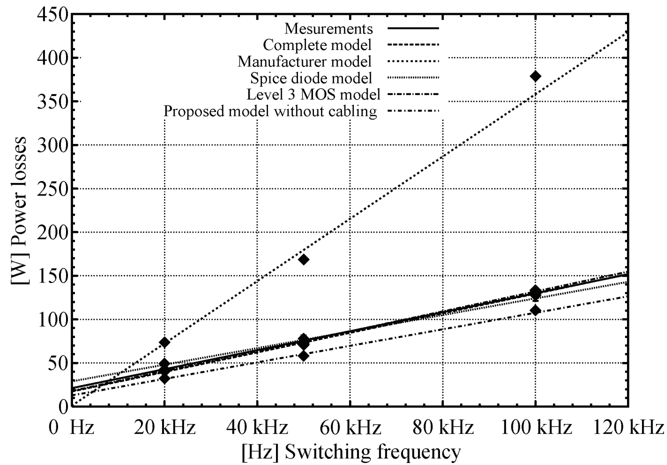

Fig. 17. Evolution of measured and simulated losses with the switching frequency. DC voltage is 20 V, load current 70 A, driving resistors are 100 Ω and dead time is 2 μs. STB210NF02 MOSFETs are used.

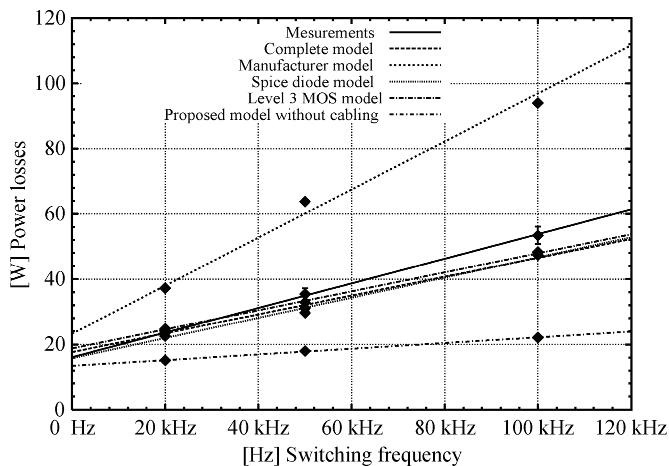

Fig. 18. Evolution of measured and simulated losses with the switching frequency. DC voltage is 20 V, load current 70 A, driving resistors are 2 Ω and dead time is 400 ns. STB210NF02 MOSFETs are used.

It is therefore possible to discriminate between conduction power losses ($P_{\rm cond.}$) and commutation energy ($E_{\rm commut.}$) by performing loss measurement at two different switching frequencies.

Fig. 17 presents experimental and simulation results for a "slow" commutating converter (high dead-time and gate resistance). The manufacturer's model is very inaccurate in commutation loss estimation (corresponding to the slope of the curve) as transistors impose the commutation speed. A bad transistor model results in very poor loss estimation. Results of Fig. 18 were obtained for a "fast" commutating converter (short dead-time and low gate resistance). In this case, commutation speed is mainly limited by the interconnections, and the transistor model has lower (but still high) influence on computed losses.

Interconnection influence on losses can be seen in Figs. 17 and 18 as simulations were performed using the power MOSFET model, but without any interconnection model. In Fig. 17, the gap between experimental and simulated results when considering no interconnection is almost independent of the switching frequency. This means that losses in wiring are conduction losses, i.e., when commutating"slowly," the inductive aspect of the interconnection is negligible. When commutating "quickly" (see Fig. 18), the difference between experimental and simulation results (when considering no interconnection model) is strongly dependent on the switching frequency. Therefore, $E_{\rm commut.}$ is strongly affected by the wiring: the inductive parasitics account for most of the commutation losses.

In Figs. 17 and 18, it can be seen that the three models with parameters identified by the authors give very good results. This proves that for low-voltage power electronics, classical Spice models can be suitable, providing care is given to parameter identification.

VI. Discussion

The comparison between Spice and Power-specific MOSFETs models which is described in this paper demonstrates that both are suitable for converter simulation. This is unusual in power electronics, because the lack of high-injection consideration in Spice diode model makes it inaccurate in most applications.

However, for the low-voltage MOSFET transistors studied here, body diodes were found to be very fast, while commutation speed is quite low. Inductive parasitics of the interconnections (circuit and transistor packaging) limit the current slope during switching, reducing commutation speed. This results in a low level of reverse recovery in the body diode. In this case, Spice models are acceptable for power electronics simulation.

It is worth noting that the increase on vehicle network voltage (42 V or more) should both result in faster commutation transients and in slower switching devices (high-voltage MOSFETs or IGBTs). The validation method used in this paper should help the limits of a given model.

In the case of avalanche simulation, the model has to include electro-thermal coupling, as the drain-to-source voltage is mainly related to the transistor temperature and to the drain current. This is not obvious in a single-transistor per switch setup (as in the converter described in this paper), but is very important when paralleling devices [23], because it has a strong effect on current sharing.

The manufacturer's model, using Spice models, was proven to be very inaccurate because of inappropriate parameters. This shows that parameter identification is a very important operation, and that power-electronics specific identification methods should be used to ensure accuracy.

VII. Conclusion

This paper focuses on automotive (low-voltage, high-current) power electronics simulation. In such a mass-market, the simulation of converters is mandatory both to speed design process and gain accurate understanding of converter performances.

Description of the different modes of operation of the main component of the low-voltage commutation cell (the MOSFET transistor) shows that its body diode, as well as its package parasitics have a strong influence on converter operation. Two MOSFET transistor models, using either standard Spice or power-electronics dedicated models are then described.

Special care is taken in the identification of the model parameters, which requires specific test circuits. The advantage of this method is that it is close to the transistor normal operating

conditions compared to frequency or small-signal-based identification methods. A model of the interconnection is computed using commercial software.

A demanding validation method is used: comparison of measured and simulated losses of a complete commutation cell (including two MOSFET transistors, a capacitor and their interconnection). Measurements are performed using a calorimeter, to ensure reliable results.

As a conclusion, it is shown that both standard Spice and power-electronic-specific models give good results, providing the set of parameters was identified carefully.

The interconnection model is also very important, both with inductive and resistive parasitics because of the high-current levels required in low-voltage converters. Wiring parasitics must be modeled for accurate simulation.

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