

# A 14-Band Low Complexity & High Performance Synthesizer Architecture for MB-OFDM Communication

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**Abstract**—This work presents a 14-band low complexity and high performance synthesizer architecture for MultiBand Orthogonal Frequency Division Multiplexing operating in the range of 3.1 to 10.6 GHz. The synthesizer uses a single PLL with trivial divide-by-2 circuits, single side band mixers, low complexity filters, and multiplexers. Specifications of the synthesizer components are chosen in order to minimize the total spurs power and respect the IEEE802.15.3a recommendations.

**Index Terms**—Frequency synthesizer, single side band mixer, ultra wide band, multiband orthogonal frequency division multiplexing.

## I. INTRODUCTION

ULTRAWIDE Band (UWB) transmissions can be used for USB wireless, Wireless 1394, and Personal Area Networks (PANs) with small radio coverage and high data rates (up to 480 Mbps at 10 meters). These emerging applications spurred new standardization efforts and two proposals were promoted within the IEEE802.15.3a Task Group: direct-sequence impulse communication and MultiBand Orthogonal Frequency Division Multiplexing (MB-OFDM) systems.

The efforts of the manufacturers to occupy the allocated band is important. The WiMedia Alliance proposal, an amalgamation of the WiMedia and MultiBand OFDM Alliance, divides the 7.5 GHz bandwidth into 14 channels of 528 MHz bandwidth [1] (Fig. 1), where band used is in a predefined order. The “Mode 1” is mandatory and consists of the three lower channels. The use of the other channels is optional at the moment.

Due to low cost requirements for consumer product application, the UWB radio should have low complexity, low power consumption, and highly integrable. The most promising architecture is thus the zero-IF architecture. Therefore, the frequency synthesizer has the function of generating the center frequency of all the channels. The transition time between two frequencies must be lower than 9.47 nsec [1]. In order to have a negligible degradation of the sensitivity; i.e. less than 0.1 dB, it has been shown [2] that the synthesizer must satisfy two criteria: the total synthesizer spurs power in the 7.5

GHz bandwidth must be less than -24 dBc compared to the desired frequency power and the phase noise of the generated frequency should be below -86.5 dBc/Hz at 1 MHz.

The generation of the center frequencies can not be done using a conventional Phase-Locked Loop (PLL) because the PLL locking transient takes a long time and requires a 10 GHz reference frequency due to the settling time. In order to have a very short switching time, the common idea consists of generating all the desired frequencies and choosing of them with multiplexers.

Most work focuses on the “Mode 1” [3]- [4] and some frequency synthesizers generate frequencies corresponding to “Mode 1” with 4 additional frequencies [5], [6]. To the authors’ knowledge, there are only three proposals that could generate all 14 frequencies [7], [8] and [2].

In [7], the synthesizer proposal describes an approach for generating the 14 frequencies without the details of the architecture. The synthesizer proposed in [8] consists of 3 Single Side Band (SSB) mixers, filters, 2 PLLs, and a series of different frequency dividers. The main disadvantage of this architecture is the silicon area used due to the two PLLs, and a high performance broad-band tunable filter spanning several gigahertz. In [2], the frequency synthesizer consists of 5 SSB mixers, filters (low pass filters are not shown), a single PLL, and a series of trivial frequency dividers (top of Fig. 7). This architecture has a good compromise between performance and silicon area because of the single PLL. However the shortcomings of this architecture come from three of the five SSB mixers and the reconfigurable filtering which must be broad-band. The nonidealities expected from an integrated implementation could consequently yield a non negligible spur level. The aim of this paper is to present a low complexity and high performance synthesizer architecture that generates the 14 channel center frequencies according to the previous specifications.

Section II presents the proposed architecture and its advantages. Then the synthesizer specifications are given in Section III. The simulation results are discussed in section IV. Finally we conclude in Section V.

## II. PROPOSAL OF A LOW COMPLEXITY SYNTHESIZER

In [2], the synthesizer generates 5 main frequencies and up/down convert these frequencies by a shift of 528 MHz in order to obtain the 14 desired frequencies. The generation of

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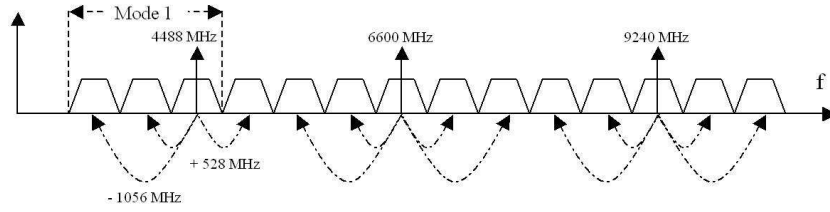


Fig. 1. Frequency plan from the MB-OFDM proposal and principle of the proposed architecture

these 5 main frequencies requires very constraining components such as a broad-band SSB mixer (top of Fig. 7, mixer III) and a broad-band reconfigurable band pass filter. According to the nonidealities expected from an integrated implementation of a reconfigurable bandpass filter, the order of magnitude of the deviation of the center frequency could be over ten of percent and where it could consequently yield a non negligible spurs level before the last up/down conversion.

To avoid such components, we propose to use only 3 main frequencies generated by SSB mixers with fixed inputs and outputs frequencies. The principle of our architecture is given in Fig. 1: (1) generation of 3 main center frequencies at 4488, 6600 and 9240 MHz; (2) up/down conversion of these frequencies by a shift of 528 or 1056 MHz in order to obtain the 14 center frequencies. The only broad-band SSB mixer is the one that up/down converts the 3 main frequencies. The proposed architecture is composed of a single PLL at 4224 MHz, 4 divide-by-2 circuits, 5 SSB mixers and filters (bottom of Fig. 7).

The key component of our synthesizer is the SSB mixer. The SSB mixer is built with the widely used configuration of 4 Double Side Band (DSB) mixers (Fig. 2). The inputs must be in quadrature while the selection of the upper or lower sideband is done according to the phase sign between the quadrature inputs. A divide-by-2 circuit is built with D-latch and provides perfect  $I$  and  $Q$  signals. The inversion of polarity between SSB quadrature inputs could be performed by directly choosing  $Q$  or its complementary  $\bar{Q}$  at the D-latch output (Fig. 7).

A large bandwidth implies a non-optimized adaptation circuit where it leads to an increase of insertion loss. A summary of the SSB mixers bandwidth is given in Table I, where it compares the complexity of our architecture and the architecture of [2].

TABLE I  
SSB MIXERS BANDWIDTH OF SYNTHESIZER DESCRIBED IN [2] AND  
PROPOSED ARCHITECTURE

| SSB mixer   | Synthesizer described in [2] |    |     |     |     | Proposed Synthesizer |    |     |    |   |
|---|------------------------------|----|-----|-----|-----|----------------------|----|-----|----|---|
|   | I                            | II | III | IV  | V   | I                    | II | III | IV | V |
| $\frac{F_{\max}}{F_{\min}}$ 1 <sup>st</sup> input | 1                            | 1  | 1   | 1   | 1   | 1                    | 1  | 1   | 1  | 2 |
| $\frac{F_{\max}}{F_{\min}}$ 2 <sup>nd</sup> input | 1                            | 1  | 3   | 2.2 | 2.9 | 1                    | 1  | 1   | 1  | 2 |
| $\frac{F_{\max}}{F_{\min}}$ output                | 1                            | 1  | 2.6 | 2.1 | 2.6 | 1                    | 1  | 1   | 1  | 3 |

### III. SYNTHESIZER SPECIFICATIONS

The total synthesizer spurs power in the 7.5 GHz bandwidth must be less than -24 dBc compared to the desired frequency

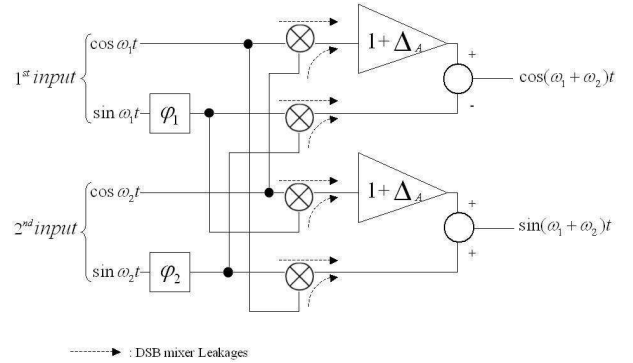


Fig. 2. SSB mixer with upconverter input configuration

power. Since the spurs generated by our synthesizer come from divide-by-2 circuits and SSB mixers, we have the following:

- The divide-by-2 outputs are always rectangular waves and have significant odd harmonic content. We must minimize their power by low-pass filtering.
- Perfect image rejection is possible at the SSB outputs only if the amplitude of DSB outputs are equal ( $\Delta_A = 0$ ) and if the inputs are strictly in quadrature ( $\varphi_1 = \varphi_2 = 0^\circ$ ). But if the DSB mixers don't have strictly the same conversion gain corresponding to  $\Delta_A \neq 0$ , and lengths of line between mixers are not strictly equal then perfect quadrature between inputs is not possible ( $\varphi_1, \varphi_2 \neq 0^\circ$ ), see Fig. 2. Moreover the DSB mixers do not have perfect isolation yielding leakages ( $L_{dB}$ ).

Thus, spurs power level depends on 5 parameters:  $\varphi_1$ ,  $\varphi_2$ ,  $\Delta_A$ ,  $L_{dB}$ , and the attenuation of harmonic of divide-by-2 outputs. In the following subsections, we study the SSB and the filters specifications required to respect the standard.

#### A. SSB mixer specifications

The total spurs power of the desired frequencies highly depends on the spurs power generated by the last SSB mixer. Thus, we have to characterize as best we can the last SSB mixer specifications.

We assume that the inputs of the last SSB are perfectly well filtered and spectrally pure. The spurs generated only depend on the gain and phase mismatches, and the DSB leakages. For the following discussion, we focus on the spurs level at the SSB quadrature output. The performance of the SSB inphase output is similar and will not be detailed in this paper.

The power of the desired signal is [2]

$$signal_Q = \frac{1 + 2(1 + \Delta_A) \cos(\varphi_1 - \varphi_2) + (1 + \Delta_A)^2}{4Re[Z_L]} \quad (1)$$

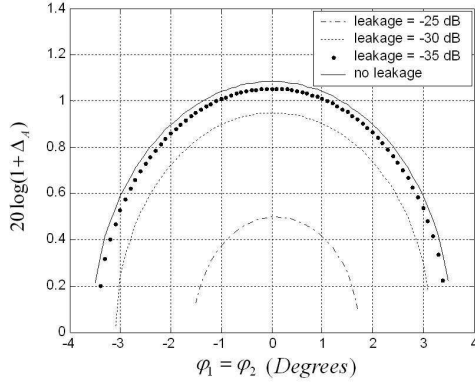


Fig. 3. Gain mismatch versus of phase mismatch for different leakage values of DSB mixers for a fixed  $SRR_Q$  of 24 dBc

where  $Z_L$  denotes the charge load.

The power of the signal image is [2]

$$image_Q = \frac{1 - 2(1 + \Delta_A) \cos(\varphi_1 + \varphi_2) + (1 + \Delta_A)^2}{4Re[Z_L]}. \quad (2)$$

The total power of the signal leakage is

$$leakage_Q = 2[1 + (1 + \Delta_A)(\sin(\varphi_1) + \sin(\varphi_2)) + (1 + \Delta_A)^2] \frac{10^{L_{dB}/10}}{4Re[Z_L]}. \quad (3)$$

In the sequel, we assume that the charge load  $Z_L$  is constant over the 14 bands. The Spurs Rejection Ratio (SRR) of the quadrature signal in a SSB mixer is

$$SRR_Q = 10 \log\left(\frac{signal_Q}{image_Q + leakage_Q}\right). \quad (4)$$

We can notice that if the DSB mixer has a perfect isolation; i.e.  $L_{dB} \rightarrow -\infty$ , then the SRR ratio tends towards the well-known SideBand Rejection Ratio (SBBR) [2].

Figure 3 gives the gain mismatch versus of the phase mismatch for different leakage values of DSB mixers for a fixed  $SRR_Q$  of 24 dBc. The worst case for the inphase and quadrature outputs are when  $\varphi_1 = -\varphi_2$  and  $\varphi_1 = \varphi_2$ . The common specifications for the leakage of DSB mixers are -30 dB [10] and the degradation of the curve corresponding to the leakage which is small compared to the curve with perfect isolation. Nevertheless, the leakage should not be greater than -30 dB because the tolerance over the gain and phase mismatch are too constraining. For example, if the leakage values are fixed at -30 dB, then a gain mismatch of 0.4 dB imposes a phase mismatch that should not exceed  $2.8^\circ$ .

### B. Low pass filter specifications

Now we assume that the three center frequencies are spectrally pure and the signal at 528 or 1056 MHz is rectangular wave. Due to the high power level of harmonics of a rectangular wave (the third harmonic is 9.54 dB below the fundamental), it is necessary to filter the divide-by-2 output by a low pass filter. For the following study, we will only take into account only the fundamental and the filtered third harmonic

of a rectangular wave.  $Att_{dB}$  denotes the total attenuation of the third harmonic

$$Att_{dB} = -9.54 \text{ dB} - A_{stop} \quad (5)$$

where  $A_{stop}$  is the attenuation of the low pass filter at this frequency.

The power of the third harmonic signal is

$$signal_{3rd\text{harm}} = [1 + (1 + \Delta_A)^2 + 2(1 + \Delta_A) \cdot \cos(\varphi_1 - \varphi_2)] \frac{10^{Att_{dB}/10}}{4Re[Z_L]}. \quad (6)$$

The power of the third harmonic image is

$$image_{3rd\text{harm}Q} = [1 + (1 + \Delta_A)^2 - 2(1 + \Delta_A) \cdot \cos(\varphi_1 + \varphi_2)] \frac{10^{Att_{dB}/10}}{4Re[Z_L]}. \quad (7)$$

The total power of the third harmonic leakage signal is

$$leakage_{3rd\text{harm}Q} = [((1 + \Delta_A) + \sin \varphi_1)^2 + \cos^2 \varphi_1] \frac{10^{(L_{dB} + Att_{dB})/10}}{4Re[Z_L]}. \quad (8)$$

The total spurs power is

$$spurs\ power_Q = image_Q + leakage_Q + signal_{3rd\text{harm}Q} + image_{3rd\text{harm}Q} + leakage_{3rd\text{harm}Q}. \quad (9)$$

Finally the SRR of the quadrature signal is

$$SRR_Q = 10 \log\left(\frac{signal_Q}{spurs\ power_Q}\right). \quad (10)$$

Figure 4 gives the gain mismatch versus the phase mismatch for different third harmonic attenuation for a fixed  $SRR_Q$  of 24 dBc. A 30 dB attenuation gives nearly the same tolerance as a perfect filtering. We choose third order low pass Chebyshev filters with a 0.5 dB ripple in the bandpass. Since the VCO output can be considered as a sine wave, then there is no need to filter the 4224 MHz frequency.

### C. Band pass filter specifications

For the following simulation, the filters at the divide-by-2 outputs attenuate by 30 dB the third harmonic. We use DSB mixers with 30 dB leakage. Careful design of the layout allows to minimize the delay error, yielding a phase mismatch of  $|\varphi_1|, |\varphi_2| \leq 2.5^\circ$  [4]. The  $SRR$  must not be below 24 dBc, so we fix the DSB gain mismatch at 0.423 dB corresponding to  $\Delta_A = 0.05$ . Those specifications are the same for all SSB mixers. The aim of the band pass filter is to have the 3 center frequencies as spectrally pure as possible with the smallest complexity. We choose band pass filters of order 2, and the highest quality factor allowed is 10, which is a realistic assumption in current CMOS technology [10].

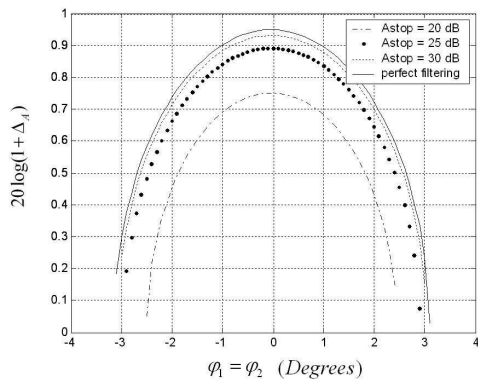


Fig. 4. Gain mismatch versus of phase mismatch for different  $3^{rd}$  harmonic attenuation for a fixed  $SRR_Q$  of 24 dBc

The 4488 MHz center frequency is used to generate two other center frequencies, and it must also be spectrally pure because spurs of 4488 MHz will propagate to the others. Table II gives the frequency of the irremediable spurs due to the SSB mixers at the 4 SSB mixers output and the Q value chosen for the 4 band pass filters. The spurs must be well filtered in order to have 3 center frequencies as pure as possible. For example, image and leakage signals at the 4488 MHz SSB output are respectively 3960 and 4224 MHz, which are very close from the desired frequency. Q value must be chosen to attenuate the closest spurs to a minimum of 3 dB. Then Q value of 4488 MHz filter must be equal to 8.5. The spurs at the output of the other mixers are far from filters center frequency, which allows to have a non constraining Q of 1.6, 1.75 and 2.5.

TABLE II  
IRREMEDIABLE SPURS DUE TO SSB MIXERS AT THE 4 SSB MIXERS  
OUTPUTS

| Filter center frequency (MHz)                 | 2640 | 4488 | 6600 | 9240 |
|---|------|------|------|------|
| 1 <sup>st</sup> input leakage frequency (MHz) | 528  | 264  | 2112 | 2640 |
| 2 <sup>nd</sup> input leakage frequency (MHz) | 2112 | 4224 | 4488 | 6600 |
| Image frequency (MHz)                         | 1584 | 3960 | 2376 | 3960 |
| Filter quality factor (Q)                     | 2.5  | 8.5  | 1.6  | 1.75 |

#### IV. SIMULATIONS

Simulations have been performed using Advanced Design System in a worst-case scenario corresponding to  $\Delta_A = 0.05$ ,  $|\varphi_1| = |\varphi_2| = 2.5^\circ$ , and leakages fixed at 30 dB. The four low pass filters attenuate the third harmonic of the divide-by-2 circuits output by 30 dB. Harmonic Balance simulations give the spurs generated in the FCC spectrum and the total spurs power for I and Q channels in dBc (Table III). The reference power is the power of the desired frequency. Note that powers smaller than 40 dBc are shown. The frequencies used to generate the desired frequencies are multiple of 264 MHz, then spurs generated are also multiple of 264 MHz. For the worst generated frequency (8712 MHz, Fig. 5), the total spurs power is lower than the required -24 dBc. Without any surprise, the best generated frequencies are the 3 center frequencies and the worst are those which pass through the last SSB mixer.

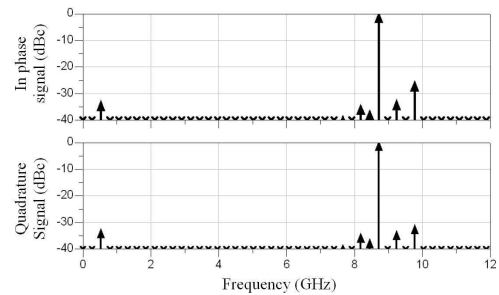


Fig. 5. Output spectrum of the synthesizer for the 8712 MHz selected frequency

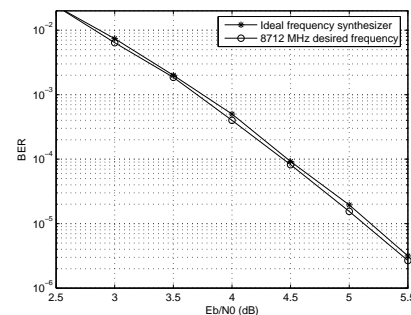


Fig. 6. BER degradation in presence of spurs generated by the 8712 MHz desired frequency

For the following simulations, we assume that all channels are used by a peer. All peers transmit at the same power and other peers are considered as interferers. Because the frequency spurs are multiple of 264 MHz and zero-IF architecture is used, all spurs downconvert another peer signal at the baseband level. Figure 6 gives the Bit Error Rate (BER) of a coded 480 Mbps transmission [1] with an AWGN channel over the worst generated frequency. The target BER is  $10^{-5}$  and the degradation in term of  $Eb/N_0$ , and so the sensitivity, is very low ( $< 0.1$  dB).

The realistic phase noise of the integrated VCO and the crystal oscillator are respectively -125 dBc/Hz at 1 MHz and -135 dBc/Hz at 1 KHz [10], which are not constraining. The synthesizer phase noise has been simulated using AC simulation and gives a phase noise lower than -105 dBc/Hz at 1 MHz for the worst generated frequency.

#### V. CONCLUSION

We proposed a low complexity frequency synthesizer that allows to generate all the 14 desired frequencies for UWB. This synthesizer is composed by a single PLL, trivial divide-by-2 circuits, four fixed frequencies, a broad-band SSB mixer, and low orders filters. The total spurs power of each desired frequency is below the necessary 24 dBc because of non-constraining characteristics. BER simulation shows that the sensitivity degradation corresponding to the worst-case scenario is below 0.1 dB. The transition time between two frequencies is fixed by the transition time of multiplexers, which is lower than the desired 9.47 nsec.

TABLE III  
SPURS GENERATED IN THE FCC SPECTRUM AND TOTAL SPURS POWER FOR INPHASE AND QUADRATURE CHANNELS

| Band(MHz) | Spurs generated in the FCC spectrum (Freq in MHz) |      |      |      |      |      |      |      |      |       |      |      | Total spurs power for I and Q channels (dBc) |       |
|-----------|---|------|------|------|------|------|------|------|------|-------|------|------|--|-------|
|           | Freq  | I    | Q    | Freq | I    | Q    | Freq | I    | Q    | Freq  | I    | Q    | I  | Q     |
| 3432      | 3168  | 35   | 35.2 | 4488 | 32.2 | 32.6 | 5544 | 25.6 | 29.2 | -     | -    | -    | -24.6  | -28.5 |
| 3960      | 3696  | 35   | 35   | 4488 | 31   | 35.3 | 5016 | 25.5 | 31.9 | -     | -    | -    | -24.4  | -29.1 |
| 4488      | 3960  | 39.2 | 35.7 | 4224 | 34.9 | 35.3 | -    | -    | -    | -     | -    | -    | -34.6  | -33.6 |
| 5016      | 3960  | 31.7 | 25.5 | 4488 | 31.9 | 32.2 | 4752 | 35   | 35   | 6072  | 40   | 40   | -28  | -24.5 |
| 5544      | 3432  | 31.9 | 25.5 | 4488 | 32.2 | 32.6 | 5280 | 35   | 35   | 7656  | 40   | 40   | -28  | -24.5 |
| 6072      | 3960  | 39   | 39   | 5808 | 36.2 | 36.2 | 6600 | 32.7 | 33.3 | 7128  | 25.6 | 31.9 | -24.6  | -28.3 |
| 6600      | 6336  | 36.2 | 36.2 | 4488 | 39   | 39.4 | -    | -    | -    | -     | -    | -    | -34.5  | -34.5 |
| 7128      | 5016  | 39.1 | 39.4 | 6072 | 31.9 | 25.6 | 6600 | 33.6 | 34   | 6864  | 36.2 | 36.2 | -28.4  | -24.8 |
| 7656      | 5544  | 35.1 | 27.3 | 6600 | 32.3 | 32.6 | 7392 | 36.1 | 36.1 | 9768  | 40   | 40   | -29.3  | -25.9 |
| 8184      | 7656  | 34.2 | 34.2 | 7920 | 36.3 | 36.3 | 9240 | 33   | 33.4 | 10296 | 25.6 | 31.9 | -24.3  | -27.7 |
| 8712      | 7656  | 38.3 | 38.5 | 8184 | 34.2 | 34.2 | 8448 | 36.3 | 36.3 | -     | -    | -    | -24.1  | -27.1 |
| 9240      | 8712  | 33.7 | 33.7 | 8976 | 36.1 | 36.1 | -    | -    | -    | -     | -    | -    | -31.8  | -31.8 |
| 9768      | 8712  | 32.2 | 26.3 | 9240 | 35.1 | 35.4 | 9504 | 36.3 | 36.3 | -     | -    | -    | -29.4  | -25.6 |
| 10296     | 8184  | 30.7 | 25.3 | 9240 | 33.8 | 34.3 | 9768 | 34.2 | 34.2 | 10032 | 36.3 | 36.3 | -27.4  | -24.3 |

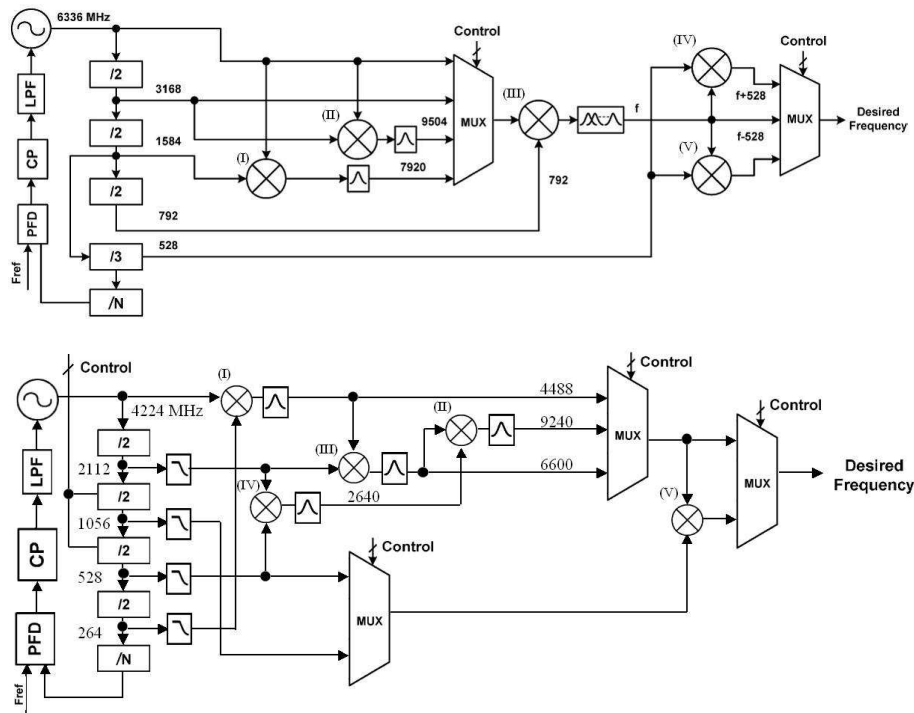


Fig. 7. Frequency synthesizer proposed in [2] (top) and the low complexity, high performance proposed synthesizer architecture (bottom)

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